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Study on determination of parasitic resistances in SiC MESFET's

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ABSTRACT

STUDY ON DETERMINATION OF PARASITIC RESISTANCES IN SiC MESFET's

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This paper presents a simple analytical method for extracting the source, drain and gate parasitic resistances. The proposed method is based on the three simple DC measurements. The parasitic resistance values are received through numerical iterations. The parasitic resistances generates from the short channel effect where S/D curve may closed. The resistance measurements prove that the method is sensitive to the accuracy of the measured voltages. Identical Schottky diodes are assumed and the values of the parasitic resistances are extracted for device frequency response and switching performance.

CHAPTER 1
INTRODUCTION

In recent years, silicon carbide has received increased attention because of its potential for a wide variety of high-power devices. The unique material properties of SiC, high electric breakdown field of 4×10^6 V/cm, high saturated electron drift velocity of 2×10^7 cm/s, and high thermal conductivity of 4.9 W/cm-°K are what give this material its tremendous potential in the power device arena. The two SiC poly types, 6H and 4H are having the biggest impact on power devices. The most significant difference between the 6H and 4h is that the electron mobility in 4H-SiC is two times that of 6H-SiC perpendicular to the c-axis and almost 10 times that of 6H-SiC parallel to the c-axis [1]. SiC devices will have better performance compared to Si and GaAs devices for high voltage applications because of SiC's higher breakdown field, saturated drift velocity, and thermal conductivity even though the electron mobility is lower. Silicon Carbide (SiC) MESFET's are emerging as a promising technology for high-power microwave applications due to a combination of superior properties of SiC, including a high breakdown electric field, high saturated electron velocity and high thermal conductivity. Because of the excellent thermal properties of SiC, the ultimate power level attainable from a SiC MESFET at any given frequency has been modeled to be at least 5 times of devices made of GaAs. The development of SiC electronic devices has been limited in the past by the lack of availability of large, high quality SiC substrates.

SiC metal semiconductor field effect transistors (MESFETs) are fabricated with more than 60 W of output power at 450 MHz from single 21.6 mm gate periphery devices (2.9 W/mm) and 27 W of output power at 3 GHz from single 14.4 mm. devices (1.9 W/mm). The excellent device performance has been attributed to the improved substrate and epitaxial films quality, optimized device thermal management, and enhanced device fabrication technologies. SiC MESFETs are popular devices for power amplifier design in high power and high-temperature applications because of SiC's superior properties, such as high breakdown voltage, high thermal conductivity, and high-saturated electron velocity [2]. The development of SiC devices in wireless

applications provides the impetus of researching in the area of nonlinear modeling, which is useful for device performance analysis in designing microwave circuits and characterizing the device technological process.

Silicon carbide (SiC) is one of the most promising alternatives to silicon (Si) for power semiconductor devices due to its superior material characteristics. For instance, its high breakdown electric field strength results in high voltage-blocking capability with a much lower on-resistance compared with Si, while its large band-gap energy leads to higher temperature operation capability, higher radiation hardness, and relatively higher thermal conductivity – an important benefit in terms of power dissipation. With rapid growth of mobile communications represented by portable telephones, further increases in the output of high-frequency power transistors for the base stations are required. Also, in the fields of satellite communications and radar, realization of high-power transistors replacing electron tubes such as TWTs and magnetrons is desirable for size reduction, weight reduction, and extension of transmitter life. As a transistor meeting such needs, the metal semiconductor field effect transistor (MESFET) based on silicon carbide (SiC) has been attracting attention. SiC is superior in material characteristics such as the electric breakdown field and thermal conductivity and is expected theoretically to provide high power density as a high-frequency transistor.

Silicon carbide (SiC)-based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power, and high-radiation conditions under which conventional semiconductors cannot adequately perform. Silicon carbide’s ability to function under such extreme conditions is expected to enable significant improvements to a far-ranging variety of applications and systems. These range from greatly improved high-voltage switching for energy savings in public electric power distribution and electric motor drives to more powerful microwave electronics for radar and communications to sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines [1-2].

In the past decade, tremendous progress has been made in the material growth and processing of wide band-gap semiconductors, particularly SiC and GaN, and high quality SiC and GaN wafers are now commercially available [3]. Both types of semiconductors have very wide band-gap (4H–SiC = 3.2 eV and GaN = 3.4 eV) and are visible blind [3]. Moreover, 4H-SiC has very high breakdown field, outstanding radiation hardness, and excellent chemical and mechanical rigidity, good thermal conductivity and as such are excellent candidates for photo detection in high temperature and high radiation environment conditions [3]. Due to the wide band-gap of SiC and GaN, the leakage current can be many orders of magnitude lower than the leakage current of Si detectors, making SiC and GaN good candidates for high sensitivity visible blind UV detection. GaN has the advantages of the availability of hetero-structures, which allows designing cutoff wavelength in the UV range by using AlGaN with different Al percentage [4]. It therefore adds great flexibility in detector design and relieves or eliminates the requirement of optical filters. SiC, however, has much better material maturity compared to GaN material. Additionally, SiC substrate and epi-growth technologies have developed to such a level as to allow the fabrication of many different types of SiC photo detectors with desired features. SiC UV p-i-n photodiodes have already been fabricated and are commercially available. SiC avalanche photodiodes with extremely high gain and low excess noise have also been demonstrated [5].

With the advancements and research in MESFET, optically controlled MESFETs also referred to as OPFETs have received considerable attention due to the inherent advantages in the high-speed optical switching and high frequency optical modulation/demodulation applications [6]. Theoretical and experimental observations have shown that the variations of the DC and dynamic properties in MESFETSs when a light beam strikes the transistor gate can be accounted for by an appropriate change in the gate junction equivalent to the built-in voltage [7]. In order to establish the OPFET device characteristics, a number of theoretical and experimental observations have been continuously reported [8-9] exploring the illumination effect on the static and dynamic characteristics of MESFET devices for various biases, optical responses of the MESFET both at DC and microwave frequencies and large-signal characteristics of the MESFET

under He-Ne illumination source. The optically controlled MESFET (or OPFET) is of great importance because of its potential as a photo detector and pre-amplifier, rf. switch and tuner, etc. Different mechanisms, which are responsible for the enhanced terminal properties of the optically controlled MESFET, are:

1. Photo-induced voltage across the Schottky barrier [10], [11],
2. Photo generated carriers below the gate [12-13] and
3. Photo conductivity effect in the source-gate and drain gate regions and the change in the gate depletion width [14].

Further, the experimental observation showed a positive voltage across the depletion region between the n-type channel and the semi-insulating substrate suggesting that the drain current enhancement is closely related to the channel width modulation of the device [15]. Considerable interest has been shown in studying and modeling Optically Controlled Field Effect Transistors (OPFET's) fabricated with Schottky gate configuration. These OPFET's are expected to emerge as promising detectors for use in integrated optoelectronic circuits. A number of theoretical and experimental investigations on the effect of illumination on MESFET structures have been reported. Preliminary investigations reveal that photo response of illuminated MESFET is due to the optically generated carriers, which increase the conductivity of the channel and the photo voltage developed across the Schottky barrier, which affects the applied reverse voltage on the gate. Simple models have been developed by several workers in order to explain the results of experimental investigations on the effect of illumination on commercially available GaAs MESFET's [16]. The large signal characteristics of an illuminated GaAs MESFET have been reported. Unfortunately, the models proposed so far are either too complicated or not adequate to be used for circuit simulation purposes. A simple yet fairly accurate model, which takes into account, all the important physical phenomena involved in an illuminated MESFET need to be considered for this purpose.

GaAs OPFET appears to be an important optical transducer for optical communication, integrated optics, and optical computer. Studies on GaAs OPFET show

that by controlling the radiation flux density, one can control the threshold voltage, drain-source current, and RF switching parameters of the device. B. B. Pal and S. N. Chattopadhyay studied the GaAs OPFET Characteristics Considering the Effect of Gate Depletion with Modulation Due to Incident Radiation. It was found that the photovoltaic effect is important because it develops a forward voltage across the metal-semiconductor junction, which increases with the increase in radiation intensity. This photo voltage modulates the depletion region width below the gate, which, in turn, modulates the channel width. The photo voltage thus is expected to increase the drain-source current. It will reduce the threshold voltage in the normally OFF devices and increase in the normally ON devices. At higher flux density and trap density, the threshold voltage shows nonlinear effect at lower value of implanted dose, which is mainly due to the recombination term. The device is pinched off at a higher drain-source voltage compared to the photo generation case only [17]. Some experiments have shown that the FET dc characteristics may alter with illumination and that FET oscillators may be tuned by varying the intensity of the light falling on the active region of the device. Also, some authors have recently reported high-speed optical detection with GaAs MESFET'S [18].

SiC photodetectors/photodiodes have a spectral response of approximately 210 – 380 nm and are not sensitive to UV radiation outside this region. This makes them ideal detectors in certain applications for monitoring the UV spectrum without the need for solar rejection filters. SiC photodetectors are extremely durable and have been proven to withstand prolonged UV exposure in production quantities in many applications. SiC Photodiodes are used in UV applications. Intrinsic spectral response is limited to the range of 200 - 400nm and no additional blocking of unwanted visual and IR-range of radiation is necessary. SiC photodiodes are proven for outstanding long-term stability under high doses of UV –C-radiation. These devices also have an excellent temperature stability, can operate at 150°C. SiC photodiode is offered with radiation hard standard space approved filters for narrow band such as UV-A, UV-B and UV-C [22].

There has been considerable work done on the development of silicon based optoelectronic integrated circuits (OEIC's) [19]. Mature silicon-processing technology,

including micromachining techniques, can be used to fabricate complex optical structures such as micro optical devices and hybrid optoelectronics. The silicon based OPFET promises excellent compatibility with current silicon IC technology requiring the same or similar low-cost and reliable manufacturing techniques of monolithic silicon-based OEICs. The ion implantation induced defects in a silicon substrate have been characterized by measuring the bulk generation lifetime of MOS capacitor and experiments have been conducted to study the dependence of substrate dopant species (phosphorous and boron) on defect formations. I-V characteristics of ion implanted solar cell devices at optical illumination have shown the efficiency in the range of 0.01%. Phosphorous ion implantation not only results in the transition of the crystalline fullerenes to amorphous material phase, but also produces a significant defect level. An effective loss of photo-generated carriers due to the ion implantation process induced defects in the active channel region of OPFET is a major issue of degradation of quantum efficiency, sensitivity, etc. The channel current obtained from the diffusion and ion implanted OPFET devices are studied and both currents under dark and optical illumination conditions are compared to realize the process-induced defects as major problem for optoelectronics device. Use of direct control of microwave semiconductor devices for optical injection locking, phase shifting, signal distribution and optoelectronic actuator has the potential to enhance the performance of future space borne phased array systems and military and commercial aviation. Previously, several authors have experimentally investigated the effect of light on dc and microwave characteristics of MESFET. Their investigations show that these changes in the characteristics are due to photoconductivity and photovoltaic effects. Further, an analytical study, by the authors taking into consideration material properties of hetro-structures showed that the hetro-structures have a higher sensitivity to optical illumination [20].

The MESFET has been used as an optical detector and control device in microwave applications by several investigators. Of the many advantages of using the MESFET as an optical detector, the most notable is compatibility with GaAs MMIC technology. De Salles has performed a thorough experimental and theoretical

characterization on the MESFET emphasizing the photovoltaic effect, which can be used to increase the drain current and change the gate capacitance. His analysis is concentrated on the active region of the device; photocurrent in the substrate is ignored [21]. Darling has developed a perturbation analysis to account for the photoconductive effect under low-level illumination. Simons derived analytical expressions for I-V characteristics of different types of FET configurations under optical illumination on the devices. He also computed variations in FET small signal parameters such as trans-conductance, channel conductance with illumination and compared with the commercially available OPFETs.

Power Added Efficiency (PAE) is a better figure of merit as it incorporates the transistor power gain. As the power gain (P_{out}/P_{in}) increases, the difference between the power added efficiency and the drain efficiency becomes small. The maximum output power point for the SiC MESFET device was under Class A operation. At a drain bias of V and mA (50%), with the device tuned for maximum power, the device had a peak output power of 30.5 dBm (3.37 W/mm) and a 3 dB compression output power of 30.2 dBm (3.1W/mm). The device had a power added efficiency of 38.4% at this bias point. The best efficiency for this device was under Class B operation, with the device tuned for maximum efficiency. The peak efficiency occurred at a bias of V and mA (5%), where the device exhibited65.7% power added efficiency. The device had 28.4-dBm output power (2.12 W/mm) at the point of peak efficiency, which was also the 3 dB compression points. At this bias point, the device had 28.8-dBm maximum output power (2.27W/mm), but efficiency decreased to 61.3% as the device went into deep compression. The RF device characteristics at peak output power and peak efficiency are seen in Figs. 2 and 3, respectively. It should be noted that the high drain bias of50 V for the large signal measurements requires a very high gate-drain breakdown voltage of over 100 V. The highest power density and power added efficiency is reported to SiC MESFET as is two times larger than GaAs MESFET. The low frequency noise research was conducted on SiC Metal-Semiconductor Field-Effect Transistors (MESFETs).

The least complex SiC power device is the Schottky rectifier, which consists of an N+ doped substrate with backside ohmic contact, a lightly doped epitaxial drift layer and a topside Schottky contact with a high-resistivity edge termination. The Schottky diode is fabricated by evaporating a high work function metal, such as titanium, nickel, or gold, onto the epitaxial layer to form the Schottky contact and by depositing an ohmic contact metal onto the back of the N^+ substrate [23]. The order of these depositions may be reversed to accommodate annealing of the ohmic contact. The process is self-aligned to the Schottky contact because the Schottky metal acts as a mask preventing damage under the contact. The most important device properties are high reverse breakdown voltage and low forward resistance, which produces a high forward current density.

CHAPTER 2
SiC MATERIAL

2.1 SiC BACKGROUND:

The requirement of a successful VLSI (very large scale integration) technology imposes severe limitations on the power consumption and demands on the speed of the basic device. As the device dimensions and power supply voltages are reduced, the SiC MESFET (Metal-Schottky Field Effect Transistor) begins to look attractive for logic and memory applications. Also, the use of ion implantation to form the channel of the device promises a high degree of control over uniformity and reproducibility in the fabrication of devices. The structure of Silicon Carbide is shown in Figure 2.1 [24].

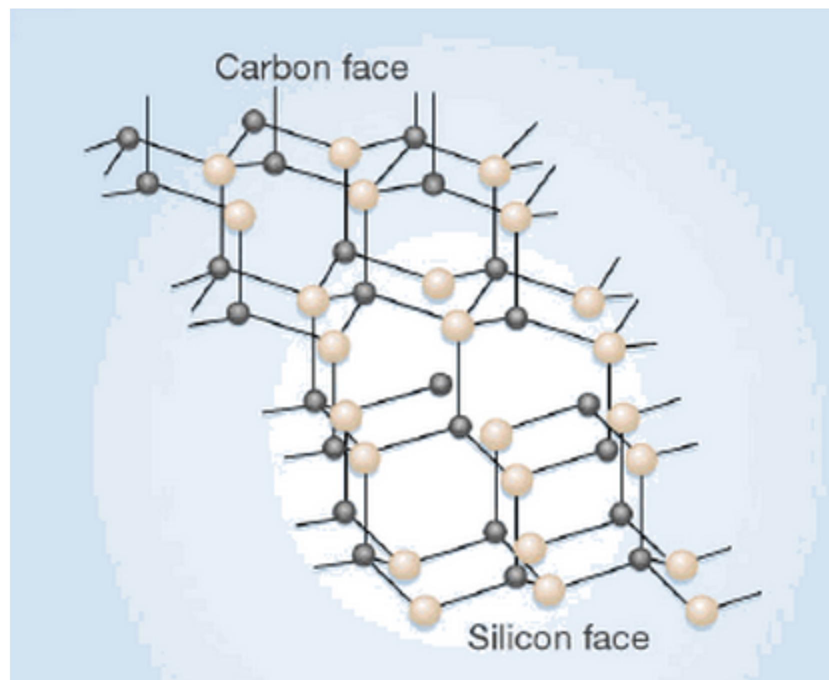

Figure 2.1 Structure of Silicon Carbide

There are several articles in the literature, which deal with the description of the I-V characteristics of structures having uniform doping concentrations or employ a two-dimensional computer simulation, which utilizes a specific channel profile. For very short channel devices, the incorporation of two-dimensional effects is necessary [24].

For moderately long channel devices fabricated with a shallow implanted channel, the channel concentration is highly nonlinear with depth and for these cases it is desirable using a one-dimensional analysis, to have an accurate analytical description of the device which directly reflects the parameters describing the implanted distribution. Such a model may then be appropriately modified as the device size decreases to include short channel effects. (SiC), also known as carborundum is a compound of silicon and carbon with chemical formula SiC. It occurs in nature as the extremely rare mineral moissanite. Silicon Carbide powder has been mass-produced since 1893 for use as an abrasive. Grains of silicon carbide can be bonded together by sintering to form very hard ceramics, which are widely used in applications requiring high endurance, such as car brakes, car clutches and ceramic plates in bulletproof vests. Electronic applications of silicon carbide as light emitting diodes and detectors in early radios were first demonstrated around 1907, and nowadays SiC is widely used in high-temperature/high-voltage semiconductor electronics. Large single crystals of silicon carbide can be grown by the Lely method; they can be cut into gems known as "synthetic moissanite". Silicon carbide with high surface area can be produced from SiO_2 contained in plant material. The 3-D structure of Silicon Carbide is clearly shown in Figure 2.2 [24].

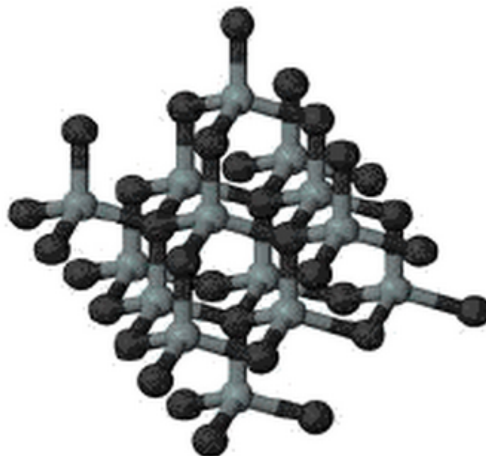

Figure 2.2 3-Dimensional Structure of Silicon Carbide

Silicon carbide has been a perennial candidate for use in the manufacture of semiconductor electronic devices. Silicon carbide has a number of characteristics, which make it theoretically advantageous for such uses. These include a wide band gap, a high

thermal conductivity, a low dielectric constant, a high-saturated electron drift velocity, a high breakdown electric field, and a high melting point. Taken together, these properties indicate that semiconductor devices formed from silicon carbide should be operable at much higher temperatures than devices made from other semiconductors, as well as at higher speeds at higher power levels, and with an increased device density [25].

Nevertheless, semiconductor electronic devices made from silicon carbide have yet to make a viable appearance in any circumstances other than laboratory research and have yet to reach their commercial potential. This lack of success results, at least partially, from the difficulty encountered in working with silicon carbide. It is an extremely hard material, often used as an abrasive. It often must be worked at extremely high temperatures under which other materials cannot be worked, and from a semiconductor standpoint, crystallizes in well over 150 poly types, many of which are separated by rather small thermodynamic differences. For these latter reasons, production of mono crystalline thin films of silicon carbide that are necessary for certain devices and production of large single crystals of silicon carbide which are useful for other applications, has remained an elusive goal. Additionally, certain doping techniques, which have been successfully developed for other materials, have proved unsuccessful when used in connection with silicon carbide. In particular, the successful use of ion implantation techniques has, until recently, remained unachieved. A few samples of abrasive grains of black Silicon Carbide is shown in Figure 2.3 [26,27].

Figure 2.3 Black Silicon Carbide Abrasive Grains

Recently, however, a number of developments have occurred which have successfully accomplished both single crystal and thin film growth of silicon carbide, as well as successful ion implantation techniques [26].The success of these techniques has made possible improved techniques for producing field effect transistors (FET's) in silicon carbide [26].

2.2 SILICON CARBIDE MANUFACTURING:

Acheson process is a process, which is used mainly for the manufacture of silicon carbide. Currently coke and quartz are used as major raw materials to produce SiC in bulk quantities. SiC has extreme hardness, sharpness and good thermal properties and hence it is employed as an abrasive and refractory material. Acheson process is a carbothermal synthesis of SiC [27]. The main raw materials are SiO_2 and C, which are made to react at high a temperature. Sawdust and salt are also added, so that saw dust burns and provides pores facilitating escape of evolved gas (at high temperatures). Firing is done for about 40 hours and after cooling, the sidewalls are removed. An outer layer of uncombined mixture is broken away, exposing the cylindrical mass of sharp, brilliant crystals [27].

The whole reaction process is very complex and the productivity is low. A robust 1-D mathematical model considering conduction, convection and radiation as heat transfer modes are developed. Finite Volume Method has been employed to solve the heat balance equations. To validate the model, an experimental facility has been developed at laboratory scale. Both model and experimental data show a good agreement with each other. Currently, efforts are on to develop a 2-D mathematical model for the process and to validate it experimentally [26,27]. A Graphical User Interface for the process is shown in Figures 2.4 and 2.5.

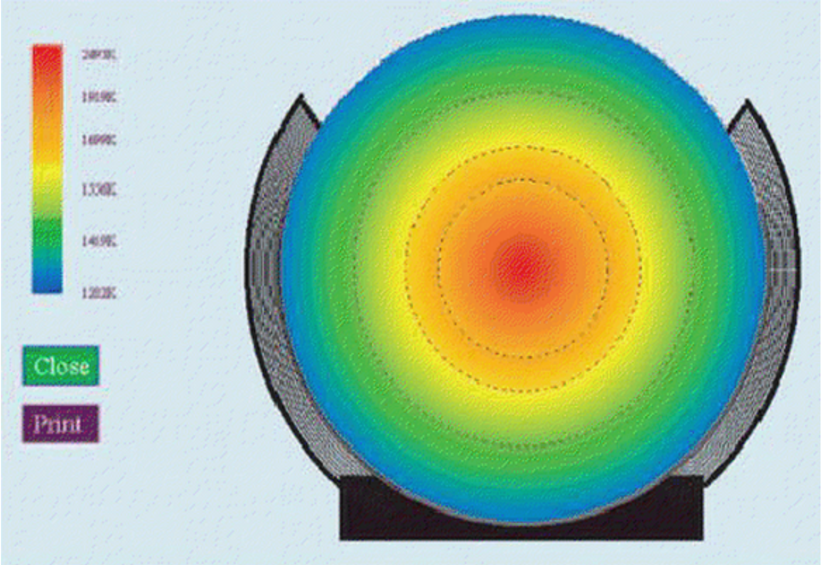

Figure 2.4 GUI developed for the Acheson process to plot the results in contours form

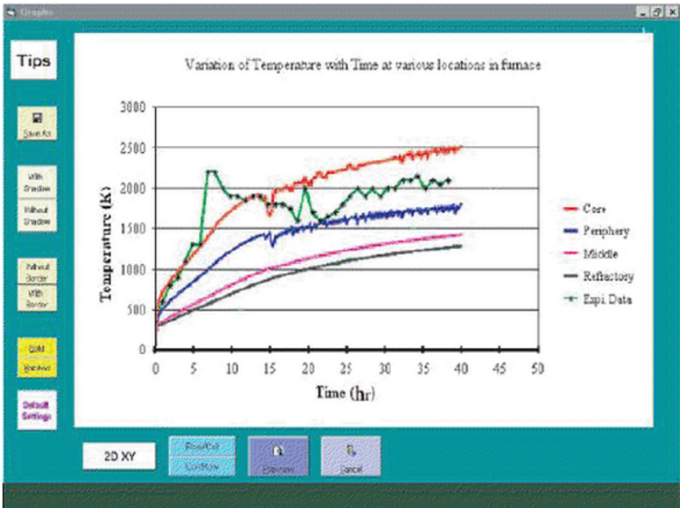

Figure 2.5 GUI developed for the Acheson process to plot the results

2.3 HISTORY OF SILICON CARBIDE:

Some scientists had reported early, non-systematic and often non-recognized syntheses of silicon carbide. They attached one lead from a dynamo to a discarded plumber's bowl, filled the bowl with clay and powdered coke, inserted the other lead into the mix and threw the switch. The Figure 2.6 shows the replication of past LED experiments [27].

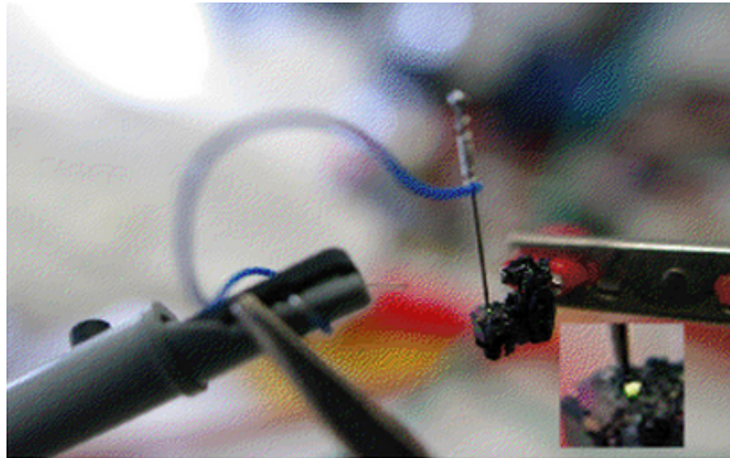

Figure 2.6 A replication of H.J. Round's LED experiments

Nothing seemed to happen, until they noticed a few bright specks on the end of the leads. When they drew one lead across a pane of glass, it cut like a diamond, making SiC the first man-made substance hard enough to cut glass. This method of growth became known as the Acheson process. They later developed the electric smelting furnace around 1885, which used this process; it was then fist recognized it as a silicide of carbon and given its chemical formula SiC. SiC does not occur naturally, so it cannot be mined like other minerals. The only occurrence of SiC in nature is found in meteorites [28].

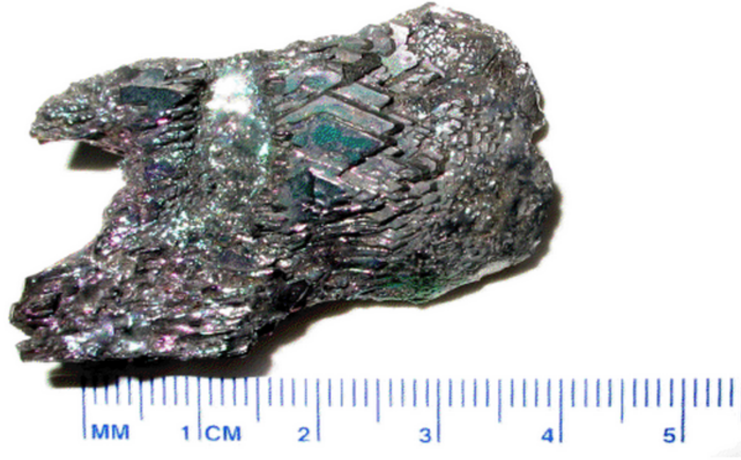

Figure 2.7 Piece of silicon carbide (SiC) Material used in steel making

A piece of Silicon Carbide material that is used for making steel is shown in Figure 2.7. To date, SiC LEDs, diodes, FETs, and numerous other components have already been in commercial production, and we can expect them to be joined by many other electronic devices in the not too distant future. The current state of wide-band-gap semiconductor technology matches that of silicon technology in the late 1970s. Wafers are typically less than 4 in., highly defective and costly, and process techniques are in the development stage. But unlike the early days of silicon device processing, wide-band-gap technology developers can learn from more than 30 years of materials processing development and fabrication improvements [29].

2.4 CHARACTERISTICS OF SILICON CARBIDE:

Silicon Carbide (SiC) belongs to a class of semiconductors having wide band gap, which means they are relatively insensitive to increased temperatures. It possesses many favorable properties making it interesting for high-temperature, high frequency and high-power applications. Its thermal conductivity is greater than that of copper, so it rapidly dissipates heat radiation. It is also resistant to many chemicals, as well as highly resistant to radiation. Silicon carbide is extremely hard allowing devices to operate under extreme pressure. It also possesses high field strength (approximately 10 times that of Si) and high saturation drift velocity (higher than GaAs), characteristics suggesting that devices made of it can be smaller and more efficient than those made of

silicon. With these characteristics, Silicon Carbide is a great candidate for a semiconductor material used in high-heat environments as to monitor temperature, as well as many other practical applications. The basic parameters and properties of major SiC polytypes are displayed in the Table 1 [30].

Polytype	3C (β)	4H	6H (α)
Crystal structure	Zinc blende (cubic)	Hexagonal	Hexagonal
Space group	T^2_d-F43m	C^4_{6v}-P6_3mc	C^4_{6v}-P6_3mc
Pearson symbol	cF8	hP8	hP12
Lattice constants (Å)	4.3596	3.0730; 10.053	3.0730; 15.11
Density (g/cm^3)	3.21	3.21	3.21
Bandgap (eV)	2.36	3.23	3.05
Bulk modulus (GPa)	250	220	220
Thermal conductivity (W/(cm·K))	3.6	3.7	4.9

Table 1 Properties of major SiC polytypes

A wide bandgap also allows SiC devices to operate at shorter wavelengths, enabling the creation of blue LEDs that could not be made from silicon. Moreover, a full-color LED display became possible with the existence of blue LEDs, as blue was a missing primary color. Within limits, there is no reason why a SiC device should not operate at 500ºC or higher, a realm that Si does not even approach. The thermal conductivity of SiC even exceeds that of copper; therefore any heat produced by a device is quickly dissipated. SiC forms a protective SiO_2 skin that to prevents further oxidation at very high temperatures, and in non-reducing atmospheres. Its inertness to chemical reactions also implies that devices have the potential to operate even in the most hazardous environments. SiC is extremely hard, probably most familiar to people as the grit coating on sandpaper. This hardness again implies that SiC devices can operate under conditions of extreme pressure. Of importance to our nuclear and space age is the fact that SiC is extremely resistant to radiation and can be used close to reactors or for space electronic hardware [31,32].

2.5 LOW-DOPED N-TYPE SIC MESFET:

The power handling capabilities and high temperature operation of SiC makes it an ideal material for the production of rectifiers.

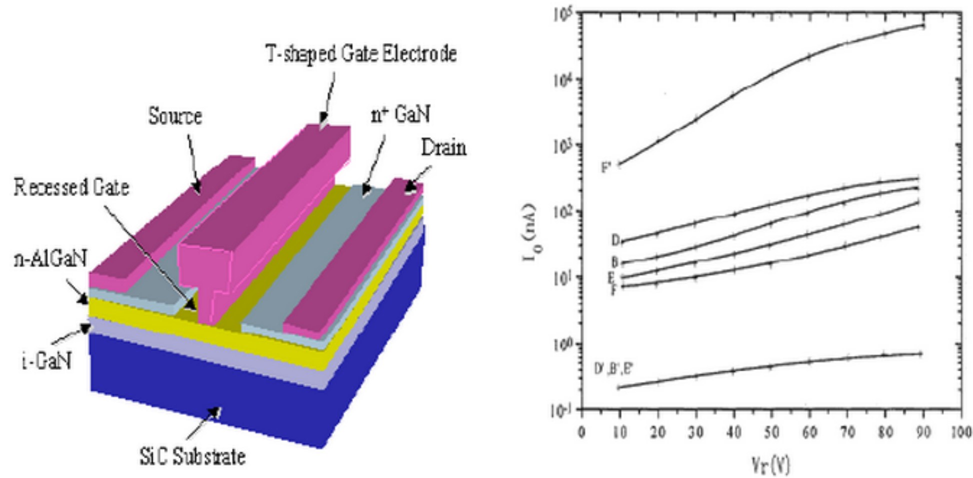

Figure 2.8 Low-doped n-type SiC MESFET

Figure 2.8 shows the low doped n-type SiC MESFET. Auburn University demonstrated an operational amplifier capable of working to temperatures up to 400ºC, which further demonstrates SiC's high tolerance to temperature. A team from Rutgers University, NJ, and United Silicon Carbide, NJ, reported results from an all-SiC half-bridge inverter using 4H-SiC power bipolar transistors at voltages of up to 400 V and current levels of up to 22 A. The group also reported 4H-SiC junction barrier Schottky diode fabrication and characterization in an inductively loaded half-bridge inverter at power levels of up to 100 kW. Another particular device of interest device that has been made is SiC photo-diodes for the ultraviolet. The photo-diode is of interest in that it can be used in such harsh environments, a property which can be exploited for the monitoring of engine combustion. These photodiodes have been shown to achieve up to four orders of magnitude higher sensitivity than its Silicon counterpart. Today, photo detectors made from SiC are used in numerous locations such as gas turbines, jet engines, and many similar applications. These sensors are primarily used to determine basic properties of a combustion flame, specifically, whether the flame is on or off [32].

2.6 ION IMPLANTATION:

In general, the heat treatment required in the activation of the ion-implanted channel is short enough that the original Gaussian profile is preserved. Even if the profile is altered it may still be described by a Gaussian with a modified value of range parameter (Rp) and straggle parameter (σ). Here an analytic description of an ion-implanted MESFET based on the assumption of a resultant Gaussian profile (described by Rp, and σ) and the total implanted dose Q is developed. In the following comparison with data it will also be assumed that the Gaussian distribution of the initially implanted profile is retained through the process. In addition, the effects of the higher moments of the implant distribution are neglected in this analysis although it is noted that the joined half-Gaussian description of the third moment may be easily incorporated if necessary [33,34].

Ions implantation is a doping technique in which the desired impurities (dopants) are introduced into the semiconductor lattice by bombarding the surface with high-energy dopant ions. This technique offers more control over dopant levels and locations than most of the other doping techniques [34]. The technique of ion implantation is extremely attractive for the fabrication of GaN and SiC based devices because it can introduce a well-defined impurity concentration at a designed zone. In fabrication of such GaN-based devices, ion implantation represents a very attractive tool for several technological steps, such as electrical and optical selective-area doping, dry etching, electrical isolation, quantum well intermixing, and ion-cut. It is well known that a successful application of ion implantation depends on understanding the production and annealing for curing radiation damage. Thus, detailed studies of ion implantation damage in GaN are not only important for investigating fundamental defect processes in solids under ion implantation but are also essential for the fast developing GaN industry. Ion implantation is preferred because of controlled, low or high dose can be introduced (10^{11} -10^{18} cm^{-2}), depth of implant can be controlled and high temperature annealing can activate slow impurity diffusion. Ion implantation can independently control the dopant concentration, junction depth. It is a low temperature, PR mask and anisotropic dopant profile. Up to now, several outstanding reviews have appeared in the literature addressing various aspects of ion

implantation into GaN. Figure 2.9 shows the ion implantation impurity profile. However, very recently, the field of ion implantation into GaN has matured considerably. Before implantation can become a viable technology for 111-nitrides, it is essential that implantation properties such as ion disorder and its removal by thermal annealing and the ability to electrically activate implanted dopants are studied in detail. Such studies have been limited until quite recently when Zolper showed that GaN could be activated both n-type and p-type by Si implantation. In addition, Tan showed that ion disorder built up rather slowly in GaN with increasing Si ion dose even at liquid nitrogen temperatures as a result of dynamic recovery of disorder during implantation. However, it is possible to amorphise GaN at extremely high implantation doses at liquid nitrogen temperatures.

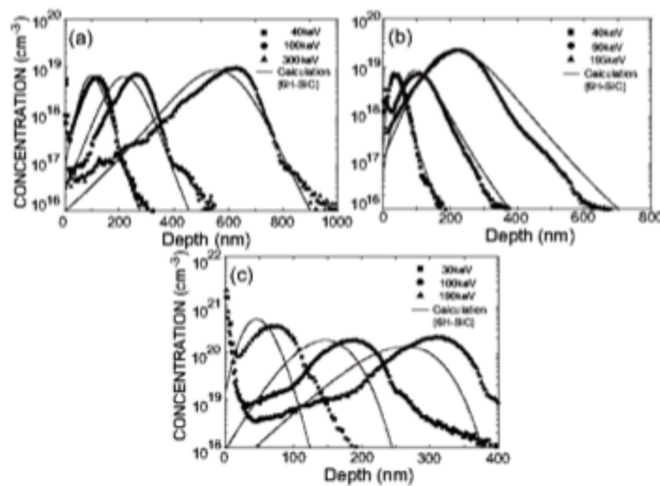

Figure 2.9 Ion Implantation impurity profile

Ion implantation is an enabling technology for creating selective area doping and forming high resistance regions in device structures. For the development of ion implantation doping for advanced GaN-based electronics, it is important to understand the dopant activation process, and implantation-induced damage generation and removal. Recent studies have shown that quite good activation efficiency can be obtained by annealing at 1100^0 C anneal, but implantation damage cannot be significantly removed at this temperature. Annealing at temperatures $>1300^0$ C are suggested to fully remove the damage and further optimize the transport properties of implanted regions in GaN. Since these temperatures are beyond the capability of most rapid thermal annealing systems,

new annealing apparatus must be developed. Consequently, there is an urgent need to carry out detailed studies on the dopant activation, impurity redistribution, defect removal, and surface degradation at these elevated temperatures. Efficient surface protection must be developed to prevent material decomposition and N_2 loss from the GaN surfaces.

Ion implantation is also attractive for inter-device isolation and producing current guiding. Efficient compensation has been achieved in the GaN materials by using N or He implantation. However, the isolation is not stable at high temperatures, i.e. typical implant damage compensation. Implantation in In-containing III-V nitrides has shown that InGaN, as used in LED, laser cavity, or transistor channel, is difficult to be rendered highly resistive. The defect level is usually high in the energy gap, not near midgap, as is ideal for implant isolation. There is a strong need for an understanding of the implant isolation process and mechanism in III-V nitride materials because of the emerging applications for high temperature, high power electronics based on this material system. In particular, attempts need to be made to explore thermally stable implant isolation in GaN, and significant compensation must be achieved in the In-containing nitrides.

Ion implantation of the aluminum ions at room temperatures, followed by annealing at about 1800° C were discussed in a paper in which they discussed ion implantation in silicon carbide to produce junctions and diodes in which nitrogen, phosphorous, antimony, and bismuth were all implanted at room temperature, and in which antimony was additionally implanted at 500°C, all to produce n-type conductivity. However, the only successful results were in producing donor (n-type) implanted materials and they admits little or no success in creating p-type SiC using implant and anneal procedures similar to those used for the n-type dopants. A setup of ion implantation process is shown in Figure 2.10 [35].

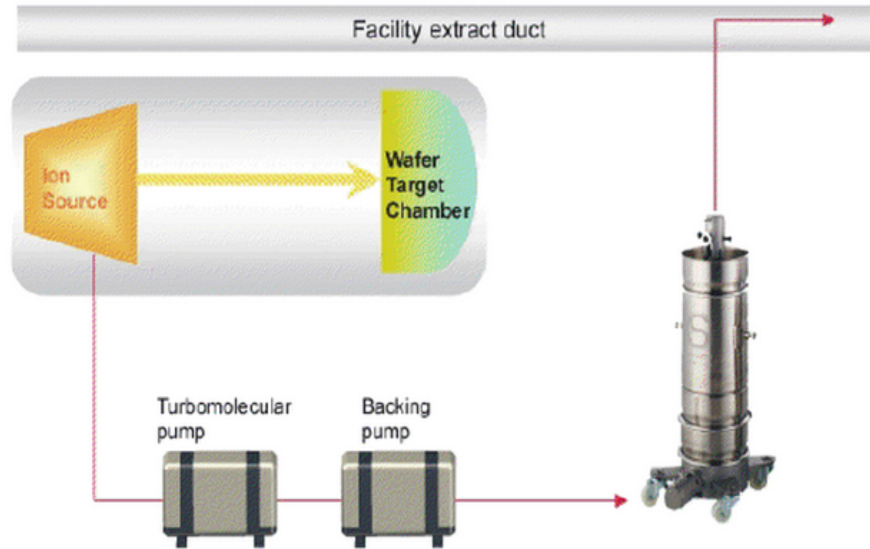

Figure 2.10 Ion Implantation process Setup

Similarly, boron, aluminum, gallium, and thallium were implanted at room temperature in an attempt to obtain p-type conductivity [35,36].

Accordingly, there presently exists no successful technique for ion implantation of both donor and acceptor dopant ions into mono crystalline silicon carbide, which results in appropriately electrically, activated n and p-type materials [37]. Therefore, it is an object of the present invention to provide a method of forming a diode operable at high temperatures, high power levels and under conditions of high radiation density which comprises forming a region of mono crystalline, electrically activated doped SiC having a first conductivity type on a substrate of mono crystalline doped silicon carbide having the opposite conductivity type by high temperature ion implantation of doping ions into the doped silicon carbide substrate which give the ion implanted region the first conductivity type. The following Figure 2.11 elaborates the ion implantation process in a flow chart [38].

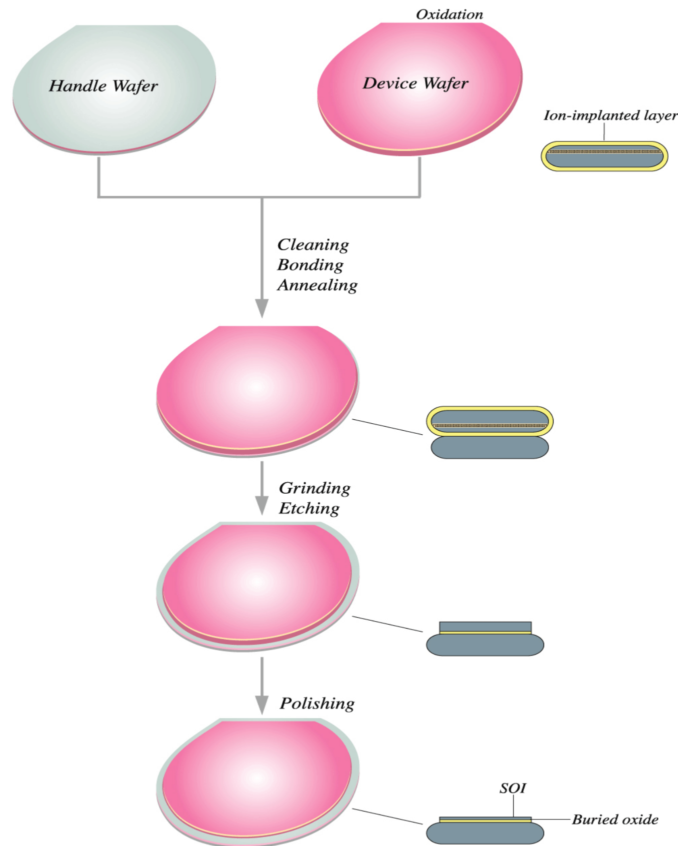

Figure 2.11 The Ion Implantation Flow

It is another object of this invention to successfully form a region of mono crystalline, electrically activated, p-type silicon carbide on a substrate of mono crystalline doped silicon carbide having an n-type conductivity type [39]. It is a further object of the invention to provide a mesa diode operable at high temperatures, high power levels and under conditions of high radiation density which diode comprises a portion of silicon carbide having a first conductivity type, a portion of more heavily doped silicon carbide having the opposite conductivity type positioned upon the first portion of silicon carbide, and respective ohmic contacts to the respective portions of silicon carbide [39]. It is also an object of the invention to provide a method of forming a diode having a region of mono crystalline, electrically activated doped silicon carbide having a p-type conductivity on a substrate of mono crystalline doped silicon carbide having a n-type conductivity by high temperature ion implantation of group III doping ions into the doped silicon carbide substrate [39-40].

It is another object of the invention to provide a planar diode operable at high temperatures, high power levels and under conditions of high radiation density in which the diode comprises a portion of silicon carbide having a first conductivity type, a portion of more heavily doped silicon carbide having the opposite conductivity type immediately adjacent to the portion of first conductivity type and respective ohmic contacts on each of the respective portions of silicon carbide [40].

2.7 SURFACE MODIFICATION PROCESS:

The ion implantation process is conducted in a vacuum chamber at very low pressure (10^{-4} to 10^{-5} torr). Large numbers of ions (typically 10^6 to 10^7 ions/cm^2) bombard and penetrate a surface, interacting with the substrate atoms immediately beneath the surface. Typical depth of ion penetration is a fraction of a micron (or a few millionths of an inch). The interactions of the energetic ions with the material modify the surface, providing it with significantly different properties than the remainder of the material. Specific property changes depend on the selected ion beam treatment parameters, for instance the particular ion species, energy, and total number of ions that impact the surface. The Figure 2.12 explains direct ion bombardment surface modification process [40-41].

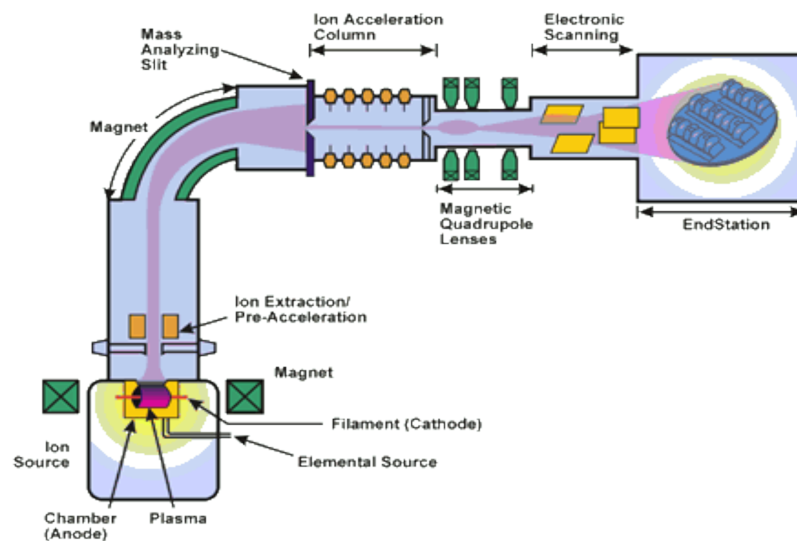

Figure 2.12 Direct ion bombardment surface modification process.

Ions are produced in a multi-step process. Stripping electrons from source atoms in plasma initially forms ions, the ions are then extracted and pass through a mass-analyzing magnet, which selects only those ions of a desired species, isotope, and charge state. The beam of ions is then accelerated using a potential gradient column. Typical ion energies are 10-200 keV. A series of electrostatic and magnetic lens elements shape the resulting ion beam and scans it over an area in an end station containing the parts to be treated [42].

The annealing behavior of an amorphous SiC layer produced by Si MeV implantation into 6H–SiC was investigated by step height measurements, x-ray diffraction analysis, and optical microscopy. Annealing at temperatures between 250 and 700 °C causes a specific densification of the amorphous layer after the first annealing period of 5 min. An Arrhenius law with activation energy of about 184 meV can describe the density increase. Further isothermal annealing up to 10 leads only to minor density changes. Therefore, it can be concluded that the structure obtained after low temperature annealing is metastable. Partial crystallization as a possible reason for densification can be excluded from the x-ray diffraction results. Consequently, amorphous states with continuously varying densities can be produced by low temperature annealing. It should be noted that the density of the amorphous layer depends not only on the annealing temperature, but is also determined by the substrate temperature during ion implantation, which influences the density of the amorphized material.

2.8 APPLICATIONS:

As noted earlier, there are many different areas of application to which SiC can apply. The most obvious application of these devices is in engines, where extremely high temperatures can cause most other semiconductor devices to fail. A more subtle application of Silicon Carbide is for the manufacturing of crucibles, and to replace the quartz wafer carrying racks used in semiconductor manufacturing. In fact, the quartz wafer carrying racks usually last only about one week before it needs to be replaced, whereas the SiC wafer rack can last a couple of years [43].

Again, due to SiC's great tolerance to heat and outstanding corrosion resistance in certain chemical environments, as well as its strength make it a perfect candidate for these applications. Here is a list of what was found about the current SiC applications to name a few: Ballistic armor tiles for personnel, vehicle and aircraft applications, bearings, tooling for semiconductor processing applications including focus rings, susceptors, and gas distribution plates, polishing plates for semiconductor wafers, highly reflective mirrors for lasers, wear components for paper making machines, small quantity special seal faces for the chemical processing industry, actuation and the list goes on. Silicon Carbide replaces metals, tungsten carbide and other ceramic materials, such as aluminum oxide, for these applications [43].

2.9 DRAWBACKS AND LIMITATIONS:

Given all the areas of superior performance, there is a reason that SiC has not replaced Silicon yet. Let us cover the most obvious and limiting areas. First is the current wafer size; the largest production wafer for resale is still around four inches, while silicon is at eight inches plus. The fact is that most semiconductor manufacturers are not set up to handle the smaller wafers anymore. The larger the wafer the more transistors you can fit on it [44].

Second is the heartiness of the SiC as it resists most adverse effects of temperature and chemicals, henceforth, normal transistor fabrication methods do not work well on the SiC chips. Doping via Ion implanting in SiC does not readily diffuse below 2000°C, which presents a problem since SiC sublimes above 1600°C. Also, the ion implantation at 400 keV only penetrates to a depth of approximately 0.5 μm, which means doping must be used during epitaxy for thick layers, such as drift regions. Lastly, for the material robustness, there is no practical SiC wet etching process [45-46].

Micro pipes and polytypes are two most important defects in PVT growth of SiC. However, the origins of micro pipes in SiC crystals are not clear to date and it is rather difficult to control. Sic polytypes in PVT growth of SiC. The above-mentioned two new defects, i.e. triangular etching pits and the shallow hexagonal etching pits, might be

possible sources of micro pipe and polytypes formation. Silicon inclusions in SiC can induce the formation of the other defects such as micro pipes, screw dislocations, planar precipitates and mis-oriented regions [46]. Two schemes can be adopted in order to avoid the formation of dendritic silicon inclusion. Firstly, since the number of Si atoms minus that of carbon atoms in equilibrium for the system of SiC + C increases with temperature [47], a lower growth temperature can be used. Secondly, it is suggested to maintain a lower temperature gradient between the growing surface and the surface of the powder source.

CHAPTER 3
SCHOTTKY DIODE

Schottky diode named after a German physicist, also known, as hot carrier diode is a semiconductor diode with a low forward voltage drop and a very fast switching action. When current flows through the diode there is a small voltage drop across the diode terminals. A normal silicon diode has a voltage drop between 0.6-1.7 V, while a Schottky diode has a voltage drop between 0.15-0.45V. A metal-semiconductor junction is formed between a metal and a semiconductor, creating a Schottky barrier. Typical metals used are molybdenum, platinum, chromium or tungsten and the semiconductor would typically be N-type silicon. The metal side acts as the anode and the N-type semiconductor acts as the cathode of the diode. The lower voltage drop can provide higher switching speed and better system efficiency [48].

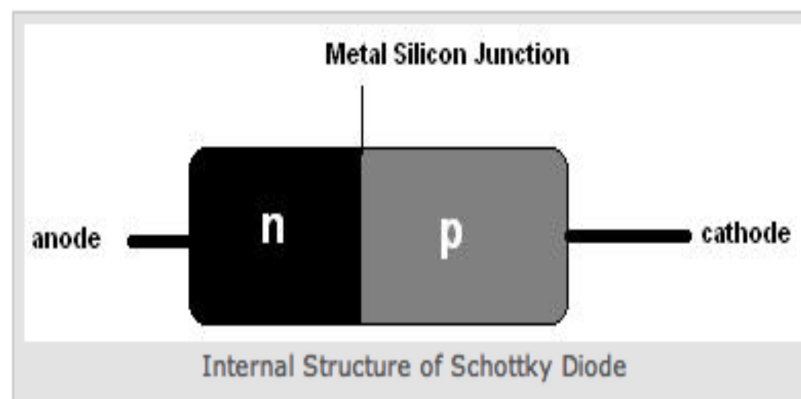

Figure 3.1 Internal structure of Schottky Diode

The most important difference between the p-n and Schottky diode is reverse recovery time, when the diode switches from non-conducting to conducting state and vice versa. Figure 3.1 shows the internal structure of Schottky Diode. Schottky diodes do not have a recovery time, as there is nothing to recover, as there is no charge carrier depletion region at the junction. Schottky diode is a majority carrier semiconductor device. If the semiconductor is doped with n-type, only the n-type carriers play a significant role in normal operation of the device. The majority carriers are quickly injected into the conduction band of the metal contact on the other side of the diode to

become free moving electrons. Therefore no slow, random recombination of n-type and p-type carriers is involved, so that this diode can cease conduction faster than an ordinary p-n rectifier diode. This property allows a smaller device area, which also makes a faster transition and hence Schottky diodes are used in switch-mode power converters. The circuit can operate at frequencies in the range 200KHz to 2 MHz. Small-area Schottky diodes are the heart of RF detectors and mixers, which can operate up to 50 GHz [48].

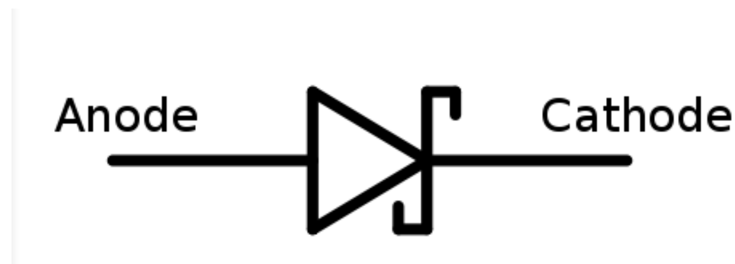

Figure 3.2 Schottky diode Symbol

Schottky diode is used as a high voltage or power rectifier. The Schottky diode rectifier has many advantages over other types of diodes. Figure 3.2 shows the symbol of Schottky diode. The low forward voltage drop offered by Schottky diode power rectifiers is a significant application in many applications. It reduces the power losses normally incurred in the rectifier and other diodes used within the power supply. With standard silicon diodes offering the main alternative, their turn on voltage is around 0.6 to 0.7 V, Schottky diode rectifiers having a turn on voltage of around 0.2 to 0.3V, there is a significant power saving to be gained. The resistance of the material will introduce losses, and the voltage drop across the diode will increase the current. The losses of the Schottky diode rectifier will be less than that of the equivalent silicon rectifier. Schottky diode rectifiers have a much higher reverse leakage current than standard PN junction silicon diodes. The maximum junction temperature of a Schottky diode rectifier is normally limited to the range 125°C to 175°C. Schottky diode rectifiers have a limited reverse voltage capability [49].

3.1 SILICON CARBIDE SCHOTTKY DIODE:

Schottky diodes constructed from Silicon Carbide have a much lower reverse leakage current as compared to a Silicon Schottky diode. As of 2011,these diodes are available in variants up to 1700 V. Silicon Carbide has a high thermal conductivity and temperature has a little influence on its switching and thermal characteristics [50]. With special packaging, it is possible to have operating temperatures of over 500 K, which allows passive radiation cooling in aerospace applications. SiC MESFET's are wide energy gap devices, with high-saturated electron velocity and high melting point. SiC basic MESFET structure is shown in figure 3.3.

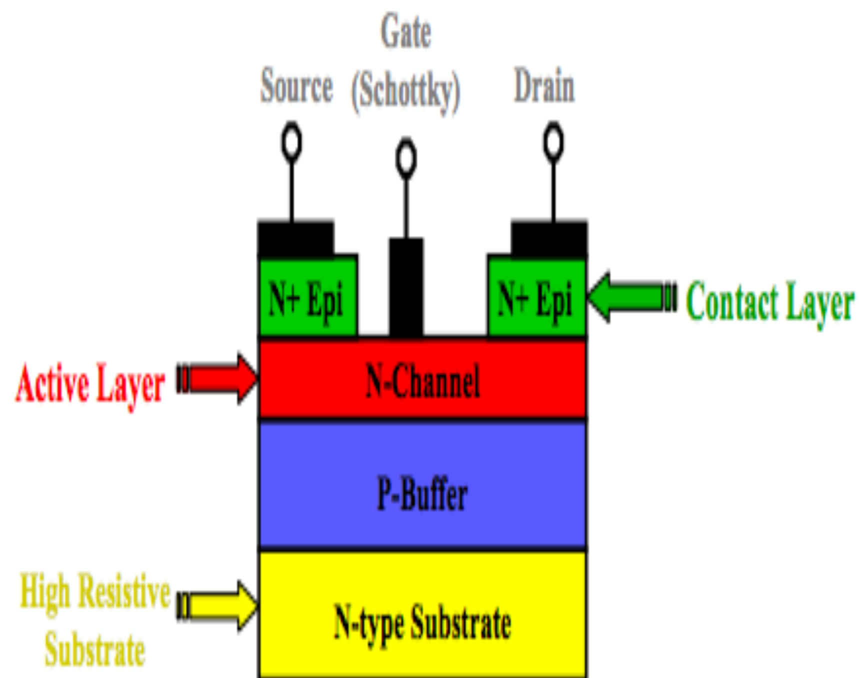

Figure 3.3 SiC MESFET Structure

3.2 SEMI-TRANSPARENT SIC SCHOTTKY DIODE:

The semi-transparent SiC Schottky diode has an "ultra-thin" (18 nm Ni/Ti) Schottky contact, a gold annular over layer and a gold corner-contact pad. The new architecture exhibits the same essential characteristics as a more conventional 'thick-contact' Schottky diode. Such diodes have a higher efficiency for low energy X-rays than that of conventional structures combined with minimal self-fluorescence from the electrode materials [51].

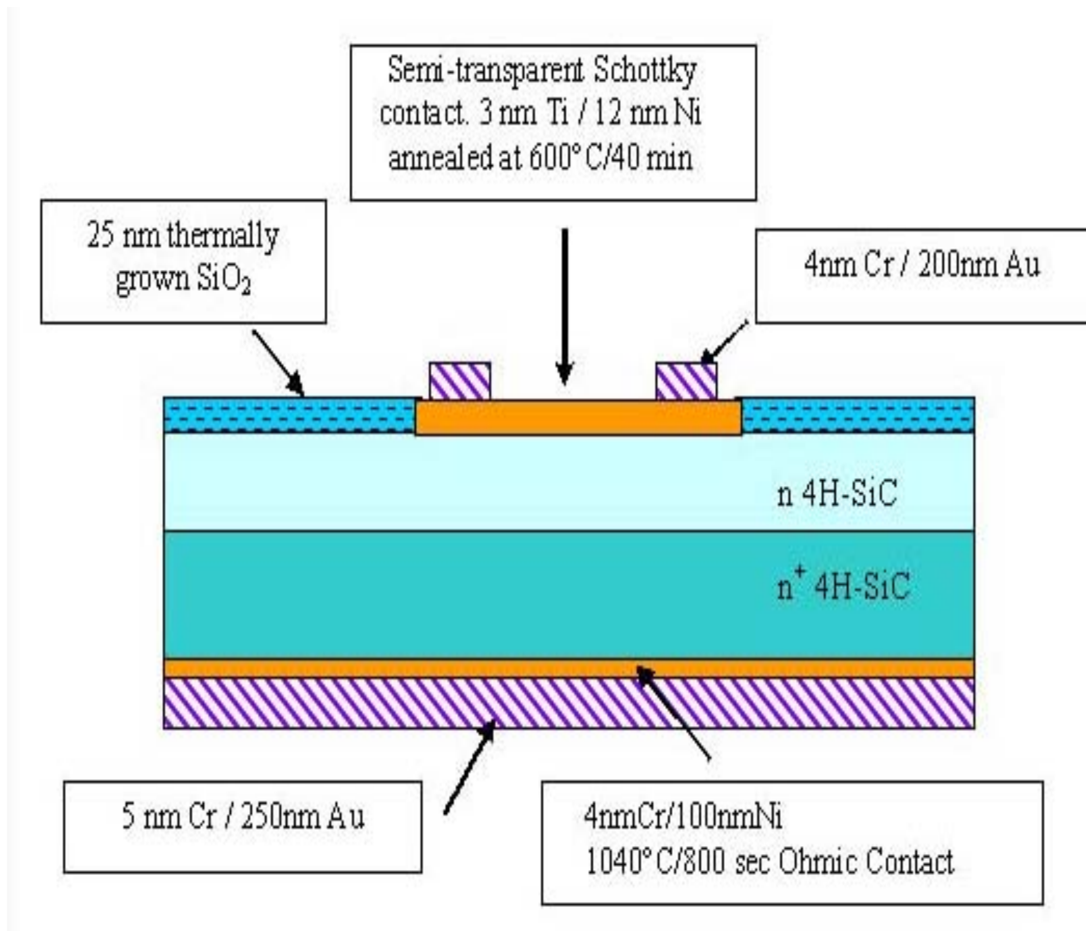

Figure 3.4 Section of 4H-SiC diode with semi transparent Schottky contact

3.3 ITO/N-GaAS SCHOTTKY PHOTO DIODES:

The use of an Schottky barrier photo diode has many advantages for very high-speed applications. In common with a conventional p-i-n detector, the absorption layer thickness can be engineered to obtain the optimum compromise between external

quantum efficiency and detector bandwidth. Figure 3.4 shows a section of 4H-SiC diode with semi transparent Schottky diode. An advantage however, is that there is no slow component associated with minority carrier effects in the p+ region of a p-i-n photo diode [52]. Planar Pt/n-GaAs Schottky diodes with 100 GHz bandwidth have been reported by Wang et al ; the metal thickness was only 100Å to allow for optocoupling. An inherent disadvantage of the Schottky photo diode, however, is the high series resistance and low efficiencies arising from the semi-transparent metal layer. This is apparent in the relatively low quantum efficiency of 19% and high series resistance of 190Ω obtained by Emeis et al in their p-InGaAs Schottky diodes (for operation at 1.3μm wavelength) with 50Å Ni semi-transparent metal contact [53]. Using a practically transparent and highly conductive layer of Indium Tin Oxide (ITO) to form the metal/semiconductor junction solves both these problems [54].

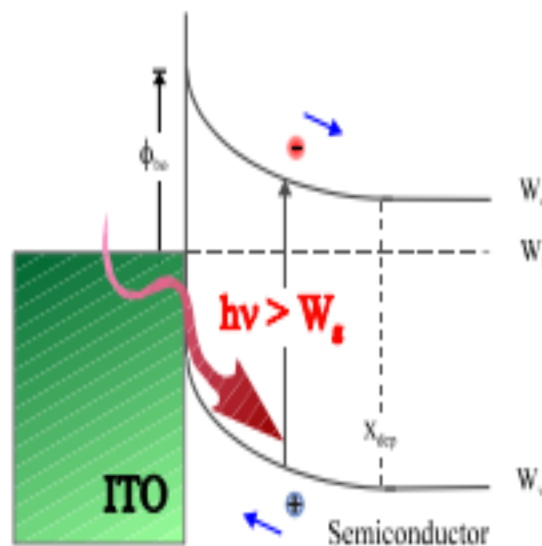

Figure 3.5 Band diagram of an ITO/n-GaAs Schottky photo diode

The absorption layer is usually lightly doped to maximize depletion and is situated directly underneath the metal contact. Light enters through the transparent ITO contact and creates photo generated electron-hole pairs. These are then swiftly separated by the built-in depletion field-giving rise to a photo current. Figure 3.5 shows the band diagram of an ITO/n-GaAs Schottky photo diode. The speed of response of such a device depends on the transit time of photo-generated carriers across the depletion

region, the junction capacitance and parasitic circuit element contribution. In a monolithic structure, device isolation, achieved by either proton bombardment or mesa etches or a combination of both reduces these parasitics. Furthermore, a planar structure is suitable for monolithic integration with other circuit elements such as HBTs or HEMTs [55].

3.4 DIODE FABRICATION:

3.4.1 Grown Junction Diode:

Diodes of this type are formed during the crystal pulling process. P and N-type impurities can be alternately added to the molten semiconductor material in the crucible, which results in a P-N junction. The larger area device then can be cut into a large number of smaller-area semiconductor diodes after slicing. The larger area also introduces more capacitive effects, which are undesirable. Such diodes are used for low frequencies [56].

3.4.2 Alloy Typed or Fused Junction Diode:

Placing a P-type impurity into the surface of an N-type crystal and heating the two until liquefaction occurs form an Alloy type or a Fused Junction diode. An alloy that will result on cooling will give a P-N junction at the boundary of the alloy substrate. Alloy type diodes have a high current rating and large PIV (Peak Inverse voltage) rating. The junction capacitance is also large, due to the large junction area. The figure 3.6 shows the alloy type or fused junction diode.

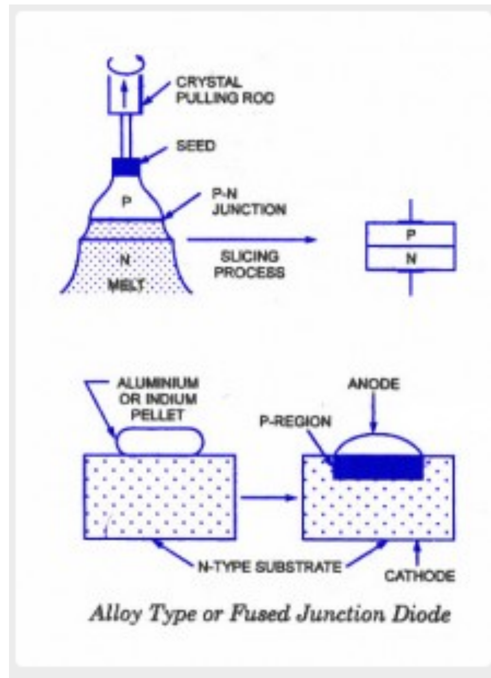

Figure 3.6 Alloy Type or Fused Junction Diode

3.4.3 Diffused Junction Diode:

Diffusion is a process by which a heavy concentration of particles diffuses into a surrounding region of lower concentration. The main difference between the diffusion and alloy process is that the liquefaction is not reached in the diffusion process. In the diffusion process heat is applied only to increase the activity of elements involved. The process of solid diffusion starts with the formation of layer of an acceptor impurity on an N-type substrate and heating the two until the impurity diffuses into the substrate to form the P-type layer. A large p-N junction is divided into parts by cutting process. Metallic contacts are made for connecting anode and cathode leads [56].

In the process of gaseous diffusion instead of layer formation of an acceptor impurity, an N-type substrate is placed in a gaseous atmosphere of acceptor impurities ad then heated. The impurity diffuses into the substrate to form P- type layer on the N-type substrate. Diffusion process requires more time than the alloy process but is relatively expensive, and can be very accurately controlled. The diffusion technique leads to the simultaneous fabrication of many hundreds of diodes on one small disc of semiconductor material and is most commonly used in the manufacture of

semiconductor diodes. Diffusion process is also used in the production of transistors and ICs(Integrated Circuits). Figure 3.7 shows Diffused Junction Diode.

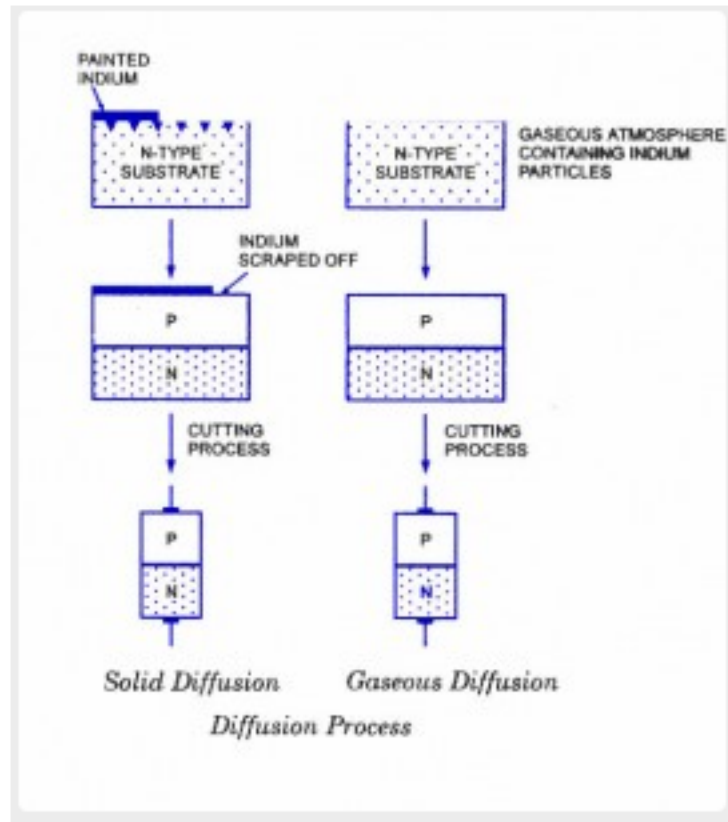

Figure 3.7 Diffusion Junction Diode

3.4.4 Epitaxial Growth or Planar Diffused Diode:

The term “epitaxial is derived from the Latin terms epi meaning ‘upon’ and taxis meaning ‘arrangement’. To construct an epitaxial grown diode, a very thin high impurity layer of semiconductor material is grown on a heavily doped substrate of the same material. This complete structure then forms the N-region on which P-region is diffused. SiO_2 layer is thermally grown on the top surface, photo-etched and then aluminium contact is made to the P-region. A metallic layer at the bottom of the substrate forms the cathode to which lead is attached. Epitaxial Growth is usually employed in fabrication of IC chips [57]. Figure 3.8 shows epitaxially grown or planar diffused diode.

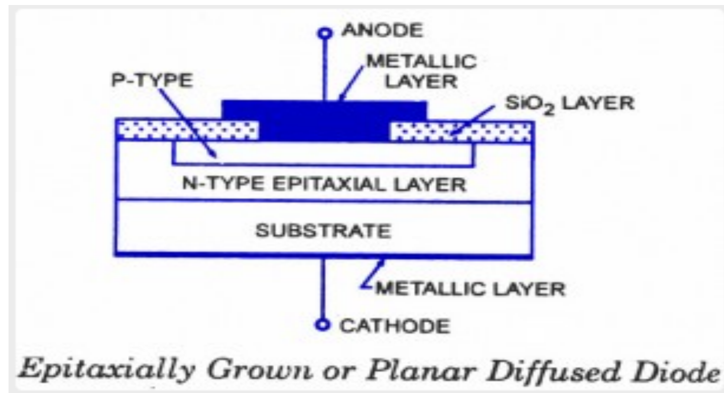

Figure 3.8 Epitaxially Grown or Planar diffused Diode

3.4.5 Point Contact Diode:

Point contact diode consists of an N-type germanium or silicon wafer about 12.5mm square by 0.5 mm thick, one face of which is soldered to a metal base by radio-frequency heating and the other face has a phosphor bronze pressed against it. Because of the small area of junction, point contact diode can be used to rectify only very small currents. The shunting capacitance of the point contact diodes is very valuable in equipment operating at super high frequencies (as high as 25,000 MHz). Figure 3.9 shows point contact diode.

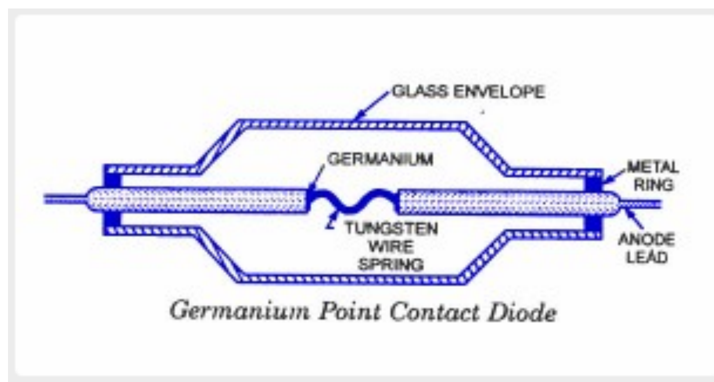

Figure 3.9 Point Contact Diode

CHAPTER 4
PARASITIC RESISTANCES

Parasitic resistances degrade the performance of both digital and analog/microwave FET's. Transconductance, power consumption, noise figure, and switching time are strongly affected by the parasitic series resistances. Accurate determination of the resistances is crucial for device and process characterization and modeling. Measurement of the series parasitic resistances is difficult requiring multiple measurements, accurate determination of parameters such as threshold voltage, built-in voltage and gate diode ideality factor. Reduction of analog circuit's areas is becoming a major issue of cost reduction because digital circuits are shrunk as device scaling precedes but analog circuits are not necessarily done. The estimation error of the parasitic resistances is one of the causes. The simulation does the accurate consideration of the parasitic resistances with the netlists including the parasitic resistances extracted by LPE (Layout Parameters Extraction) after layout design. Accurate models of the parasitic resistances for pre-layout design have not been proposed. It is impossible o construct accurate models, which consider all parasitic resistances and are applicable to arbitrary layout patterns conforming to design rules [58].

For the polycide resistor shown in figure 4.1, the parasitic resistance has been assumed to be in the inverse proportion to the expected number of the contacts in W-direction (nctw) or the expected total number of the contacts (nctw x nctl). The actual parasitic resistance decreases on the number of contacts in L-direction (nctl), and cause large errors. If the parasitic resistances of resistors cannot be accurately considered in pre-layout design, the errors must be added to the margins or some efforts to reduce the influences of the errors are needed. The inaccuracy of the parasitic resistances estimation enlarges the mismatch between resistors including the parasitic resistances and the linearity of the DAC degrades [59].

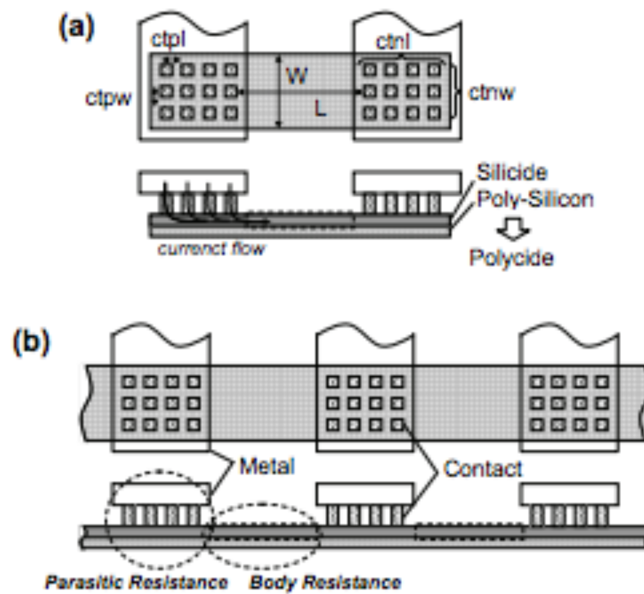

Figure 4.1 Layout and Cross sectional view of polycide resistor

4.1 TEST STRUCTURES FOR PARASITIC RESISTANCES:

The test structure to measure the parasitic resistance (R_s) of the resistors is shown in figure 4.2.The resistor used in analog circuits is connected to four pads by interconnects that diverge on the terminal of the resistor. W, L and nctl are variously changed. The body resistance and the parasitic resistance of the resistor not including the resistance of the system and the interconnect from the pads of the terminals can be obtained by the Kelvin method. The parasitic resistances are measured for a 40nm CMOS technology by using the test structures. Nctl larger than 4 doesn't reduce the parasitic resistance but increases circuit area [60].

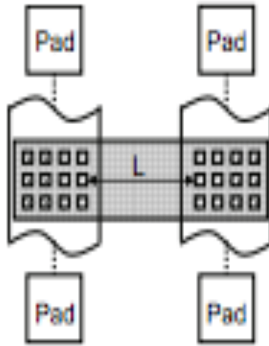

Figure 4.2 Test Structure for extraction of parasitic resistances

4.2 EXTRINSIC PARASITIC RESISTANCE:

The source, drain, substrate, and gate regions are made of resistive materials and present a series resistance at each terminal. Although in certain fabrication processes special techniques are used to lower series resistances, a general case is considered where the value of these resistances is not negligible. If the signals applied to a device are varying very fast, capacitance currents, which are of the form C dv/dt, can be large and can cause significant drops across these resistances. At very high frequencies, the effects of the resistances may not be negligible, in which case they should be included in the small signal model. The resistance of the source region is distributed along with the junction capacitance of that region.

The extrinsic resistances of the SiC MESFET are key parameters that affect the gain and the noise figure of the transistor. While several techniques for extracting the parasitic resistance have been reported, only a few have been published to extract the extrinsic resistances. The reported techniques make use of either dc or S-parameter measurements from which some relations between the unknown resistances are derived. Applying the technique introduced by Dambrine to calculate the extrinsic resistances for a single-gate FET using S-parameter measurements, only five independent equations can be derived for the DGFET. Carrier transportation, Source/Drain (S/D) electrostatic coupling, and parasitic resistance effects determine MESFET device performance [61].

4.3 MEASUREMENT OF PARASITIC RESISTANCES:

Shunt and series resistance are derived from the I-V characteristic at I_{SC} and V_{OC}. Figure 4.3 shows a simulated I-V curve of a 36 cell module with R_{sh} and R_s as determined from the slopes indicated, together with the simulation input values. A comparison of the different values shows that the resistances obtained from the slopes are not accurate. There are series methods that can be employed to calculate the parasitic resistance [62].

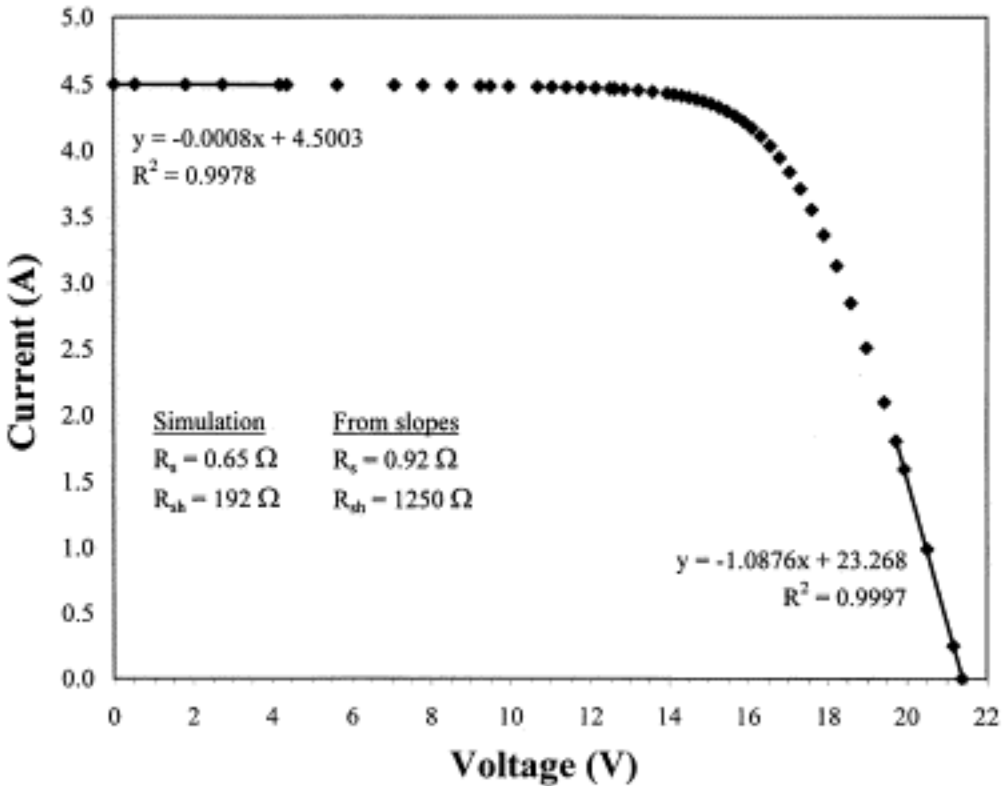

Figure 4.3 Simulated I-V characteristics of a crystalline silicon module

R_s can be determined by measuring I-V curves at different light intensities from a line drawn through points corresponding to a fixed current below the respective I_{SC} on each curve. R_s is then obtained from the slope of this curve, with $R_s = \Delta V / \Delta I$. Dark I-V measurements have been commonly used to evaluate the effect of series resistance and

other parameters on module performance. Non-linear parameter estimation software is used to fit to data measured in both low and high current regions. In addition to the estimated parameters, FitAll software also gives the absolute deviation for each parameter as well as the sensitivity of the estimation method to the various parameters. R_{sh} can also be derived from the slope of the reverse-biased I-V characteristic prior to junction breakdown. Figure 4.4 shows the measured dark I-V characteristics of 14W a – Si module before outdoor deployment. The solid line indicates the theoretical fit for the module. The standard deviation of the fit was of the order of 1.0×10^{-3}, indicating that the estimated parameters accurately describe the dark I–V characteristics of the a-Si:H module. From the measurements taken after out door exposure it was found that R_s, I_0 and n increased with the outdoor exposure, while R_{sh} remained relative constant throughout the test period. The increase in saturation current from 5.7 nA before outdoor exposure to 27.5 μA after 130 kWh/m^2, indicates an increase in the recombination current, I_D. This increase in recombination current is attributed to an increase in the density of defect states in the energy bandgap. These defects are formed by energy released from recombination of e–h pairs. Therefore, as electrons and holes recombine, weak Si–H or Si–Si bonds are broken by the energy released. These broken bonds form defect states, creating more recombination sites. The increase in recombination sites, in turn, enhances the recombination of e–h pairs. The formation of defect states in the bandgap reduces the carrier lifetime. This results in deterioration of the p–n junction quality. Fortunately, this effect is self-limiting since there are only so many weak bonds to break. The increase in saturation current and hence the deterioration of the p–n junction quality is associated with a decrease in performance of the a-Si module [62].

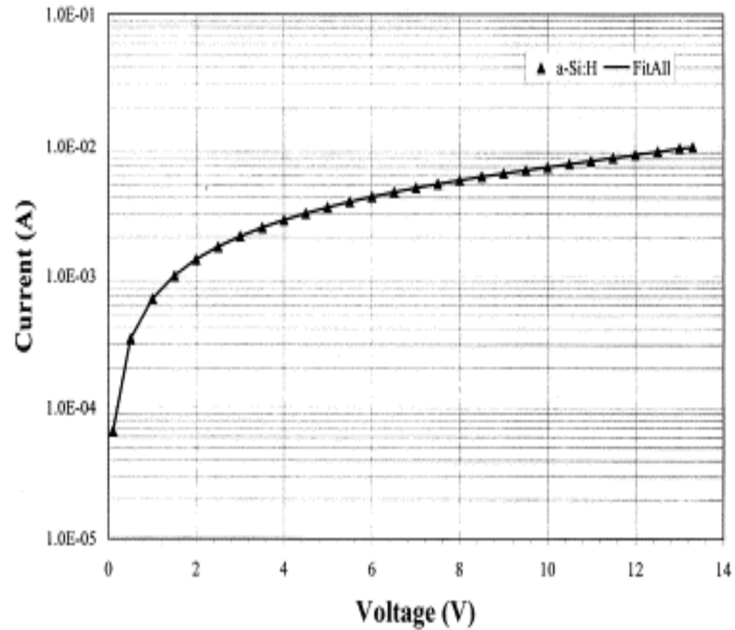

Figure 4.4 Dark I-V characteristics of an a-Si module before outdoor exposure

The knowledge of the parasitic resistances is needed in most parameter extraction methods of SiC MESFET's. Accurate and fast parameter extraction is important when designing and developing microwave circuits. Transconductance, noise figure and power consumption are strongly affected by the parasitic resistances. There are several approaches proposed for the extraction of parasitic resistances, most of them are based on a combination of DC and small-signal parameters measured under certain special bias point. For wafer probing, a fast and reproducible technique of determining the parasitic resistances is desirable. The method used in this paper to determine the parasitic resistances uses only three DC measurements from which three relations between the drain, source and gate resistances R_D, R_S, R_G are obtained. The parasitic resistances are calculated analytically from the three equations. The numerical iterations are avoided and the extraction of the parasitic resistances becomes faster and more reliable. The measured voltages are further processed to reduce the measurement noise and to obtain reliable results of the parasitic resistances [63].

The non-linear Statz MESFET model, available in most commercial circuit simulators is shown in Figure 4.5. This model has three dominant non-linearities: the transconductance I_{ds}, the gate –source capacitance C_{gs} , and the gate drain capacitance

C_{gd} ,which are expressed in terms of the intrinsic gate to source and drain to source voltage.

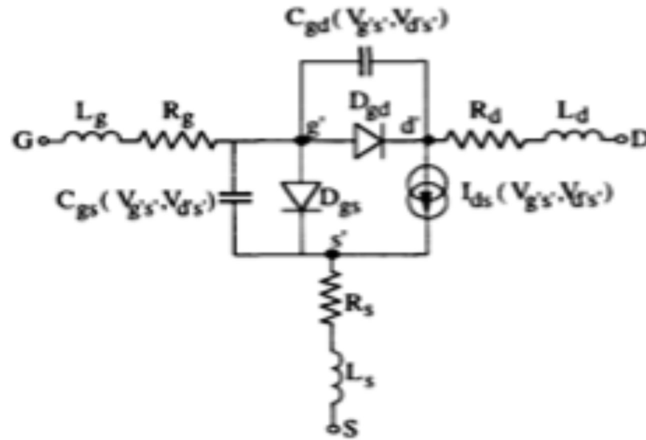

Figure 4.5 Non linear Statz MESFET Model

The DC equivalent circuit model of the SiC MESFET shown in the Figure 4.6 is derived from the nonlinear Statz Model. The model includes the parasitic resistances R_G, R_S and R_D, the diodes D_{GD} and D_{GS} representing the gate-channel Schottky junction and the channel resistance R_{CH}. Before the parasitic resistances are calculated, the junction saturation current I_S and the ideality factor N of the Schottky diodes is determined. Since the model does not have the transconductance, it only applies to cold-FET (V_{ds} = 0V) operation. The diodes in the model are assumed to be identical and are modeled by the Shockley equation.

$I = I_{sat}\,[\exp(V/n.Vt)-1]$ 4(a)

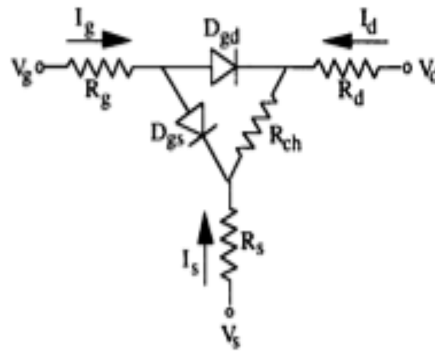

Figure 4.6 DC equivalent circuit model for a SiC MESFET

The reverse saturation current I_{sat} and the ideality factor n can be accurately determined from a forward diode measurement. Vt is the thermal voltage kT/q, which is 26mV at room temperature.

The first measurement setup is shown in Figure 4.7, where a current I_g is forced through the gate while the intrinsic drain to source voltage is forced to zero by a second current source of $I_g/2$ at the drain. No current flows through the channel resistance, so R_{ch} can be neglected. The voltage at the drain is proportional to the difference between the source and drain resistance.

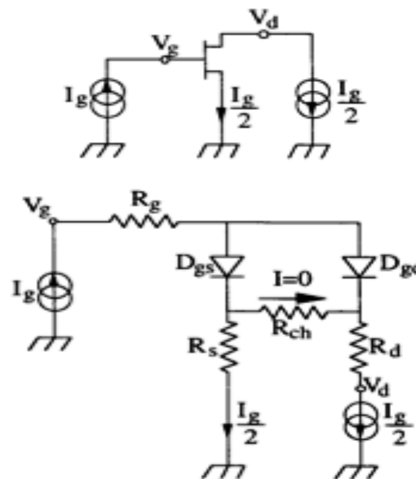

Figure 4.7 First DC measurement setup

The following relations are obtained from the voltages measured at the drain and the gate, and using the Kirchhoff's voltage law.

$R_d + 2V_d / I_g = R_s$

4(b)

$R_g + R_s/2 = (V_g\text{-}n.V_t.\ln(1+(Ig/2.I_{sat})))/I_g$

4(c)

In the low current region of this measurement, where the voltage drop across the parasitic resistances can be neglected, the diode ideality factor n, and the reverse saturation current I_{sat} can be extracted [64].

The second measurement setup is shown in Figure 4.8, where the current I_g is forced through the gate with the drain left open and the source connected to ground, so $I_s = -I_g$. The voltages at the drain and the gate are measured. The currents through the two Schottky diodes are given by

$I_1 = I_{sat}.\{\exp[(V_g\text{-}(R_s+R_g).\ Ig)/n.\ Vt)]\text{-}1\}$

4(d)

$I_2 = I_{sat}.\{\exp[(V_g\text{-}R_g.I_g\text{-}V_d)/n.\ Vt]\text{-}1\}$

4(e)

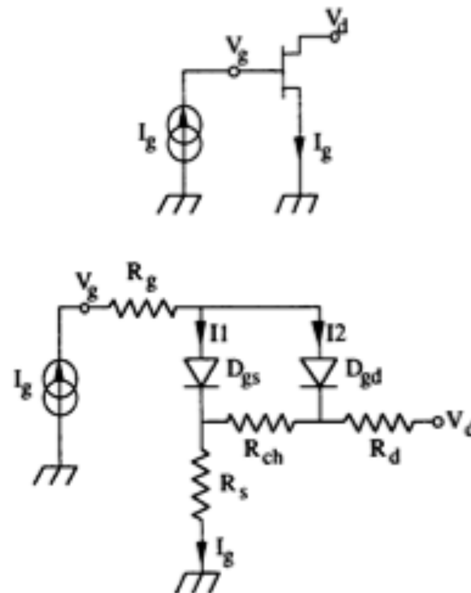

Figure 4.8 Second DC measurement setup

$I_g = I_1 + I_2$, hence the above equations can be solved to obtain the relation between R_s and R_g.

$R_s+R_g=[V_g-n.V_t.\ln\{(2+(I_g/I_{sat})[1+\exp(R_{s.}I_g-V_d)/n.Vt)]-1\}]/I_g$
4(f)

The non-linear equations can be solved to determine the values of R_s, Rd, and R_g. To get a first approximation of $R_s+R_{g,}$ Rs is set to zero in the right hand side of the equation and the new value of Rs is used to get the new approximation for R_s+R_g. This concludes the first iteration loop after which the second loop starts. The iteration process is terminated when the difference between a new and a previous value of Rs is smaller than a predefined value. The solution of these equations converges after a few iteration cycles.

SiC MESFET has become very promising for high microwave in the commercial and military applications due to its superior properties and the relatively mature device fabrication technology, such as wide band gap (3.26 eV), high breakdown field (3MV/cm), large thermal conductivity (3.5W/cm.K) and high electron saturation velocity ($2x10^7$cm/s). To achieve high output power density, 4H-SiC MESFET must sustain large saturated drain current and support high breakdown voltages [65].

CHAPTER 5
RESULTS AND DISCUSSIONS

The parasitic parameters are important to develop the MESFET device for high frequency performance and high-speed response. The extrinsic parasitic components are generated from contact resistance; ohmic contact and source drain spacing. Therefore the following study has been presented to extract the extrinsic parasitic parameters. The three values of parasitic resistances R_S, R_G and R_D are calculated and the graphs are plotted. The parasitic resistance R_S is calculated from the below equation 5(a).

$$R_S=(2nV_t/I_G)\ln(0.5W_3-0.5\sqrt{(W_3^2-4W_3)})+nV_tW_2/I_G \quad 5(a)$$

Where

$$W_2 = [2(V_{G2}-V_{G1})/nV_t]+2\ln0.5$$

5.1(a)

$$W_3 = \exp[(V_{D2}/nV_t)-W_2]$$

5.2(a)

R_S is the parasitic resistance of source.

Parasitic resistances R_D and R_G are calculated analytically from the two equations 5(b) and 5(c)

$$R_D + (2V_{D1}/I_{G1}) = R_S$$

5(b)

$$(R_S/2)+R_G=[V_{G1}-nV_T(1+(I_{G1}/2I_S))]/I_{G1}$$

5(c)

R_D is the parasitic resistance of drain.

R_G is the parasitic resistance of gate.

n is the ideality factor of SiC, which is in the order of 1.5.

V_t is the thermal voltage, which is 26mV.

I_G is the gate current when the intrinsic drain to source voltage is forced to zero.

I_S is the saturation current which is the order of 10^{-12} for SiC

V_{G2} is the gate voltage from the second measurement

V_{G1} is the gate voltage from the first measurement

V_{D1} is drain voltage from the first measurement

V_{D2} is the drain voltage from the second measurement

W_2 andW_3 are the parts in the equation 5(a)

The values of W_2 andW_3 are calculated from the equations 5.1(a) and 5.2(a).

5.1 Plot of Drain voltage V_D versus Source Resistance R_S varying Gate Voltage V_G:

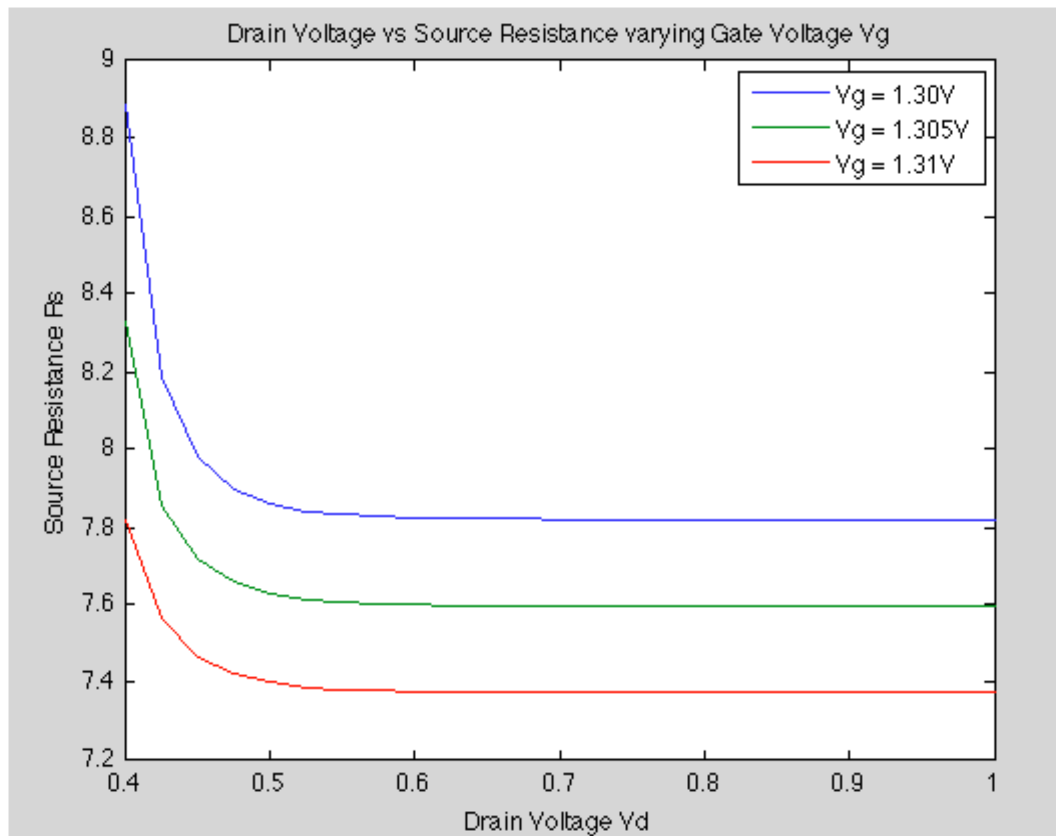

Figure 5.1 V_D versus R_S varying V_G

The Figure 5.1 shows a plot of drain voltage V_D versus source resistance R_s for different gate Voltage V_G of 1.30V, 1.305V and 1.31V and this plot has been drawn by using the equation 5(a). The source resistances exponentially decrease between the

drain voltages from 0.4 to 0.5V, whereas the source resistance becomes saturated beyond 0.6V to 1V for different gate voltage. The knee source resistance between the drain voltage of 0.4V and 0.5V is a clear evident of change of transconductance; the device can behave the linearity and non-linearity due to drain bias change.

5.2 Plot of Drain voltage V_D versus Drain Resistance R_D varying Gate Voltage V_G:

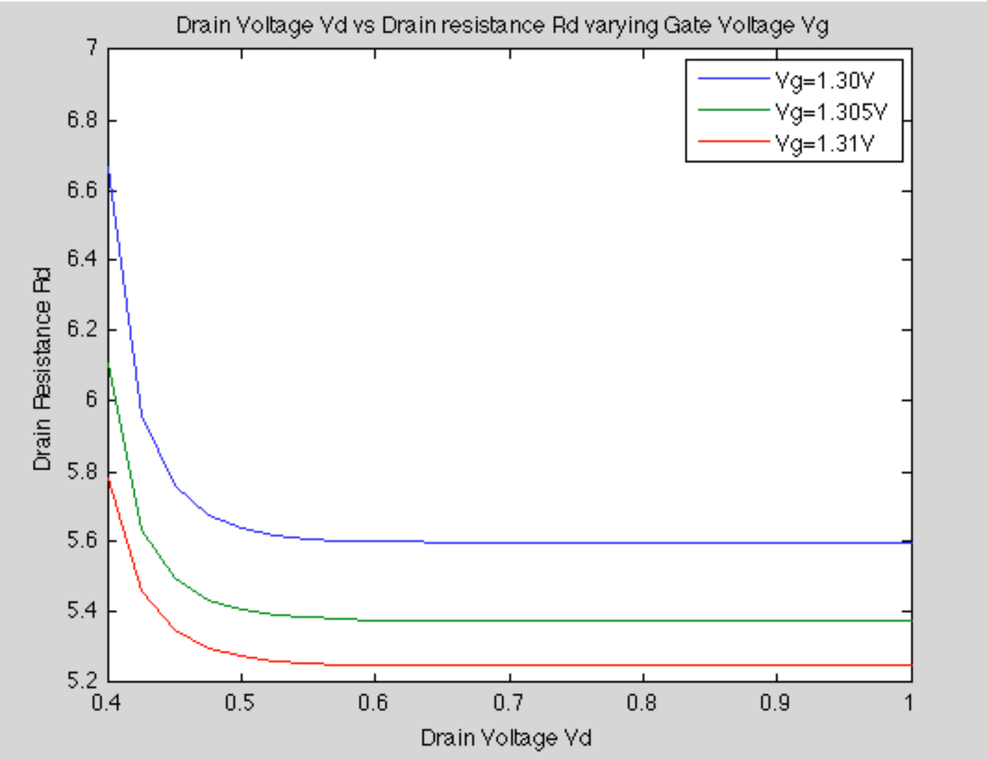

Figure 5.2 V_D versus R_D varying V_G

The Figure 5.2 shows a plot of drain voltage V_D versus Drain Resistance R_D for different gate Voltage V_G of 1.30V, 1.305V and 1.31V and this plot has been extracted from the equation 5(b). The drain resistances have similar nature of exponential decay

between the drain voltages from 0.4 to 0.5V, whereas the source resistance becomes constant beyond 0.6V to 1V for different gate voltage. The knee source resistance between the drain voltage of 0.4V and 0.5V is a clear evident of change of transconductance; hence the device behavior shows the property of linearity and non-linearity due to drain bias change. The extrinsic parameters R_S and R_D show the symmetrical properties with the change of drain voltage for different gate biasing.

5.3 Plot of Drain voltage V_D versus Gate Resistance R_G varying Gate Voltage V_G:

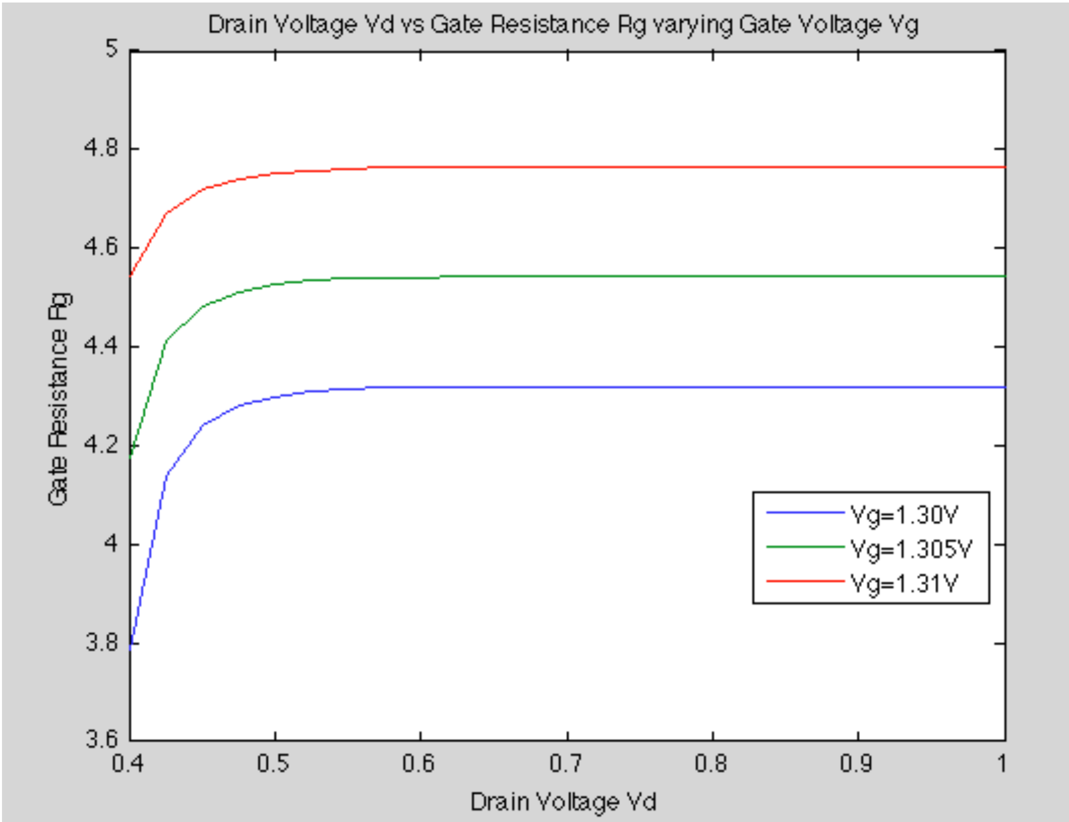

Figure 5.3 V_D versus R_G varying V_G

The figure 5.3 presents a plot of gate resistance R_G versus drain voltage V_D for different gate voltage of 1.30V, 1.305V and 1.31V and the plot has been obtained by using the equation 5(c). The gate resistance R_G exponentially increases at the drain voltage of 0.4 -0.5V for gate voltages of 1.30V, 1.305V and 1.31V and the gate

resistance value reaches to steady state constant value from 0.55V to 1.0V for same gate voltages. The gate resistances increase from the drain voltage from 0.4V to 0.5V, because of the excess carrier generation. The gate resistances become saturation, when the excess carriers reach to steady state value.

CHAPTER 6
CONCLUSION

A new and accurate method is presented in the paper for extracting the parasitic resistance values of SiC MESFET's. The suggested method makes use of only three simple DC measurements, with the intrinsic drain to source voltage set to zero. The advantage of this method is it is not necessary to either calculate or neglect the channel resistance. The simulation results show better correspondence between the original and the extracted parameter values. The extrinsic resistances affect the frequency and the performance of the device; hence by calculating the parasitic resistances the performance of the device can be improved.

This method does not make use of an optimization technique to extract the parameters, so it is fast and the extracted values are more relevant. Graphs are plotted for the extracted values of parasitic resistances of source, drain and gate versus the drain voltage for different gate voltages. The parasitic resistance plays an important role to determine the high frequency response and high switching performance. This study shows an important avenue to develop a MESFET with high frequency and high speed switching performance.

REFERENCES

[1] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, "Conductivity anisotropy in epitaxial 6H and 4H SiC," in Diamond, Sic, and Nitride Wide Bandgap Semiconductors, C.H. Carter, Jr., G. Gildenblatt, S. Nakamura, and R.J. Nemanich, Eds., Material Research Society Proc., vol. 339. Pittsburgh, PA: MRS, 1994, pp. 595-600.

[2] Baliga, B.J., "Power Semiconductor Devices for Variable-Frequency Drives," Proceedings of the IEEE 82(8), 1112, 1994.

[3] Elasser, A. and Chow, T.P., "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," Proceedings of the IEEE 90(6), 969, 2002.

[4] Johnson, C.M., "Clear road ahead?" Power Engineer 18(4), 34, 2004.

[5] J.S.Sullivan and J.R. Stanley, "6H-SiC Photoconductive Switches Triggered at Below
Band gap Wavelengths".

[6] C. Baak, et.al "GaAs MESFET: A high speed optical detector," Electron Lett., vol 13,
p.139, 1977.

[7] J. Graffeuil, P. Rossel and H.Marinot, Electron Lett.,vol 15.p.439, 1979.

[8] J. L. Gautier, D. Pasquet and P. Pouvil, "Optical effects on the static and dynamic characteristics of a GaAs MESFET," IEEE Trans. MTT, vol. Mtt-33, pp.819-822, 1985.

[9] H. Mizuno, "Microwave characteristics of an optically-controlled GaAs MESFET," IEEE MTT, vol. MTT-31, pp.596-600, 1983

[10] S. Mishra, V. K. Singh, and B. B. Pal, "Effect of radiation and surface recombination on the characteristics of an implanted GaAs MESFET," IEEE Trans. Electron Devices, vol. 37, pp. 2–10, Jan. 1990.

[11] J. Graffeuil, P. Rossel, and H. Martinot, "Light induced effects in GaAs FET's," Electron. Lett. vol. 15, no. 14, pp. 439–441, July 1979.

[12] R. N. Simon and K. B. Bhasin, "Analysis of optically-controlled microwave/millimeter wave device structures," IEEE Trans. Microwave Theory Tech., vol. MTT-34, pp. 1349–1355, Dec. 1986.

[13] S. N. Mohammad, M. S. Unlu, and H. Morkoc, “Optically-controlled current–voltage Characteristics of ion-implanted MESFET’s,” Solid-State Electron., vol. 33, no. 12, pp. 1499–1509, 1990.

[14] J. Pan, “GaAs MESFET for high speed optical detection,” in SPIE Int. Tech. Symp., San Diego, CA, 1978.

[15] W. D. Edwards, “Two and three terminal gallium arsenide FET optical detectors,” IEEE Electron Device Lett, vol. EDL-1, pp. 149–150, Aug. 1980.

[16] A. A. De Salles, “Optical control of GaAs MESFET’s,” IEEE Trans. Microwave Theory Tech., vol. MTT-31, pp. 812-820, 1983.

[17] B.B. Pal and S.N. Chattopadhyay. "GaAs OPFET characteristics considering the effect of gate depletion width modulation due to incident radiation", IEEE Trans. On Electron Devices, Vol.ED-39, pp.1021-1027, 1992.

[18] R. N. Simons and K. B. Bhasin, “Analysis of Optically controlled microwave/ millimeter-wave device structures,” IEEE Trans Microwave Theory Tech, vol.34, no.12, pp.1349-1355, December 1986.

[19] Giovanni Breglio, et.al. “Two silicon optical modulators realizable with a fully compatible bipolar process,” JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCEVOL.7, NO.3, SEPTEMBER, 2007 207 IEEE Journal of selected topics in Quantum Electronics, vol.4, pp. 1003-1010, 1998.

[20] Kei Kanemoto, et. al., “Dependence of ion implantation: Induced defects osubstratedoping,” J. Appl. Phys. 89, pp.3156-3161, 2001.

[21] De Salles, “$Al_{0.3}Ga_{0.7}As$/GaAs HEMT's under optical illumination”.

[22] J. Graffeuil, P. Rossel, and H. Martinot, “Light-induced effects in GaAs F.E.T.s,” Electron Lett. vol. 15, no. 14, pp. 439-441, July 1979.

[23] J. Pan, “GaAs MESFET for high speed optical detection,” in SPIE Int. Tech. Symp. (San Diego, CA), 1978.

[24] Weimer, A. W. (1997).Carbide,nitride, and boride materials synthesis and processing. Springer. p. 115.ISBN 0412540606.

[25] Mabery, Charles F. (1900). "Notes, On Carborundum".Journal of the American Chemical Society (Johnson Reprint Company, via Google Books scan of Harvard University copy)XXII (Part II): 706–707. Retrieved 2007-10-28.

[26] Dunwoody, Henry H.C. (1906) U.S. Patent 837,616"Wireless telegraph system" (silicon carbide detector)

[27] Hart, Jeffrey A.; Stefanie Ann Lenway, Thomas Murtha. "A History of Electroluminescent Displays".
[28] Moissan, Henri (1904). "Nouvelles recherches sur la météorité de Cañon Diablo". Comptes rendus 139: 773–86.
[29] Di Pierro S., Gnos E., Grobety B.H., Armbruster T., Bernasconi S.M., and Ulmer P.2003). "Rock-forming moissanite (natural α-silicon carbide)". American Mineralogist 88: 1817–21.
[30] Alexander, C. M. O'D. (1990). "In situ measurement of interstellar silicon carbide in two CM chondrite meteorites".Nature 348: 715–17. doi:10.1038/348715a0.
[31] Harris, Gary Lynn (1995). Properties of silicon carbide. IET. p. 19; 170–180. ISBN0852968701.
[32] Lely, Jan Anthony (1955). "Darstellung von Einkristallen von Silicium Carbid und Beherrschung von Art und Menge der eingebauten Verunreinigungen". Berichte der Deutschen Keramischen Gesellschaft 32: 229–236.
[33] N.Ohtani, T.Fujimoto, T.Aigo, M.Katsuno, H.Tsuge, H.Yashiro (2001). Nippon Steel Technical Report no. 84 : Large high-quality silicon carbide substrates.
[34] Byrappa, K.; Ohachi, T. (2003). Crystal growth technology. Springer. pp. 180–200. ISBN 3540003673.
[35] Pitcher, M. W.; Joray, S. J; Bianconi, P. A. (2004). "Smooth Continuous Films of Stoichiometric Silicon Carbide from Poly(methylsilyne)". Advanced Materials 16: 706.doi:10.1002/adma.200306467.
[36] Park, Yoon-Soo et al. (1998). SiC materials and devices. Academic Press. pp. 20–60. ISBN 0127521607.
[37] Laine, Richard M.; Babonneau, Florence (1993). "Preceramic polymer routes to silicon carbide". Chemistry of Materials 5: 260. doi:10.1021/cm00027a007.
[38] Cheung, Rebecca (2006). Silicon carbide microelectromechanical systems for harsh environments. Imperial College Press. p. 3. ISBN 1860946240.

[39] Morkoç, H.; Strite, S.; Gao, G. B.; Lin, M. E.; Sverdlov, B.; Burns, M. (1994). "Large-bandgap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies". Journal of Applied Physics 76: 1363. doi:10.1063/1.358463.

[40] Muranaka, T. et al. (2008). "Superconductivity in carrier-doped silicon carbide" (free
download). Sci.Technol.Adv.Mater. 9:044204. doi:10.1088/14686996/9/4/044204

[41] Bhatnagar, M.; Baliga, B.J. (March 1993). "Comparison of 6H-SiC, 3C-SiC, and Si for power devices". IEEE Transactions on Electron Devices 40 (3): 645–655.

[42] Rost H J, Dolle J, Doerschel J, Siche D, Schulz D and Wollweber 2000 Mater. Sci. Forum 353–356 29

[43] Li H Q, Chen X L, Ni D Q and Wu X 2003 J. Cryst. Growth 258 100

[44] Lepkowski, W.; Wilk, S.J.; Thornton, T.J. (2009), "45 GHz Silicon MESFETs on a 0.15 μm SOI CMOS Process", SOI Conference, 2009 IEEE International (Foster City, CA): 1–2, ISBN 978-1-4244-4256-0, ISSN 1078-621X

[45] H. Henry, G Augustine, G DeSalvo, R. B. R. C. Brooks, J. Oliver,A. Morse, B. Veasel, P. Esker, and R. Clarke, "S-band operation of SiC power MESFET with 20 W (4.4 W/mm) output power and 60% PAE,"IEEE Trans. Electron Devices, vol. 51, no. 6, pp.839-845,Jun.2004.

[46] H.-Y. Cha, C. I. Thomas, G Koley, L. F. Eastman, and M. G Spencer,"Reduced trapping effects and improved electrical performance in buried gate 4H-SiC MESFETs," IEEE Trans. Electron Devices, vol. 50, no. 7,pp. 1569-1574, Jul. 2003.

[47] Kristoffer Andersson, Mattias Siidow, Per-Ake Nilsson, Einar Sveinbjornsson, and Hans Hjelmgren, "Fabrication and Characterization of Field-Plated Buried-Gate SiC MESFETs" IEEE

Si by capacitance spectroscopy methods. Sov. Phys. Semicond. 19 (1985) 69

[48] Hagen, S.H., Kapteyns, C.J. Philips Res. Repts. 25 (1970) 1.D.W., Parker, J.H., Choyke, W.J., Patrick, L. Phonon Dispersion Curves by Raman Scattering in Si, Polytypes 3C, 4H, 6H, 15R, and 21R. Phys. Rev. 173, 3 (1968) 787.

[49] Hemstreet, L.A., Fong, C.Y. Silicon - 1973, Eds. Marshall, R.C., Faust, J.W., Ryan, C.E., Univ. of South Carolina Press, Columbia, S.C. 1974, 284.

[50] N. Emeis, H. Schumacher and H. Beneking, "High Speed GaInAs Schottky Photodetector", Electronics Letters, 21(5), 1985, pp. 180 – 181.

[51] CREE Research Inc., 4600 Silicon Dive, Durham, NC 27703, USA.

[52] Temcamani F, Pouvil P, Noblanc O, Brylinski C, Bannelier P, Darges B and Prigent J P, "Silicon carbide MESFETs performances and application in broadcast power amplifiers" *lEEE Trans. Electron Devices,* MTT-S Int. Microwave Symposium Digest, vol. 2, pp. 641-4, 2001.

[53] Allen S T, Pribble W L, Sadler R A, Alcorn T S, Ring Z and Palmou J W,"Progress in high power SiC microwave MESFETs" *lEEE Trans. Electron Devices,* MTT-S Int. Microwave Symposium Digest vol. 2, pp. 321-4, 1999.

[54] Villard F, Prigent J-P, Morvan E, DuaC,Brylinski C, Temcamani F and Pouvil P, "Trap-free process and thermal limitations on large-periphery SiC MESFET for RF and microwave power", *lEEE Trans. Electron Devices,* Microw.Theory Tech. vol. 51, pp. 1129-34, 2003.

[55] Y. Taur, et.al, IEDM Technical Digest, p.789, 1998

[56] S.Thompson, et.al, Symp. VLSI Tech. Dig., p.132, 1998

[57] B.Y Tusi, et.al, IEEE TED vol 40, No.1, p197, 1993

[58] International Technology Roadmap for Semiconductor, 2001 edition

[59] SILVACO international, Santa Clara, CA 94054, USA

[60] D.J.Frank et al, IEDM Tech. Dig., p553, 1992

[61] B.Yu, et al, IEDM Tech. Digest, p348, 1999

[62] C.Park, et al, Symp. VLSI Tech. Dig., p.69, 2001

[63] E.0. Johnson,"Physical limitations on frequency and power parameters of transistors," RCA Rev., vol. 26, pp. 163-177, 1963.

[64] D. Alok, B. J. Baliga, and P. K. McLarty, "A simple edge termination or siliconcarbide devices with nearly ideal breakdown voltage," IEEE Electron Device Lett. Vol. 1.5, no. 10, p. 394-395, 1994.

[65] C.E. Weitzel, "Wide Bandgap Semiconductor RF MESFET Power Densities," Technical Digest of International Conference on Silicon Carbide and Related Materials, Kyoto, Japan, September, 1995, pp. 3 17-3 18.

APPENDIX-A

k	Boltzmann constant
T	Absolute temperature at 300K
V_{bi}	Built-in voltage of active channel and substrate junction
I_{sat}	Saturation Current
I_g	Gate current
R_S	Source parasitic resistance
R_D	Drain parasitic resistance
R_G	Gate parasitic resistance
n	Ideality factor
V_t	Thermal voltage
V_{G2}	Gate voltage from the second measurement
V_{G1}	Gate voltage from the first measurement
V_{D1}	Drain voltage from the first measurement
V_{D2}	Drain voltage from the second measurement

APPENDIX-B

%Matlab Code for V_D versus R_S varying V_G

```
n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs1 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.30;
Vg2 = 1.503;
Isat = 10^(-12);
%Parameters
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs1(k) = (2*T*log(R))+(T*W2);
Rd = Rs1-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
```

```
Rg = ((Vg1-(n*Vt*Z))/(Ig))-(Rs1/2);
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs1);
display(Rd);
display(Rg);
 end
 n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs2 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.305;
Vg2 = 1.503;
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
```

```
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs2(k) = (2*T*log(R))+(T*W2);
Rd = Rs2-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg = ((Vg1-(n*Vt*Z))/(Ig))-(Rs2/2);
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs2);
display(Rd);
display(Rg);
end
 n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs3 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.31;
Vg2 = 1.503;
```

```
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs3(k) = (2*T*log(R))+(T*W2);
Rd = Rs3-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg = ((Vg1-(n*Vt*Z))/(Ig))-(Rs3/2);
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs3);
display(Rd);
display(Rg);
end
plot(Vd2,Rs1,Vd2,Rs2,Vd2,Rs3);
title(' Drain Voltage vs Source Resistance varying Gate Voltage Vg');
xlabel('Drain Voltage Vd');
```

```
ylabel('Source Resistance Rs');
```

%Matlab Code for V_D versus R_D varying V_G

```
n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs1 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65) (0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95) (0.975) (1.0)];
Vg1 = 1.30;
Vg2 = 1.503;
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs1(k) = (2*T*log(R))+(T*W2);
Rd1 = Rs1-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
```

```
Rg = ((Vg1-(n*Vt*Z))/(Ig))-(Rs1/2);
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs1);
display(Rd1);
display(Rg);
 end
n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs2 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.305;
Vg2 = 1.503;
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
```

```
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs2(k) = (2*T*log(R))+(T*W2);
Rd2 = Rs2-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg = ((Vg1-(n*Vt*Z))/(Ig))-(Rs2/2);
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs2);
display(Rd1);
display(Rg);
end
n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs3 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.3079;
Vg2 = 1.503;
```

```
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs3(k) = (2*T*log(R))+(T*W2);
Rd3 = Rs3-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg = ((Vg1-(n*Vt*Z))/(Ig))-(Rs3/2);
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs3);
display(Rd3);
display(Rg);
end
plot(Vd2,Rd1,Vd2,Rd2,Vd2,Rd3);
title('Drain Voltage Vd vs Drain resistance Rd varying Gate Voltage Vg ')
ylabel('Drain Resistance Rd')
```

```
xlabel('Drain Voltage Vd')
```

%Matlab Code for V_D versus R_G varying V_G

```
n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs1 = zeros(1,4);
for k = 1:4;
Vd2 = [(0.4) (0.5) (0.6) (0.7)];
Vg1 = 1.30;
Vg2 = 1.503;
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs1(k) = (2*T*log(R))+(T*W2);
Rd = Rs1-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg1 = ((Vg1-(n*Vt*Z))/(Ig))-(Rs1/2);
%displaying the results
display(A);
```

```
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs1);
display(Rd);
display(Rg1);
end
n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs2 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.305;
Vg2 = 1.503;
Isat = 10^(-12);
%Parameters
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
```

```
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs2(k) = (2*T*log(R))+(T*W2);
Rd = Rs2-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg2 = ((Vg1-(n*Vt*Z))/(Ig))-(Rs2/2);
%displaying the results
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs1);
display(Rd);
display(Rg2);
 end
 n = 1.5;
Vt = 26*10^(-3);
Ig = 45*10^(-3);
Vd1 = 0.05;
Rs3 = zeros(1,25);
for k = 1:25;
Vd2 = [(0.4) (0.425) (0.45) (0.475) (0.5) (0.525) (0.55) (0.575) (0.6) (0.625) (0.65)
(0.675) (0.7) (0.725) (0.75) (0.775) (0.8) (0.825) (0.85) (0.875) (0.9) (0.925) (0.95)
(0.975) (1.0)];
Vg1 = 1.31;
Vg2 = 1.503;
```

```
Isat = 10^(-12);
A = (Vg2-Vg1)/(n*Vt);
X = 0.5;
B = log(X);
W2 = (2*A)+(2*B);
C = (Vd2(k)/(n*Vt))-W2;
W3 = exp(C);
P = W3^(2)-(4*W3);
Q = sqrt(P);
R = (0.5*W3)-(0.5*Q);
S = log(R);
T = ((n*Vt)/Ig);
Rs3(k) = (2*T*log(R))+(T*W2);
Rd = Rs3-(2*(Vd1/Ig));
V = 1+(Ig/(2*Isat));
Z = log(V);
Rg3 = ((Vg1-(n*Vt*Z))/(Ig))-(Rs3/2);
% displaying the results
display(A);
display(B);
display(C);
display(R);
display(T);
display(W2);
display(W3);
display(Rs3);
display(Rd);
display(Rg3);
end
plot(Vd2,Rg1);
title(' Drain Voltage Vd vs Gate Resistance Rg varying Gate Voltage Vg')
```

```
ylabel('Gate Resistance Rg')
xlabel('Drain Voltage Vd)
```