CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

VIRTEX 4 LX200 AUTOMATED TEMPERATURE STRESS TEST

SERIAL INTERFACE AND TEST CONTROL

LOGIC DESIGN IMPLEMENTATION

A graduate project submitted in partial fulfillment of the requirements
For the degree of Master of Science
in Electrical Engineering.

By

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May 2012

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Abstract

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The overall project is to create a system that automatically tests the internal components of Xilinx Virtex 4 LX200 device, while the device is running in a thermal chamber at temperatures that stresses the device ratings.
The purpose of test is to detect the above or below normal temperatures that the device operates reliably to determine if the part can be up-screened.
Also the overall system design is to provide a generic test-bed to be used on screening future parts within the same family.

The overall system components are: the Unit Under Test (UUT), an Interface Adapter Board and a PC hosting the software that controls the test process.

This project report is specifically about the circuit design that provides for the logic implementation in VHDL (Very High Speed Hardware Description Language) that is programmed in the UUT. By it self, this project report is a standalone circuit design that follows the hardware and software interface requirements. The programmed device then will provide for an asynchronous serial interface, test execution control and feedback test results for different internal components of the UUT.

The end product of the design implementation is a program file that will be loaded in the UUT.
The VHDL code, programming file and supporting files are included in a CD ROM identified with the project name and released with this report.

Chapter 1 : Introduction

This project report contains the Virtex 4 LX-200 Burn-In Test Board logic design requirements, the circuit implementation in Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (HDL), the circuit requirements verification and the circuit design documentation.

Even though the overall project is related to the area of testability and reliability, this project deals with the logic implementation in a device so it can be tested and the test results can provide data for an assessment about the device under temperature stress conditions.

Consequently, this report will only deal with the logic design implantation, the requirement compliance and the design verification by methods of analysis simulation and test.

The overall system design shall discuss the necessity for screening tests, infant mortality, burn-in test and subjects related to testability and reliability.

This project by itself is self contain and the source code is transferable to other devices with exception of IP cores which are intrinsic to a particular device. Constrain file regarding to IO are driven by the hardware design.

1.1 Report Organization

Chapter 2 presents the applicable document used in the design implementation. Chapter 3 states the project definition and its requirements. In chapter 4 goes in detail about the design solution, while chapter 5 goes through the design verification.
Chapter 6 explains how the requirements are tested, while chapter 7 talks about the packaging and layout requirements.
Chapter 8 is the conclusion and closing statement of the project and the last chapter is the appendix that contains the design source code and test benches.

UUT FPGA - Xilinx Virtex-II 3000 - architecture, followed by the system description in chapter 3 where all the boards and cables are introduced in some details. In chapter 4, the driver board FPGA design is discussed. All the functional blocks implemented in the driver FPGA and their connectivity is shown. Finally, some conclusions and future enhancements are drawn in the final chapter.

Chapter 2 : Requirements

2.1 Item Definition

The Virtex 4 LX 200 Burn-in Test (BIT) Serial Interface and Control Circuit Element provides for the implementation of logic functions required by the project as follows:

- Provide a UART circuit to communicate with the Adapter Board via an RS-232 interface.
- Accept Discrete Inputs as “COMMANDS” input settings from the Adapter Board.
- Drive Discrete Outputs as “STATUS” of processes to the Adapter Board.
- Decode and process “TEST VECTORS” driven through the Adapter Board via the RS-232 Interface. Vector to Process are: Block RAM, DSP and Input and Output Wrap Around.
- Output “Test Data” via the UART transmitter.
- Set up constrain file at the configuration level per Burn-in test schematic diagram.

Figure 1 shows the interconnect diagram of this circuit and its immediate interface.

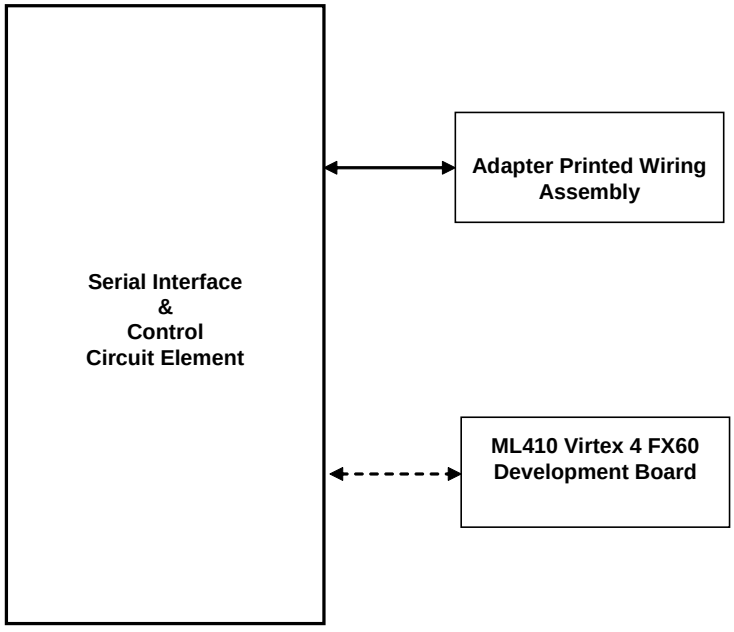


Figure 1. Circuit Element Interconnect Diagram

2.2 Electrical Interfaces

The circuit shall have the input, output, power, and test interfaces as specified in Figure 2.

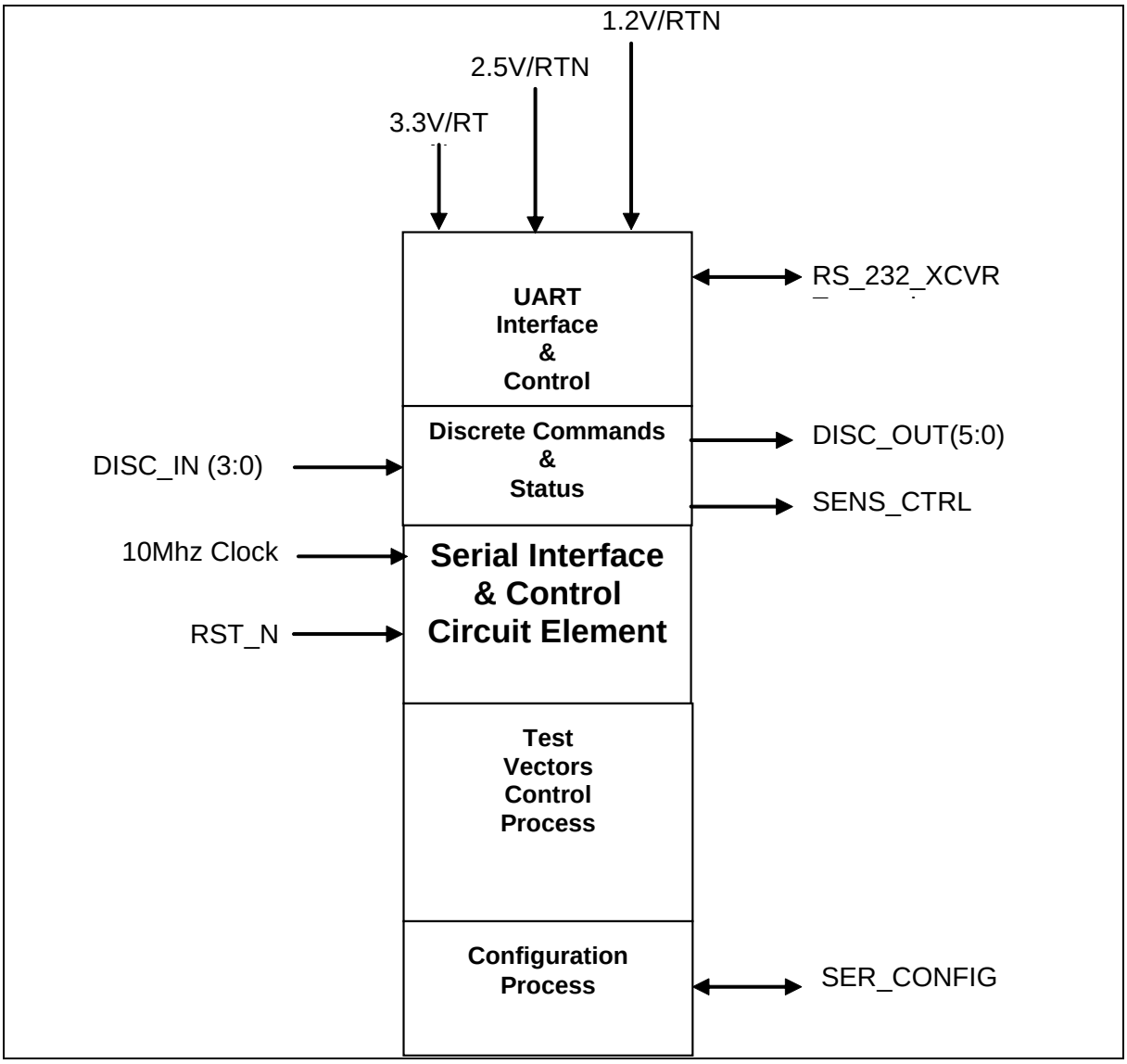


Figure 2. Interface Diagram

2.2.1 Input Signals

The circuit shall function as specified, when it receives the input signals listed in Table I.

Table I. Input Interface Description

Signal Name	Description	Type
DISC_IN(3:0) X 4	4 Discrete Inputs	Digital
RST_N	Device reset	Digital

The circuit shall function as specified, when all the digital input signals (listed in Table I) have the characteristics of a standard LVTTL device, driving one standard LVTTL load.

2.2.2 Output Signals

This circuit, when functioning as specified shall generate the output signals listed in Table II.

Table II. Output Interface Description

Signal	Description	Type
DISC_OUT(5:0)	6 Possible discrete outputs.	Digital
SENS_CTRL	Temperature sensor control signals	Digital

The circuit, when functioning as specified shall generate all the digital output signals (listed in Table II) compliant with the characteristics of a standard LVTTL output device, capable of driving into ten (10) standard LVTTL loads.

2.2.3 Bidirectional Signals

The circuit shall function as specified, when it receives the input signals listed in Table II.

Table III. Bi-Directional Interface Description

Signal Name	Description	Type
RS_232_XCVR	Serial Interface	Digital
SER_CONFIG	Serial Configuration Device interface	Digital

The circuit, when functioning as specified shall generate bi-directional signals compliant with the characteristics of a standard LVTTL output device, capable of driving into ten (10) standard LVTTL loads and as a standard LVTTL input device, driven into one standard LVTTL load.

2.2.4 Power Supply

The circuit shall function as specified, when it receives the power supply inputs listed in Table V.

Table IV. Power Supply Interface Description

Signal Name	Description	Type
3.3VDC/RTN	Input 3.3VDC and return	Power
2.5VDC/RTN	Input 2.5VDC and return	Power
1.2VDC/RTN	Input 1.2VDC and return	Power

The circuit shall function as specified, when the power supply inputs have the characteristics specified in Table VI.

Table V. Power Supply Characteristics

Supply Voltage	Parameter	Conditions	Min	Nom	Max	Units
3.3	Voltage		3.13	3.3	3.45	V
	Current		150	300	500	mA
	Ripple	10Hz to100kHz			10	mVpp
2.5	Voltage		2.2	2.5	2.7	V
	Current		150	300	500	mA
	Ripple	10Hz to100kHz			10	mVpp
1.2	Voltage		1.1	1.2	1.30	V
	Current				20	mA
	Ripple	10Hz to100kHz			10	mVpp

The circuit, when functioning as specified shall load the power inputs with the requirements specified in Table VII.

Table VI. Power Supply Load Requirements

Supply Voltage	Parameter	Conditions	Min	Nom	Max	Units
3.3V	Load Capacitance				10	µF
5V	Load Capacitance				10	µF
1.2V	Load Capacitance				10	µF

2.2.5 Electrostatic Discharge (ESD) Protection

Electrical equipment shall perform as specified after exposure to personnel induced electrostatic discharge (ESD) equivalent to a minimum of 4,000 volts (from a 150 picofarad (pF) source capacitor through a 330 ohm series resistor) onto each external connector contact (pin/receptacle) with respect to chassis ground. This requirement shall be met without electrical cable interfaces.

2.3 Mechanical Interfaces & Requirements

The circuit I/O shall interface with the connector as described on the Burn-in test schematic drawing.

2.4 Functional Performance

Figure 3 shows the functional block diagram of this circuit. The functional performance of the different logic blocks within the circuit is described below.

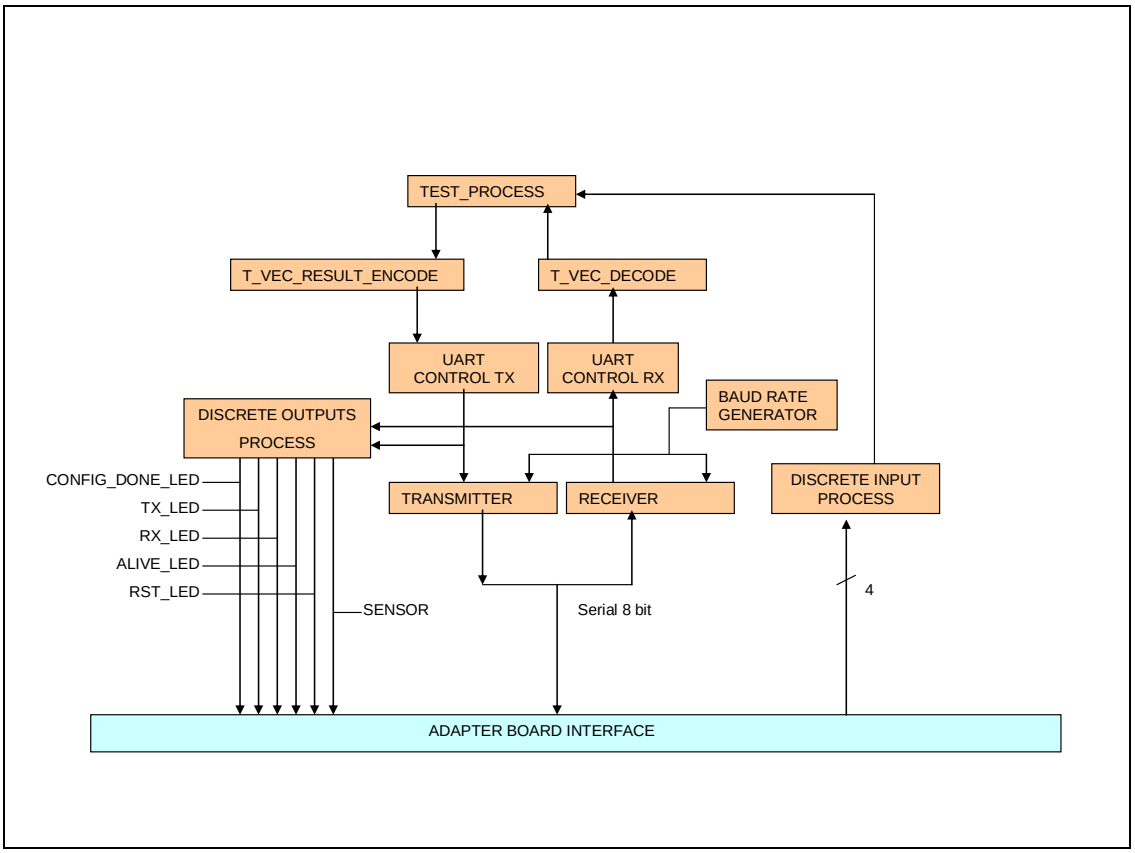


Figure 3. Functional Block Diagram

The unit under test is isolated from the rest of the components which reside on the interface adapter PWA. The purpose of this implementation is to keep the UUT with minimum number of components that will be stressed from -55°C to 125 °C of temperature.
The UUT has then the Virtex FPGA, the clock oscillator which operates at 10 MHz, a thermocouple and a whole bunch of resistor and capacitor.

2.4.1 Interface Connector

The connector provides the interface for the power signals, serial communication and discrete Input and Output to the UUT.

2.4.2 Baud Rate Generator

It is a logic implementation that provides for the proper BAUD rate for this implementation. Per requirement it is 9600 Baud.

2.4.3 UART

2.4.3.1 Receiver

This is another logic implementation of the UART input. It is an asynchronous process and it consists of UART receiver, UART baud rate generator and UART receiver control.
It provides for the proper reception and detection of data coming across the serial input at 9600 Baud.
Reads the serial data coming in and creates an 8 bit word.

2.4.3.2 Transmitter

This is another logic implementation of the UART output. It is an asynchronous process and it consists of the UART transmitter, UART baud rate generator and UART transmitter control.
It provides for the proper setup of the parallel word to be transmitted serially at 9600 Baud.

2.4.4 Test Process

2.4.4.1 Test Vector Decode

This logic block, parses the serial data in a way that the Test Vector Decode can utilize to execute the test. Transfers the data from the serial receiver and stores it in a RAM for later user.

2.4.4.2 Test Vector Results Encode

One the test vector has been executed, this logic block takes the data to a holding memory location and then sets it up ready for a parallel to serial translation so it can be send back via the serial transmitter.

2.4.5 Discrete Input - Output Processing.

2.4.5.1 Discrete Input Data

This section is reserved for the processing of discrete levels that will indicate the process a particular action.
Currently a generic switch is allocated to be use as a loop back control for troubleshooting purposes.

2.4.5.2 Discrete Output Data

This block is use to provide visual display of the status of the UUT. Several LEDs are utilized as indicators of different operations in the UUT, such as a heartbeat indicating an “I am alive” condition of the UUT among others

2.5 Environmental Conditions

The circuit shall function as specified, prior, during, and after exposure to the environments specified in Table XII. The Stress test shall go beyond the environmental conditions to 125°C

Table VII. Environmental Conditions

Environmental Parameter	Range
Non-Operating Temperature	Ambient
Operating Temperature	-40 to +100°C
Vibration	TBD
Shock	TBD

2.6 Testability and Producibility

The design of the circuit shall be testable at the Printed Wiring Assembly (PWA). The design of the circuit shall be producible at the Printed Wiring Assembly (PWA).

2.7 Programmatic Requirements

2.7.1 EEE Parts

All EEE parts are commercial grade, except for the FPGA which is industrial grade.

Chapter 3 Design Solution

3.1 Operational Description

This circuit has been implemented in VHDL. The circuit implementation code and test-benches have been attached in appendix section.
This circuit supports three main logic functions as described below, they are: UART Control, Test Vector Process and Discrete I/O Control also shown in Figure 4.

3.1.1 Asynchronous UART

This Circuit provides for non-clocked serial communications between two devices. There is a receiver and transmitter logic implementation set up to operate at Baud 9600 bps.
The receiver once detected the start bit of a new word, collects each bit one of the data bits into a shift register. At the end of the bit collection, the data contents of the shift register are copied into a transfer register to be used by other module.

On the transmitter end, this circuit waits for a flag that indicates that the "Transfer Buffer" is not empty. Once the detection of the "not empty" occurs; the UART_TX start putting one bit at the time in the transmitter output at the agreed baud rate.

3.1.2 Test Vector Execution

This logic block process the data stored by the receiver UART. It decodes the command data word as stated in the Software Interface Requirement section. The decoded output then selects the command to be executed.

The design implement three main tests; Block RAM, DSP and DIO. Each one these tests have also a variety of subtype selections. The command decode word will then execute the selected type. The result of the test will be stored in a RAM to be use in a later process.

3.1.3 Test Results Process

Once the test has been executed, this logic block transfers the test results from the memory storage location where the test data has been placed, to the transmitter FIFO.
Once the transmitter FIFO starts getting filled in with data, a flag is set that triggers the transmitter UART with a signal that data is ready to be transmitted.

3.1.4 Discrete I/O Control

This logic block monitors for discrete inputs and drives discrete outputs.
Current implementation only requires for detecting a loop back switch setting and to provide for I am alive" discrete output.
I addition to provide a visual output of the "I'm alive" status, this circuits also hook-up to the LEDs for the transmitter and receiver traffic.

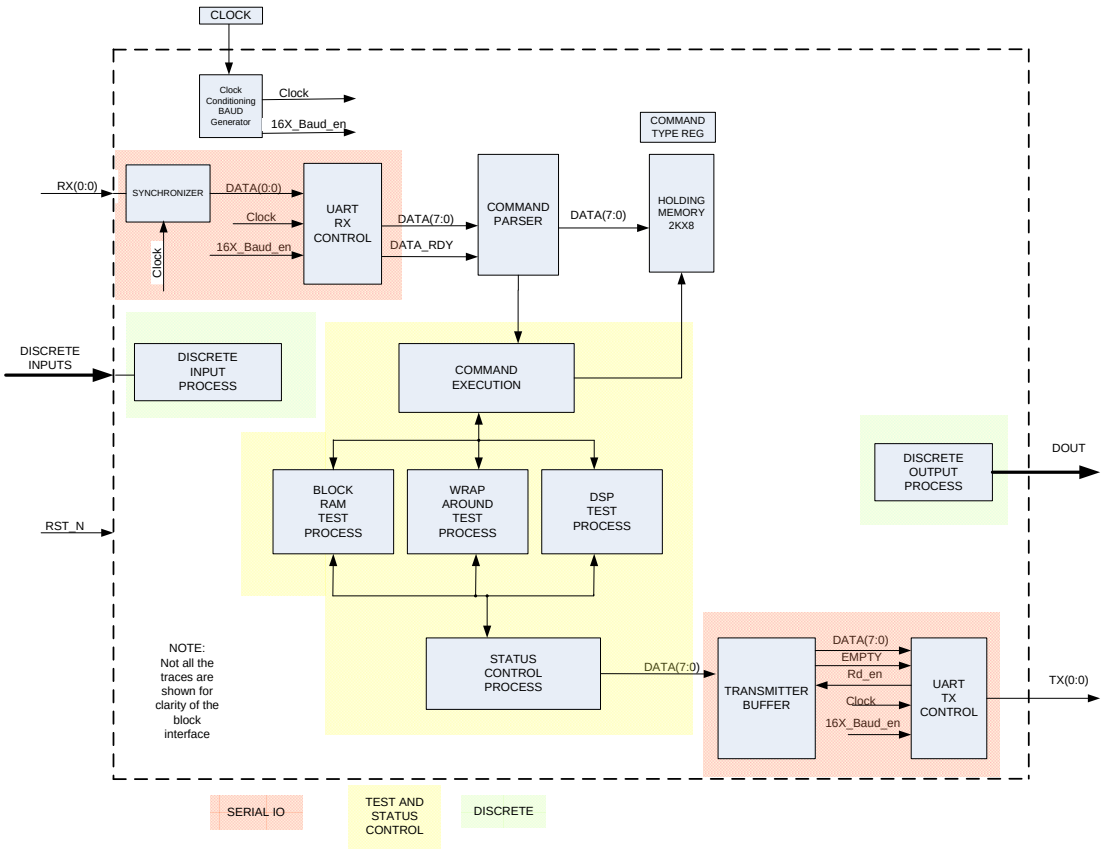


Figure 4. Operational Block Diagram

3.2 Circuit Description

3.2.1 Baud Generator

The Baud Generator block is a clock divider that outputs a 100nS pulse 16 times per every bit that the UUT receives or transmits. The output of the clock divider is based on the selected clock and baud rate of the system.
This implementation has a system clock of 10 MHz and the selected baud rate is 9600 bps.

3.2.2 UART Receiver

UART receiver controller implements the state machines for doing RS232 reception.
Based on the detection of the falling edge of the synchronized rxd input, this module waits 1/2 of a bit period (8 periods of baud_x16_en) to find the middle of the start bit, and re-samples it. If rxd is still low it accepts it as a valid START bit, and captures the rest of the character, otherwise it rejects the start bit and returns to idle.

After detecting the START bit, it advances 1 full bit period at a time (16 periods of baud_x16_en) to end up in the middle of the 8 data bits, where it samples the 8 data bits.

After the last bit is sampled (the MSbit, since the LSbit is sent first), it waits one additional bit period to check for the STOP bit. If the rxd line is not high (the value of a STOP bit), a framing error is signaled regardless of the value of the rxd, though, the module returns to the IDLE state and immediately begins looking for the start of the next character.

The following picture shows the state machine used for the bit recognition. Separate process are use to determine the 16 count per bit and the bit count within the received word.
This module utilizes the output of the Baud generator module as a pulse to count the bit samples.

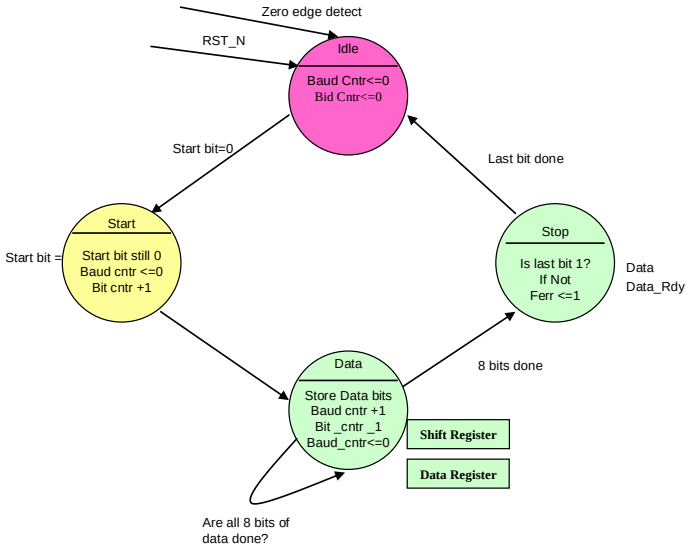


Figure 5. UART rx Finite State Machine

3.2.3 Receiver Data Parcer

This circuit is another State Machine that takes the receiver data and stores it into a holding memory (dual port RAM), so it can be used by the "Test Command" module in the execution of the test.

When in IDLE state, it waits for the rising edge detect of DATA_RDY signal, once this occurs, it indicates that the first word has arrived. Then it goes to the next state the where it compares to the constant (hex 0x66) allocated to the START WORD.

If compare matches, then it sets a flag indicating that the Start Word was detected, and it goes to the next state (CMD_TEST); otherwise, it returns to the Idle State. Once in the CMD_TEST, the command word is registered and it moves to the ADDR_INIT state. At this point the address counter is initialized, and the max_address variable is set to the maximum number of words to be written into the holding memory. Then the state advances to the DATA_WRDS state.

Once in this state, once per every rising edge of the rx_data rdy flag, the receive data is read and copy (written) to the holding memory. It will loop in this state as long as all the words are read and written to the holding memory. Once this task is completed, the state advances to the LAST_WORD state. In this last state, the START flag is cleared and the END flag is set. The END WORD (hex 0xE7) is tested and it returns to the IDLE state, and stays there until the next word arrives.

3.2.4 Test Execution

After data has gone thru the receiver block, the command word is stored into a register and the receiving data is stored into a holding memory.
The decoded command indicates of what test has to be executed as stated on the Software Interface Requirement section. The Test Vector Execution (TVE) logic block, uses the decode indicator to trigger the beginning of the test execution.

This design implement in a modular manner, in case more test need to be added. This implementation supports three main tests: Block RAM, DSP and DIO. Each type of test has a subset of test and they are executed based on the command decode.
The Block RAM test supports tests to 1x16K, 2x8K, 4x4K and 8x2K BRAM.
For the DSP Test, the test can exercise an ADD, Subtract, Multiply or divide type of operations.
For the DIO Wrap around a series of 640 bits will be daisy chained through the IO pins via a shift register, and collected at the other by a shift register to finally be transfer to a holding memory and then transmitted back to the sender.

In all types of test, the whole process consists in manipulation data, and placing the data in the right format to do read and write operation, or to do arithmetic operations or to be serially shifted into the DIO. Once the test has been executed a flag is set that indicates that data is ready to re-formatted by the "Test result process" so it can be loaded into the transmitter FIFO.

3.2.5 Test Results Process

The test result process transfer the data from a RAM location which holds the test data results to the Transmitter FIFO.
This module sets up the Start word, the Command word tested, the Data words (test results) and the End word packet for transmission

3.2.6 UART Transmitter

The UART transmitter, implements the state machines for doing RS232 transmission. Whenever a character is ready for transmission (as indicated by the empty signal from the transmitter FIFO); this module will transmit the character. The basis of this design is a simple state machine. When in IDLE, it waits for the transmitter FIFO to indicate that a character is available, at which time, it immediately starts transmit ion. It spends 16 baud_x16_en periods in the START state, transmitting the START condition (1'b0), then transitions to the DATA state, where it sends the 8 data bits (LSbit first), each lasting 16 baud_x16_en periods, and finally going to the STOP state for 16 periods, where it transmits the STOP value (1'b1).

On the last baud_x16_en period of the last data bit (in the DATA state), it issues the POP signal to the character FIFO. Since the State Machine is only enabled when baud_x16_en is asserted, the resulting pop signal must then be ANDed with baud_x16_en to ensure that only one character is popped at a time.

On the last baud_x16_en period of the STOP state, the empty indication from the character FIFO is inspected; if asserted, the State Machine returns to the IDLE state, otherwise it transitions directly to the START state to start the transmission of the next character.

There are two internal counters; one which counts off the 16 pulses of baud_x16_en, and a second which counts the 8 bits of data.
The generation of the output (txd_tx) follows one complete baud_x16_en period after the state machine and other internal counters.

3.2.7 Discrete I/O Control

On the discrete input side, this circuit element monitors the switch status for the loop back control. If set to one, the UARTs have their normal operations. If set to “zero” then the transmit output is loop back to the received input.

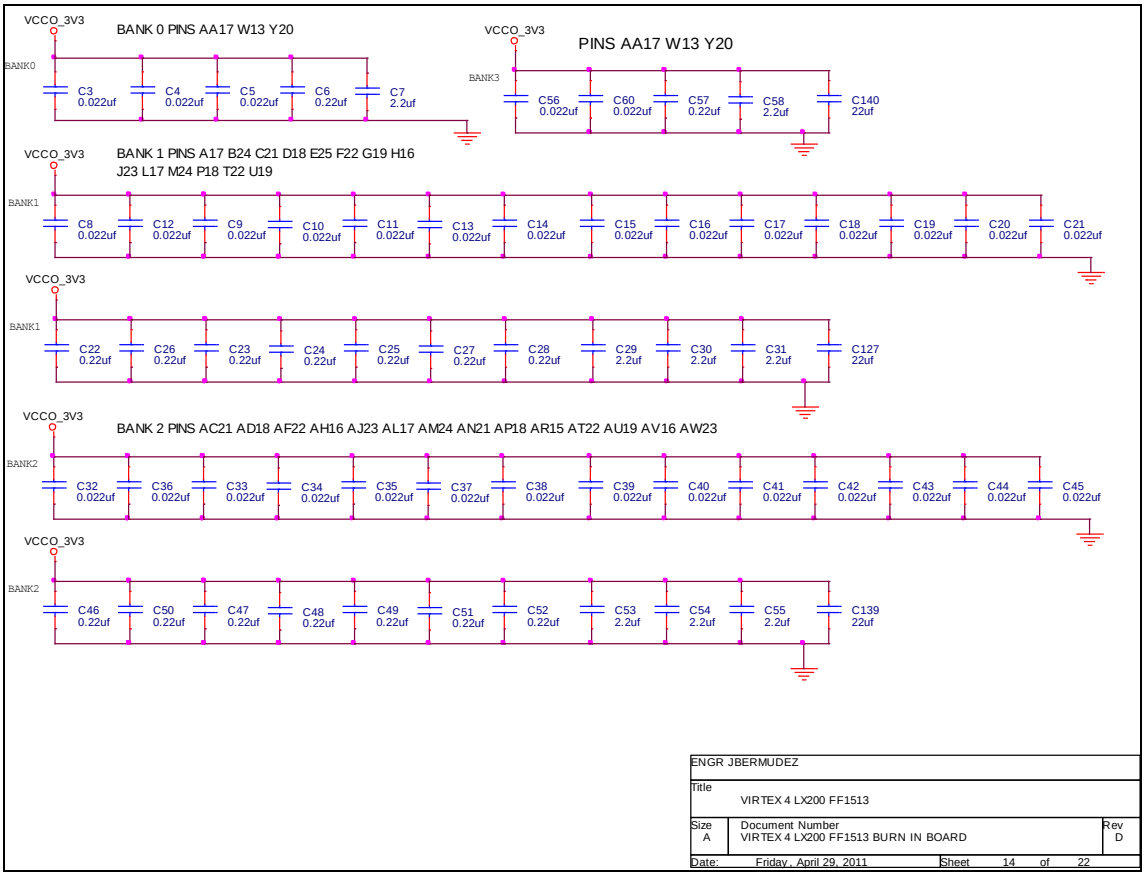
The Discrete output section deals with connecting one of the outputs to the “I ‘m alive" signal. This signal represent that the system has been successfully program and it is running. Other discrete output implementations are the connections of the TX and RX signals to the two different LED to indicate transmit and receive traffic. Pin assignment for the interface is described in the unit constrain file and also are specified in the schematic diagram.

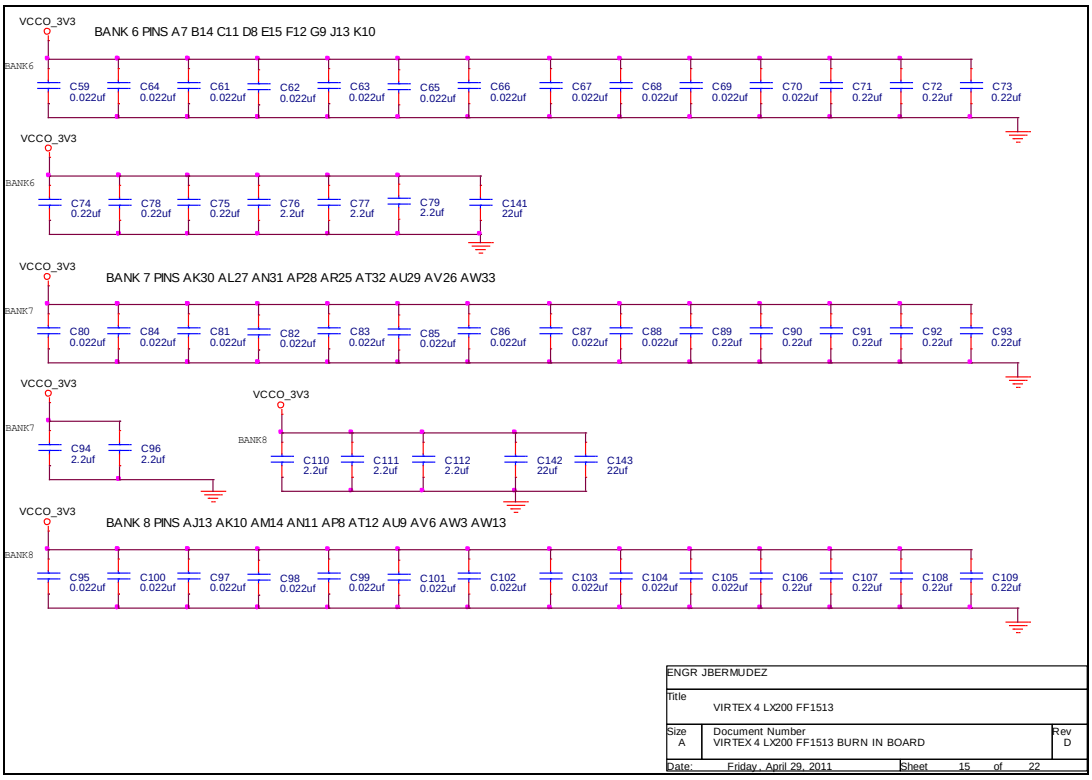
3.2.8 Schematics

This section contains the Burn-in Test Board circuit schematics.
The schematic also shows the Virtex 4 LX200, a component selected for the logic implementation and used on the Unit Under Test (UUT). In addition to this FPGA, this circuit uses a 10 MHz clock, and a temperature sensor to let the user know the temperature under test. The circuit is powered externally; it uses 3.3V for the I/O interface and 2.5V for the LVDS interface and 1.2V for the core voltage. Finally the passive components are the resistors and capacitors spread all over the circuit. The detailed parts list of this circuit is described on the parts list section.

3.2.8.1 Decoupling Capacitors

The following schematic sheets are related to the Circuit Element Decoupling capacitors.

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BANK6
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C64 0.022uf
C61 0.022uf
C62 0.022uf
C63 0.022uf
C65 0.022uf
C66 0.022uf
C67 0.022uf
C68 0.022uf
C69 0.022uf
C70 0.022uf
C71 0.22uf
C72 0.22uf
C73 0.22uf
C74 0.22uf
C78 0.22uf
C75 0.22uf
C76 2.2uf
C77 2.2uf
C79 2.2uf
C141 22uf
BANK 7 PINS AK30 AL27 AN31 AP28 AR25 AT32 AU29 AV26 AW33
BANK7
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C84 0.022uf
C81 0.022uf
C82 0.022uf
C83 0.022uf
C85 0.022uf
C86 0.022uf
C87 0.022uf
C88 0.022uf
C89 0.22uf
C90 0.22uf
C91 0.22uf
C92 0.22uf
C93 0.22uf
C94 2.2uf
C96 2.2uf
BANK8
C110 2.2uf
C111 2.2uf
C112 2.2uf
C142 22uf
C143 22uf
BANK 8 PINS AJ13 AK10 AM14 AN11 AP8 AT12 AU9 AV6 AW3 AW13
C95 0.022uf
C100 0.022uf
C97 0.022uf
C98 0.022uf
C99 0.022uf
C101 0.022uf
C102 0.022uf
C103 0.022uf
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Title
VIRTEX 4 LX200 FF1513
Size A
Document Number
VIRTEX 4 LX200 FF1513 BURN IN BOARD
Rev D
Date: Friday, April 29, 2011
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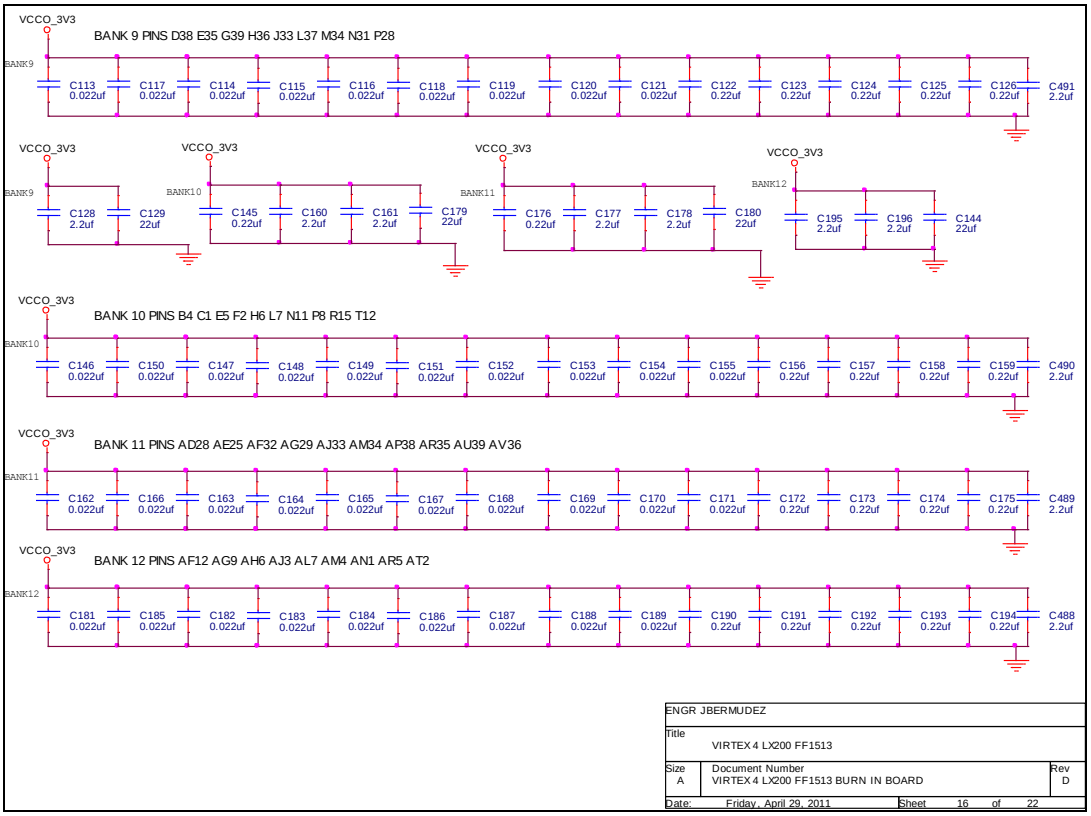
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BANK9
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C178 2.2uf
C180 22uf
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C154 0.022uf
C155 0.022uf
C156 0.22uf
C157 0.22uf
C158 0.22uf
C159 0.22uf
C490 2.2uf
BANK 11 PINS AD28 AE25 AF32 AG29 AJ33 AM34 AP38 AR35 AU39 AV36
C162 0.022uf
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C163 0.022uf
C164 0.022uf
C165 0.022uf
C167 0.022uf
C168 0.022uf
C169 0.022uf
C170 0.022uf
C171 0.022uf
C172 0.22uf
C173 0.22uf
C174 0.22uf
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C489 2.2uf
BANK 12 PINS AF12 AG9 AH6 AJ3 AL7 AM4 AN1 AR5 AT2
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C194 0.22uf
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Size A
Document Number
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Rev D
Date: Friday, April 29, 2011
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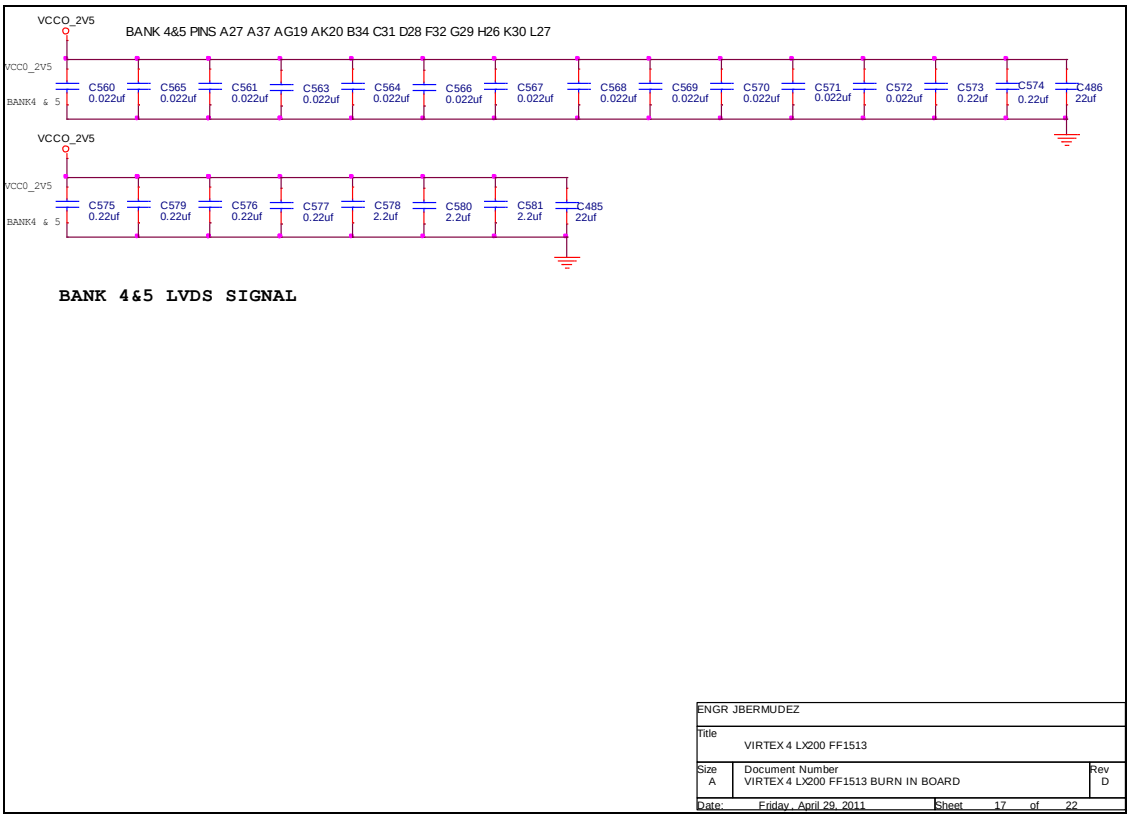
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C561 0.022uf
C563 0.022uf
C564 0.022uf
C566 0.022uf
C567 0.022uf
C568 0.022uf
C569 0.022uf
C570 0.022uf
C571 0.022uf
C572 0.022uf
C573 0.22uf
C574 0.22uf
C486 22uf
VCCO_2V5
VCCO_2V5
BANK4 & 5
C575 0.22uf
C579 0.22uf
C576 0.22uf
C577 0.22uf
C578 2.2uf
C580 2.2uf
C581 2.2uf
C485 22uf
BANK 4&5 LVDS SIGNAL
ENGR JBERMUDEZ
Title
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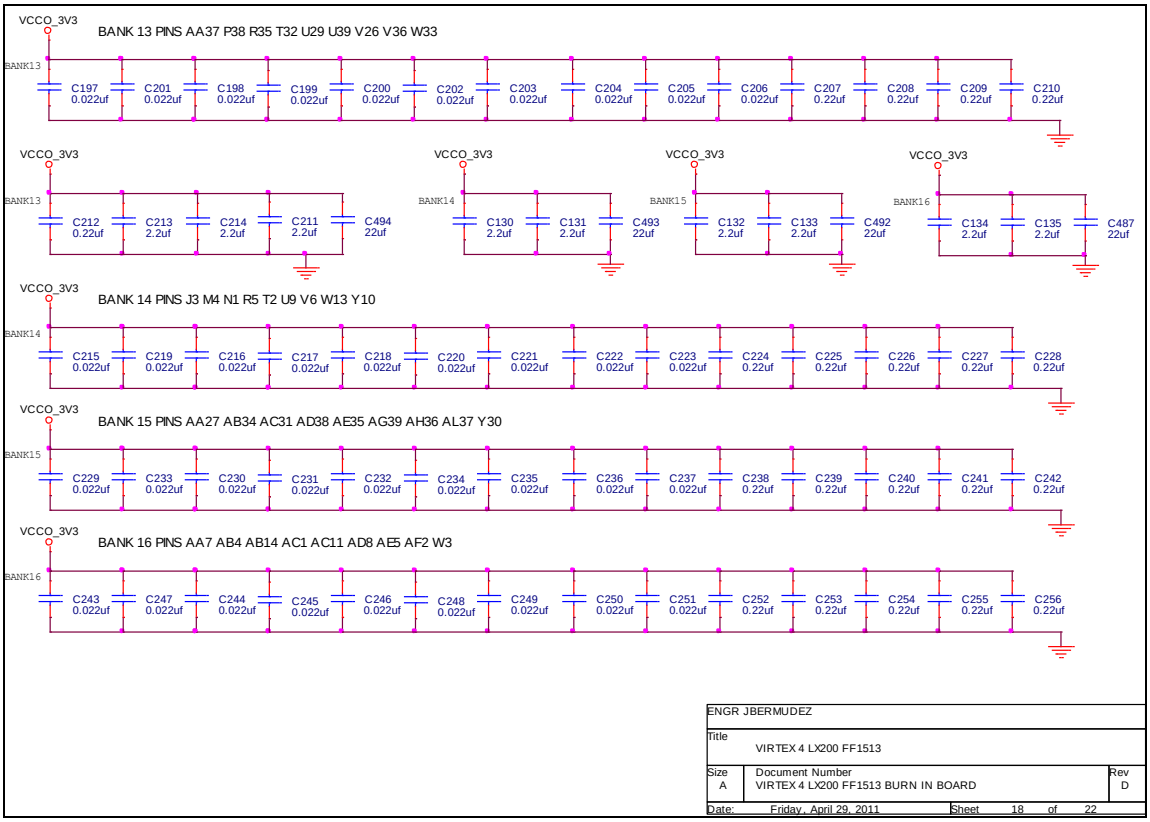
VCCO_3V3
BANK 13 PINS AA37 P38 R35 T32 U29 U39 V26 V36 W33
BANK13
C197 0.022uf
C201 0.022uf
C198 0.022uf
C199 0.022uf
C200 0.022uf
C202 0.022uf
C203 0.022uf
C204 0.022uf
C205 0.022uf
C206 0.022uf
C207 0.22uf
C208 0.22uf
C209 0.22uf
C210 0.22uf
VCCO_3V3
BANK13
C212 0.22uf
C213 2.2uf
C214 2.2uf
C211 2.2uf
C494 22uf
VCCO_3V3
BANK14
C130 2.2uf
C131 2.2uf
C493 22uf
VCCO_3V3
BANK15
C132 2.2uf
C133 2.2uf
C492 22uf
VCCO_3V3
BANK16
C134 2.2uf
C135 2.2uf
C487 22uf
VCCO_3V3
BANK 14 PINS J3 M4 N1 R5 T2 U9 V6 W13 Y10
BANK14
C215 0.022uf
C219 0.022uf
C216 0.022uf
C217 0.022uf
C218 0.022uf
C220 0.022uf
C221 0.022uf
C222 0.022uf
C223 0.022uf
C224 0.22uf
C225 0.22uf
C226 0.22uf
C227 0.22uf
C228 0.22uf
VCCO_3V3
BANK 15 PINS AA27 AB34 AC31 AD38 AE35 AG39 AH36 AL37 Y30
BANK15
C229 0.022uf
C233 0.022uf
C230 0.022uf
C231 0.022uf
C232 0.022uf
C234 0.022uf
C235 0.022uf
C236 0.022uf
C237 0.022uf
C238 0.22uf
C239 0.22uf
C240 0.22uf
C241 0.22uf
C242 0.22uf
VCCO_3V3
BANK 16 PINS AA7 AB4 AB14 AC1 AC11 AD8 AE5 AF2 W3
BANK16
C243 0.022uf
C247 0.022uf
C244 0.022uf
C245 0.022uf
C246 0.022uf
C248 0.022uf
C249 0.022uf
C250 0.022uf
C251 0.022uf
C252 0.22uf
C253 0.22uf
C254 0.22uf
C255 0.22uf
C256 0.22uf
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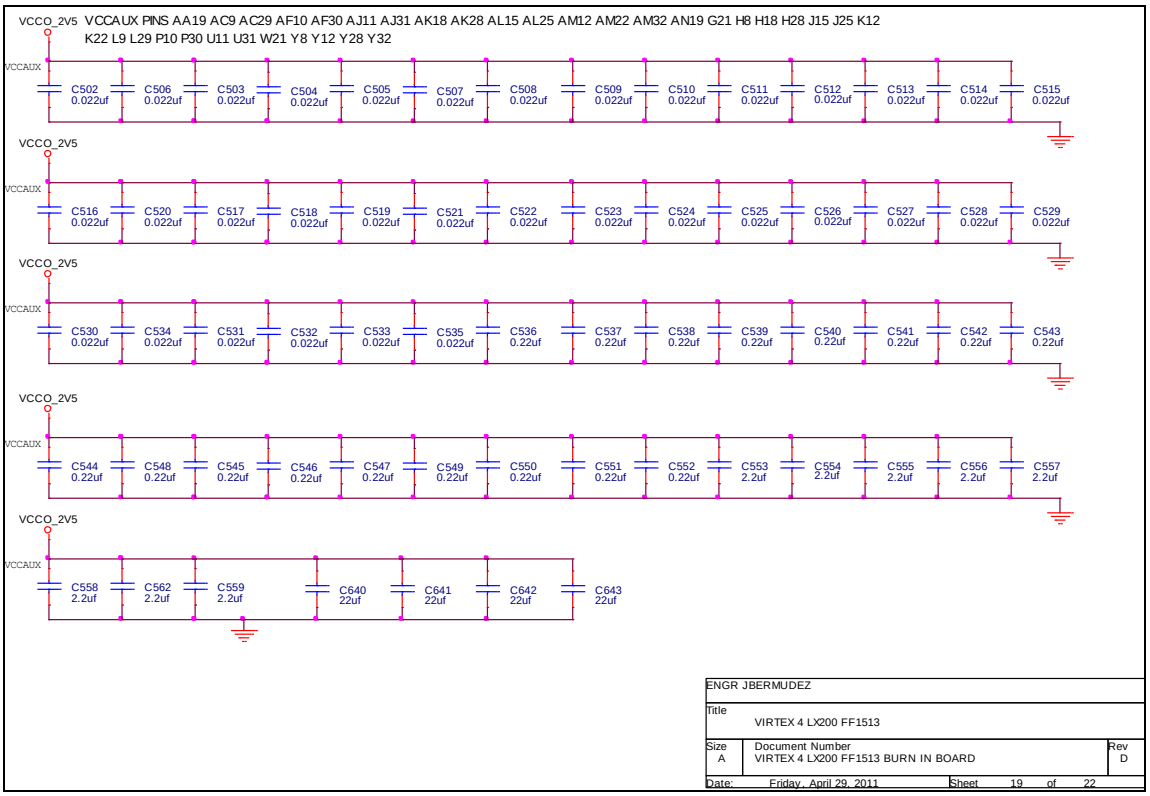
VCCO_2V5
VCCAUX PINS AA19 AC9 AC29 AF10 AF30 AJ11 AJ31 AK18 AK28 AL15 AL25 AM12 AM22 AM32 AN19 G21 H8 H18 H28 J15 J25 K12
K22 L9 L29 P10 P30 U11 U31 W21 Y8 Y12 Y28 Y32
VCCAUX
C502 0.022uf
C506 0.022uf
C503 0.022uf
C504 0.022uf
C505 0.022uf
C507 0.022uf
C508 0.022uf
C509 0.022uf
C510 0.022uf
C511 0.022uf
C512 0.022uf
C513 0.022uf
C514 0.022uf
C515 0.022uf
C516 0.022uf
C520 0.022uf
C517 0.022uf
C518 0.022uf
C519 0.022uf
C521 0.022uf
C522 0.022uf
C523 0.022uf
C524 0.022uf
C525 0.022uf
C526 0.022uf
C527 0.022uf
C528 0.022uf
C529 0.022uf
C530 0.022uf
C534 0.022uf
C531 0.022uf
C532 0.022uf
C533 0.022uf
C535 0.022uf
C536 0.22uf
C537 0.22uf
C538 0.22uf
C539 0.22uf
C540 0.22uf
C541 0.22uf
C542 0.22uf
C543 0.22uf
C544 0.22uf
C548 0.22uf
C545 0.22uf
C546 0.22uf
C547 0.22uf
C549 0.22uf
C550 0.22uf
C551 0.22uf
C552 0.22uf
C553 2.2uf
C554 2.2uf
C555 2.2uf
C556 2.2uf
C557 2.2uf
C558 2.2uf
C562 2.2uf
C559 2.2uf
C640 22uf
C641 22uf
C642 22uf
C643 22uf
ENGR JBERMUDEZ
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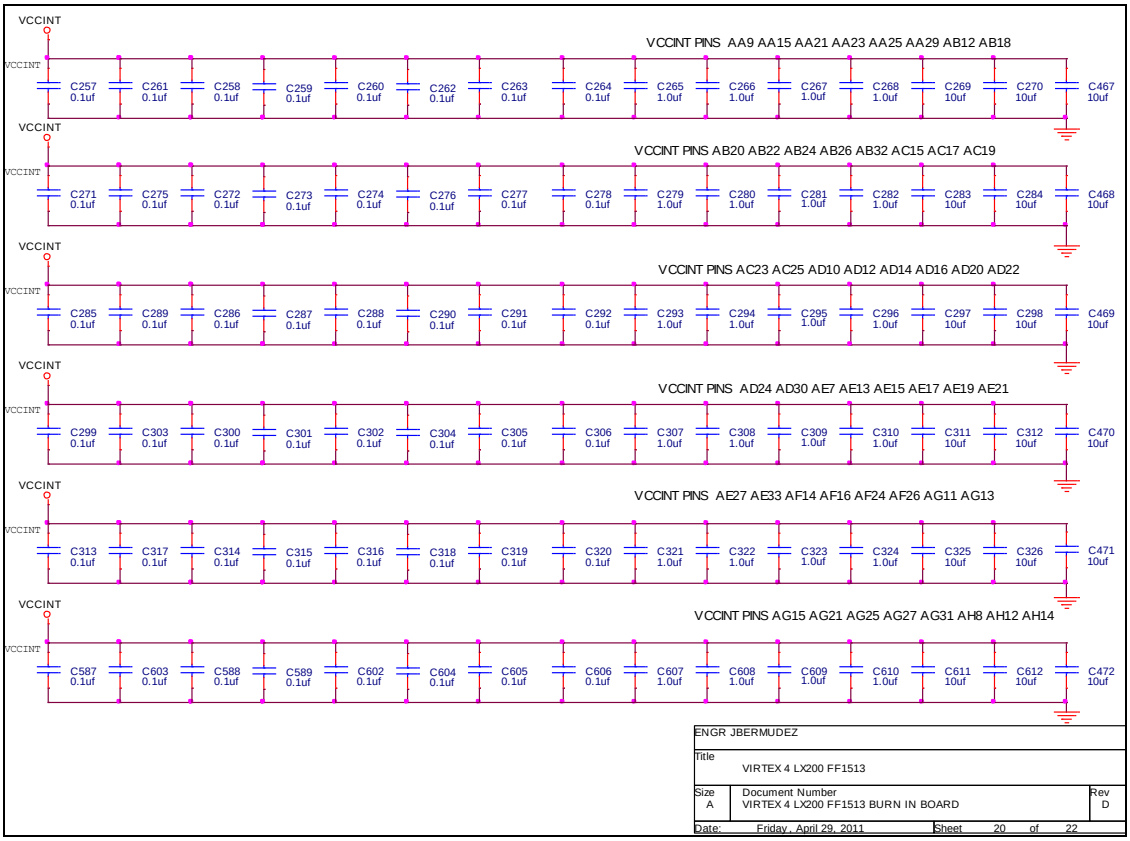
VCCINT
VCCINT PINS AA9 AA15 AA21 AA23 AA25 AA29 AB12 AB18
C257 0.1uf
C261 0.1uf
C258 0.1uf
C259 0.1uf
C260 0.1uf
C262 0.1uf
C263 0.1uf
C264 0.1uf
C265 1.0uf
C266 1.0uf
C267 1.0uf
C268 1.0uf
C269 10uf
C270 10uf
C467 10uf
VCCINT PINS AB20 AB22 AB24 AB26 AB32 AC15 AC17 AC19
C271 0.1uf
C275 0.1uf
C272 0.1uf
C273 0.1uf
C274 0.1uf
C276 0.1uf
C277 0.1uf
C278 0.1uf
C279 1.0uf
C280 1.0uf
C281 1.0uf
C282 1.0uf
C283 10uf
C284 10uf
C468 10uf
VCCINT PINS AC23 AC25 AD10 AD12 AD14 AD16 AD20 AD22
C285 0.1uf
C289 0.1uf
C286 0.1uf
C287 0.1uf
C288 0.1uf
C290 0.1uf
C291 0.1uf
C292 0.1uf
C293 1.0uf
C294 1.0uf
C295 1.0uf
C296 1.0uf
C297 10uf
C298 10uf
C469 10uf
VCCINT PINS AD24 AD30 AE7 AE13 AE15 AE17 AE19 AE21
C299 0.1uf
C303 0.1uf
C300 0.1uf
C301 0.1uf
C302 0.1uf
C304 0.1uf
C305 0.1uf
C306 0.1uf
C307 1.0uf
C308 1.0uf
C309 1.0uf
C310 1.0uf
C311 10uf
C312 10uf
C470 10uf
VCCINT PINS AE27 AE33 AF14 AF16 AF24 AF26 AG11 AG13
C313 0.1uf
C317 0.1uf
C314 0.1uf
C315 0.1uf
C316 0.1uf
C318 0.1uf
C319 0.1uf
C320 0.1uf
C321 1.0uf
C322 1.0uf
C323 1.0uf
C324 1.0uf
C325 10uf
C326 10uf
C471 10uf
VCCINT PINS AG15 AG21 AG25 AG27 AG31 AH8 AH12 AH14
C587 0.1uf
C603 0.1uf
C588 0.1uf
C589 0.1uf
C602 0.1uf
C604 0.1uf
C605 0.1uf
C606 0.1uf
C607 1.0uf
C608 1.0uf
C609 1.0uf
C610 1.0uf
C611 10uf
C612 10uf
C472 10uf
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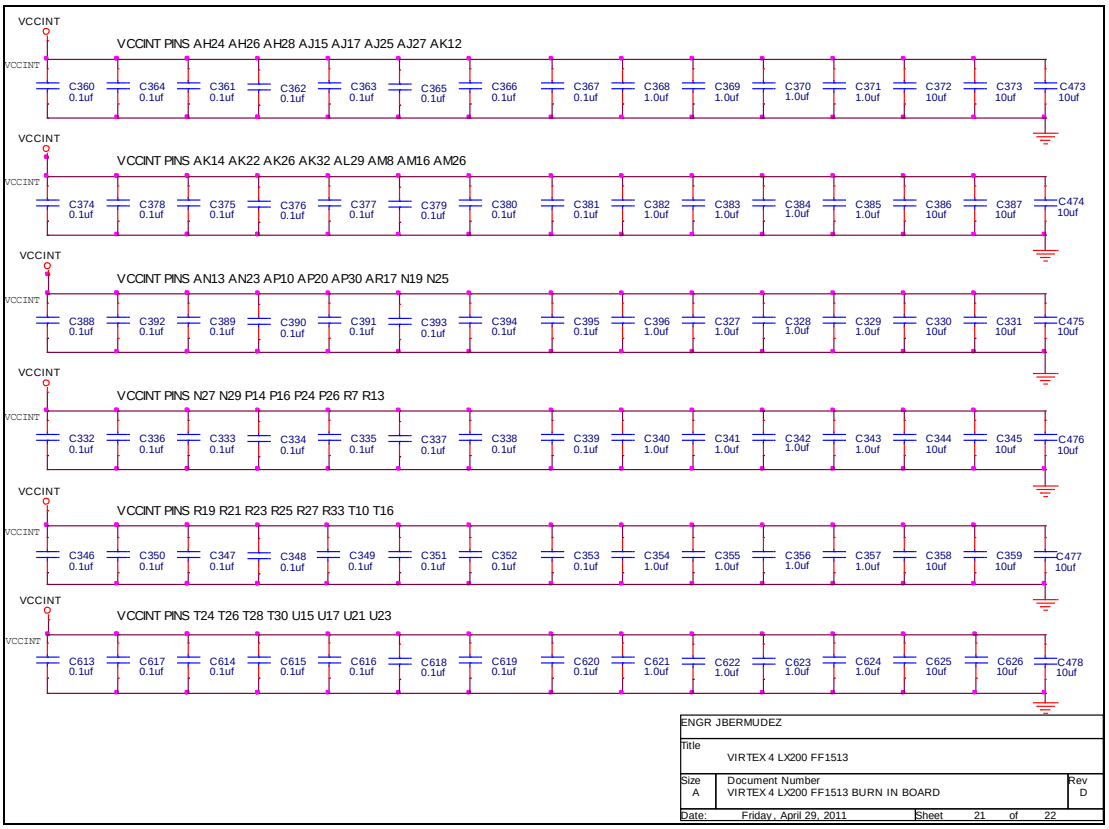
VCCINT
VCCINT PINS AH24 AH26 AH28 AJ15 AJ17 AJ25 AJ27 AK12
C360 0.1uf C364 0.1uf C361 0.1uf C362 0.1uf C363 0.1uf C365 0.1uf C366 0.1uf C367 0.1uf C368 1.0uf C369 1.0uf C370 1.0uf C371 1.0uf C372 10uf C373 10uf C473 10uf
VCCINT PINS AK14 AK22 AK26 AK32 AL29 AM8 AM16 AM26
C374 0.1uf C378 0.1uf C375 0.1uf C376 0.1uf C377 0.1uf C379 0.1uf C380 0.1uf C381 0.1uf C382 1.0uf C383 1.0uf C384 1.0uf C385 1.0uf C386 10uf C387 10uf C474 10uf
VCCINT PINS AN13 AN23 AP10 AP20 AP30 AR17 N19 N25
C388 0.1uf C392 0.1uf C389 0.1uf C390 0.1uf C391 0.1uf C393 0.1uf C394 0.1uf C395 0.1uf C396 1.0uf C327 1.0uf C328 1.0uf C329 1.0uf C330 10uf C331 10uf C475 10uf
VCCINT PINS N27 N29 P14 P16 P24 P26 R7 R13
C332 0.1uf C336 0.1uf C333 0.1uf C334 0.1uf C335 0.1uf C337 0.1uf C338 0.1uf C339 0.1uf C340 1.0uf C341 1.0uf C342 1.0uf C343 1.0uf C344 10uf C345 10uf C476 10uf
VCCINT PINS R19 R21 R23 R25 R27 R33 T10 T16
C346 0.1uf C350 0.1uf C347 0.1uf C348 0.1uf C349 0.1uf C351 0.1uf C352 0.1uf C353 0.1uf C354 1.0uf C355 1.0uf C356 1.0uf C357 1.0uf C358 10uf C359 10uf C477 10uf
VCCINT PINS T24 T26 T28 T30 U15 U17 U21 U23
C613 0.1uf C617 0.1uf C614 0.1uf C615 0.1uf C616 0.1uf C618 0.1uf C619 0.1uf C620 0.1uf C621 1.0uf C622 1.0uf C623 1.0uf C624 1.0uf C625 10uf C626 10uf C478 10uf
ENGR JBERMUDEZ
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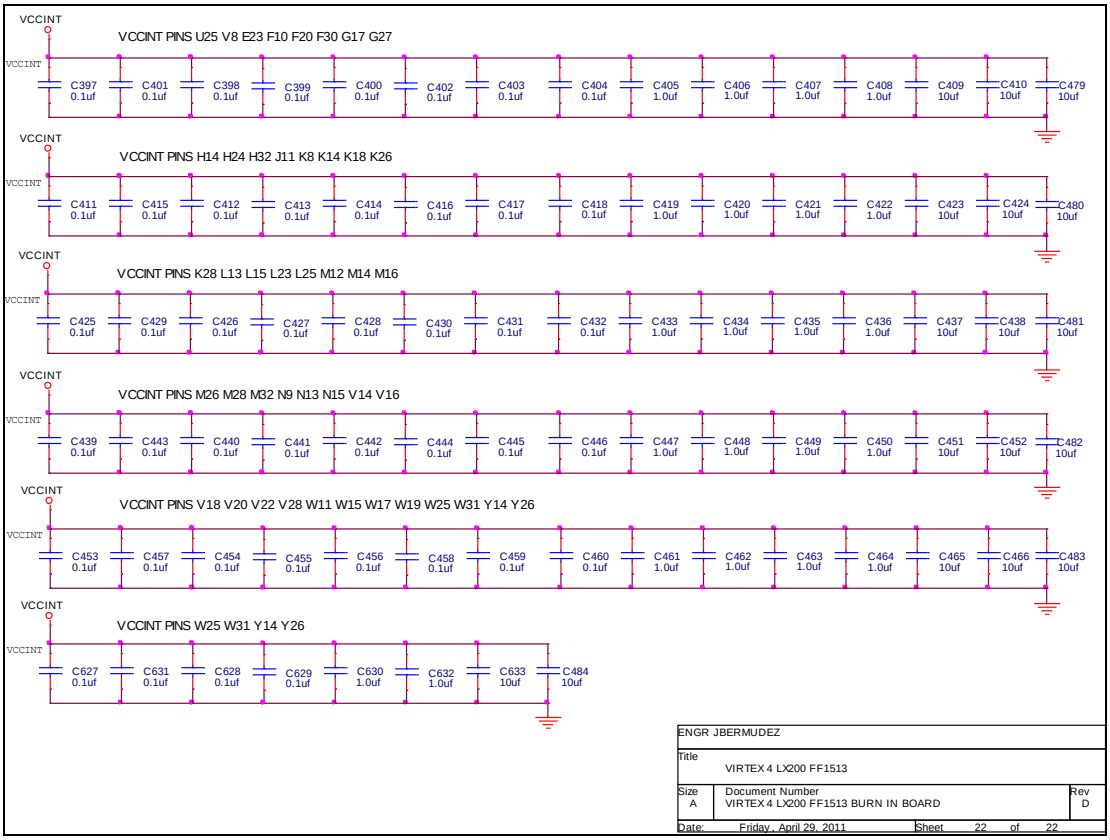
VCCINT
VCCINT PINS U25 V8 E23 F10 F20 F30 G17 G27
C397 0.1uf C401 0.1uf C398 0.1uf C399 0.1uf C400 0.1uf C402 0.1uf C403 0.1uf C404 0.1uf C405 1.0uf C406 1.0uf C407 1.0uf C408 1.0uf C409 10uf C410 10uf C479 10uf
VCCINT PINS H14 H24 H32 J11 K8 K14 K18 K26
C411 0.1uf C415 0.1uf C412 0.1uf C413 0.1uf C414 0.1uf C416 0.1uf C417 0.1uf C418 0.1uf C419 1.0uf C420 1.0uf C421 1.0uf C422 1.0uf C423 10uf C424 10uf C480 10uf
VCCINT PINS K28 L13 L15 L23 L25 M12 M14 M16
C425 0.1uf C429 0.1uf C426 0.1uf C427 0.1uf C428 0.1uf C430 0.1uf C431 0.1uf C432 0.1uf C433 1.0uf C434 1.0uf C435 1.0uf C436 1.0uf C437 10uf C438 10uf C481 10uf
VCCINT PINS M26 M28 M32 N9 N13 N15 V14 V16
C439 0.1uf C443 0.1uf C440 0.1uf C441 0.1uf C442 0.1uf C444 0.1uf C445 0.1uf C446 0.1uf C447 1.0uf C448 1.0uf C449 1.0uf C450 1.0uf C451 10uf C452 10uf C482 10uf
VCCINT PINS V18 V20 V22 V28 W11 W15 W17 W19 W25 W31 Y14 Y26
C453 0.1uf C457 0.1uf C454 0.1uf C455 0.1uf C456 0.1uf C458 0.1uf C459 0.1uf C460 0.1uf C461 1.0uf C462 1.0uf C463 1.0uf C464 1.0uf C465 10uf C466 10uf C483 10uf
VCCINT PINS W25 W31 Y14 Y26
C627 0.1uf C631 0.1uf C628 0.1uf C629 0.1uf C630 1.0uf C632 1.0uf C633 10uf C484 10uf
ENGR JBERMUDEZ
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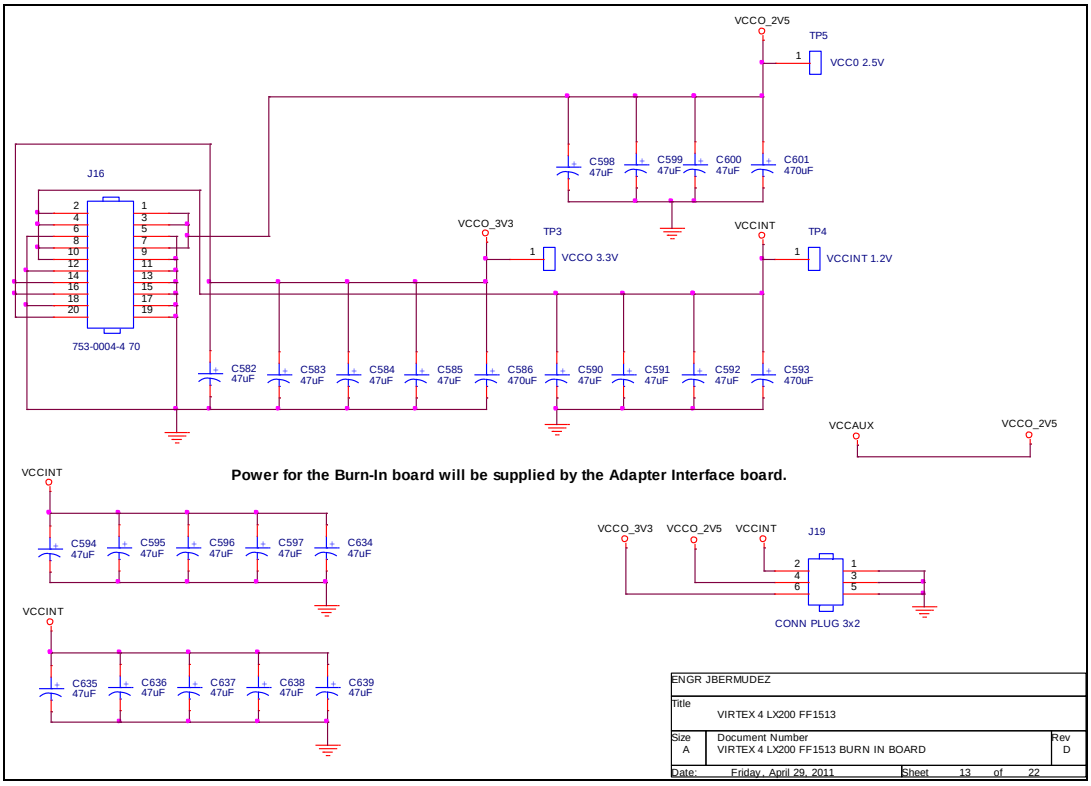
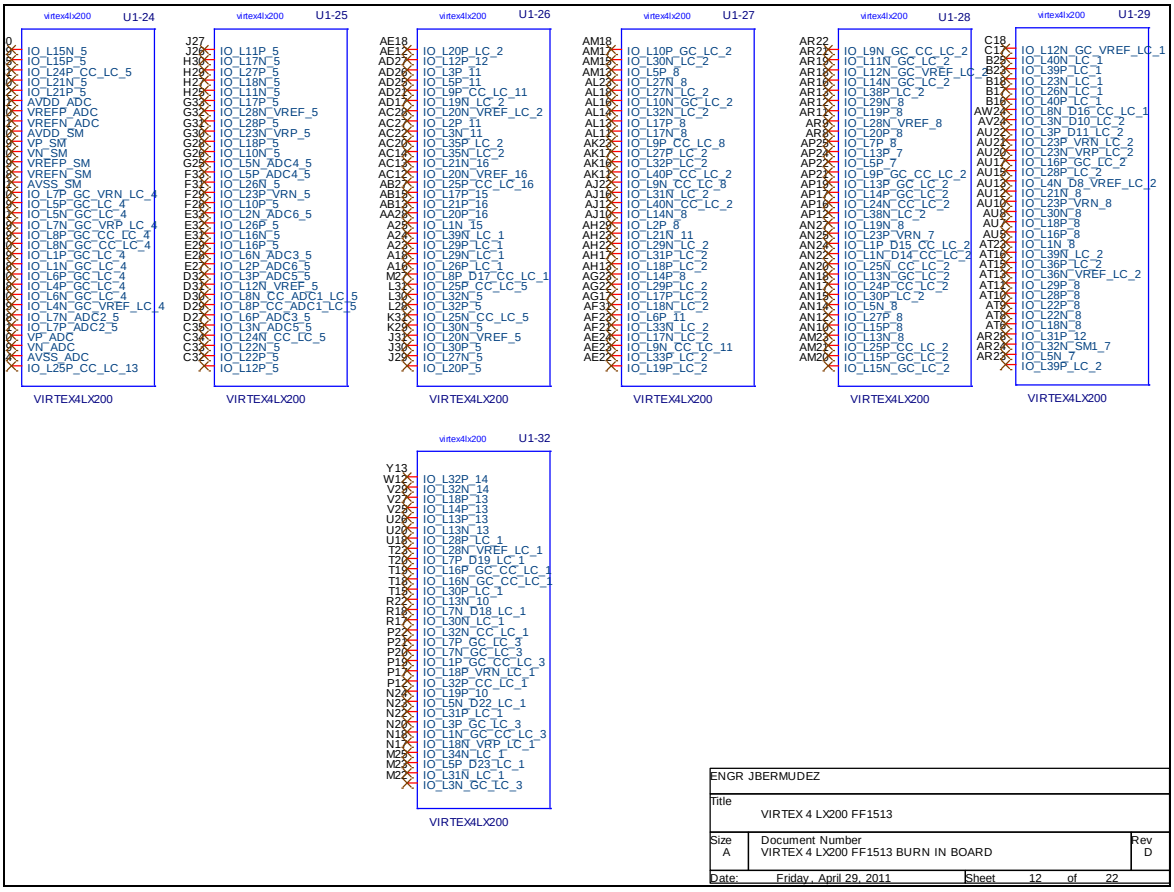
3.2.8.2 Power Interface

The following schematic is related to the Circuit Element Power Interface.



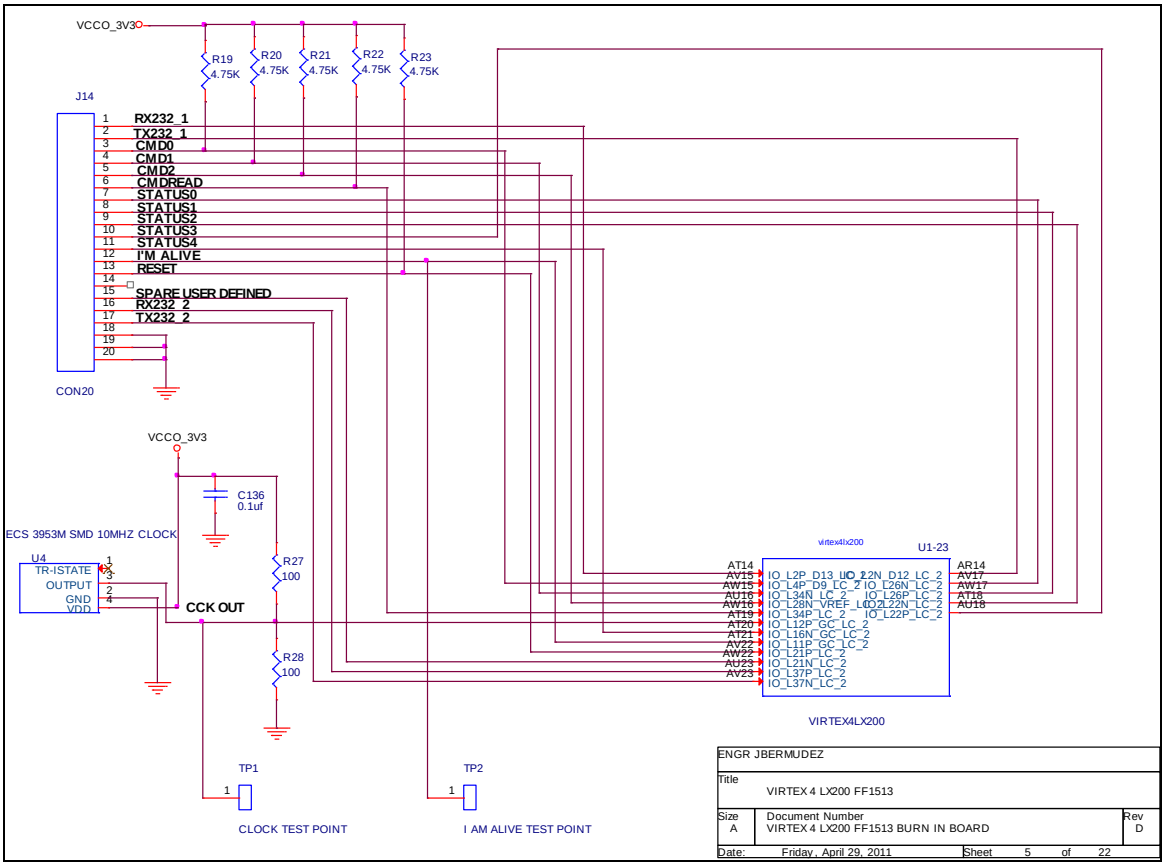
3.2.8.3 No Connects

The following schematic shows the Circuit Element NO CONNECT I/O.



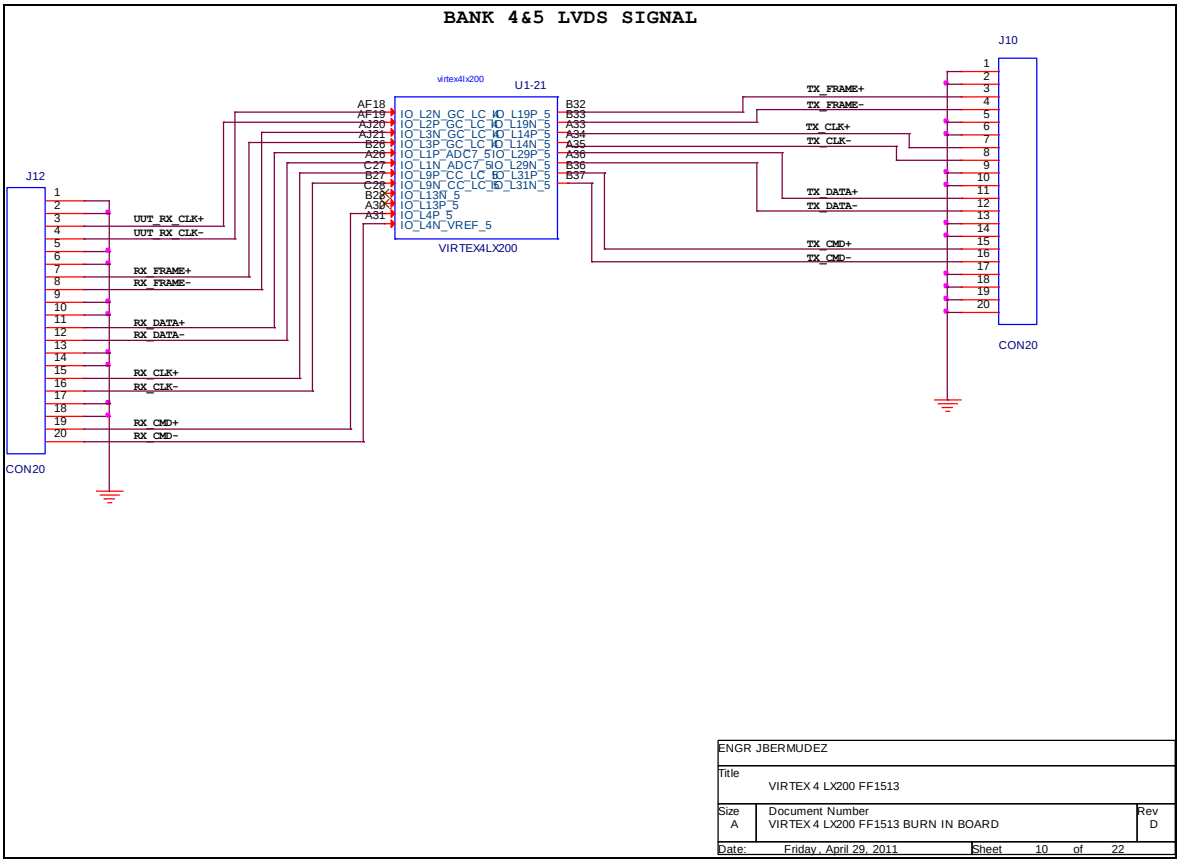
3.2.8.4 Test Interface

The following schematic is the Circuit Element Test Interface.



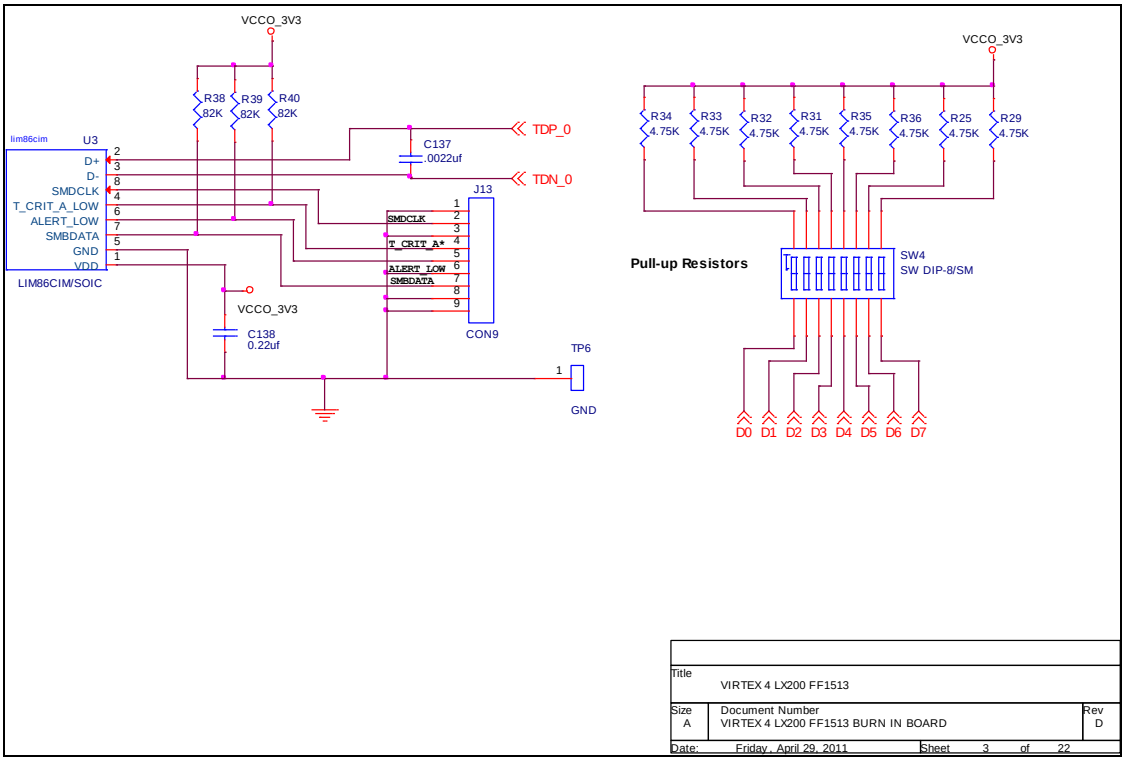
3.2.8.5 LVDS Interface

The following schematic sheet is the LVDS interface to the ML410 Virtex4 FX60 PWA.



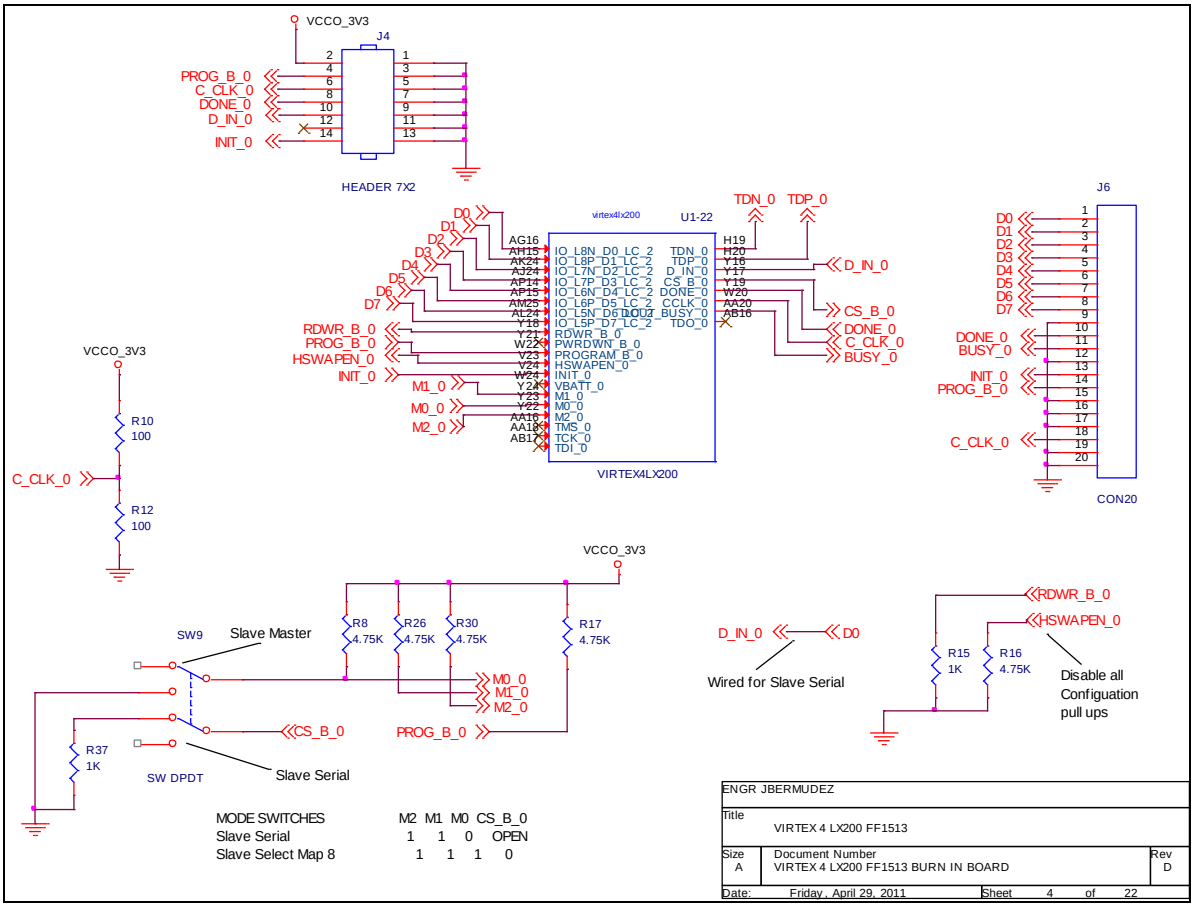
3.2.8.6 Temperature Sensor Interface

The following schematic is the Circuit Element sensor interface.



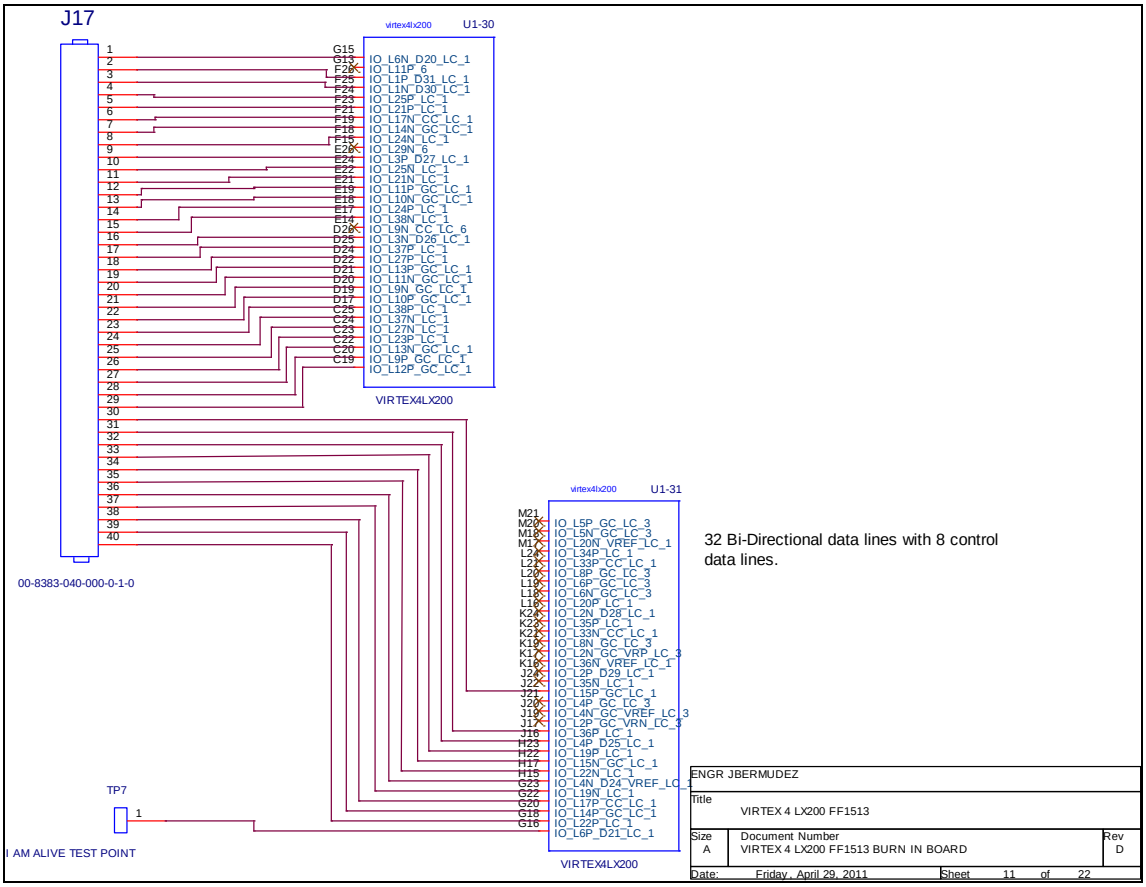
3.2.8.7 Configuration Interface

The following schematic shows the Circuit Element configuration interface.



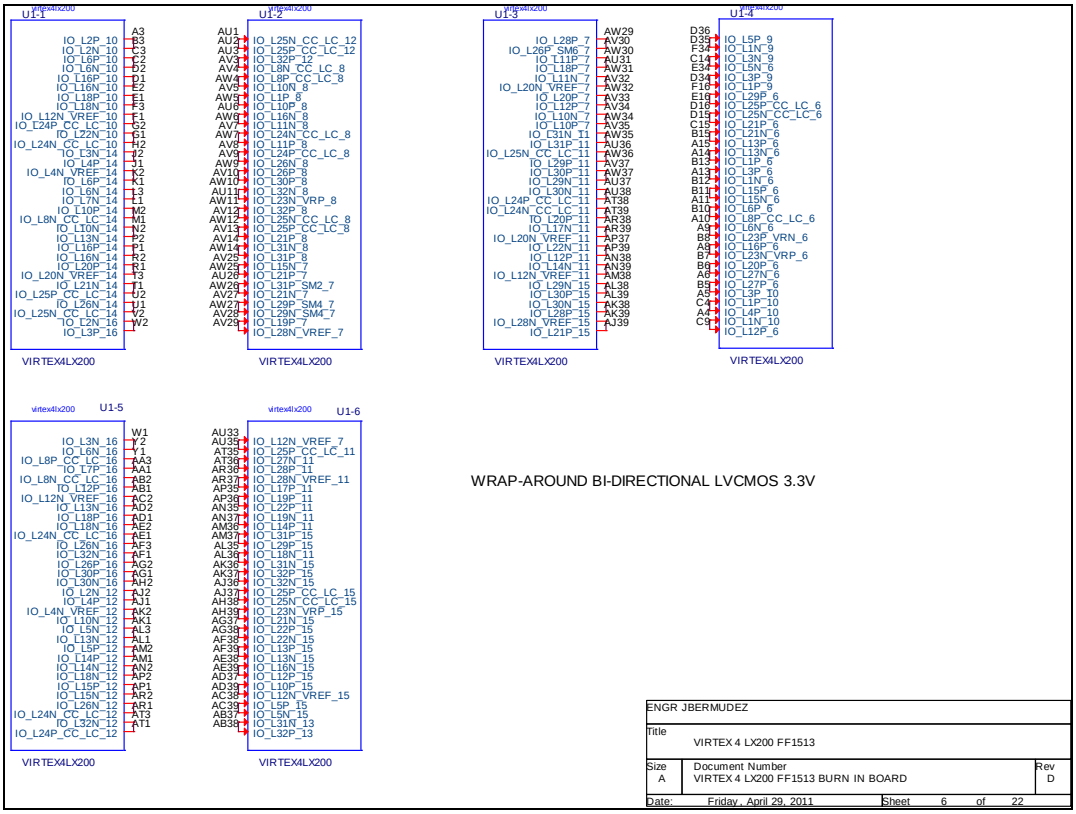
3.2.8.8 Bidirectional and Control Data Signals

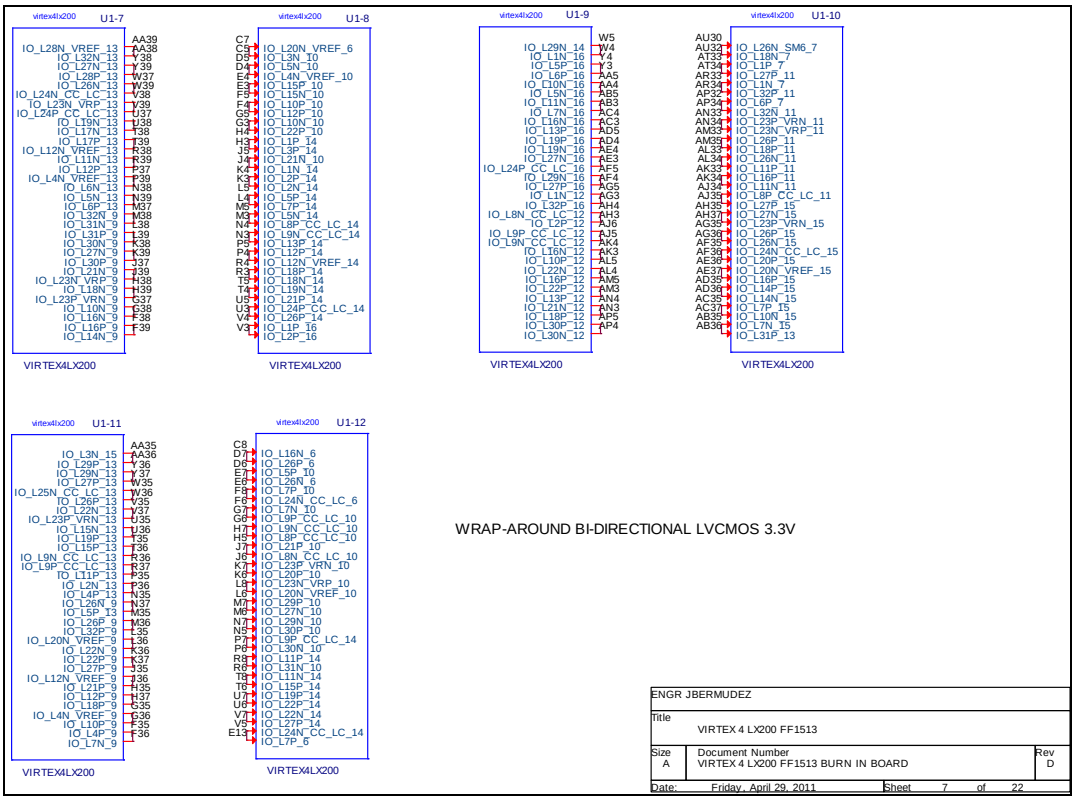
The following schematic is the bidirectional and control data signals.



3.2.8.9 Wrap Around IO

The following schematics display the hardware hook-up for the wrap around I/O.




U1-7
U1-8
U1-9
U1-10
U1-11
U1-12
VIRTEX4LX200
WRAP-AROUND BI-DIRECTIONAL LVCMOS 3.3V
ENGR JBERMUDEZ
Title
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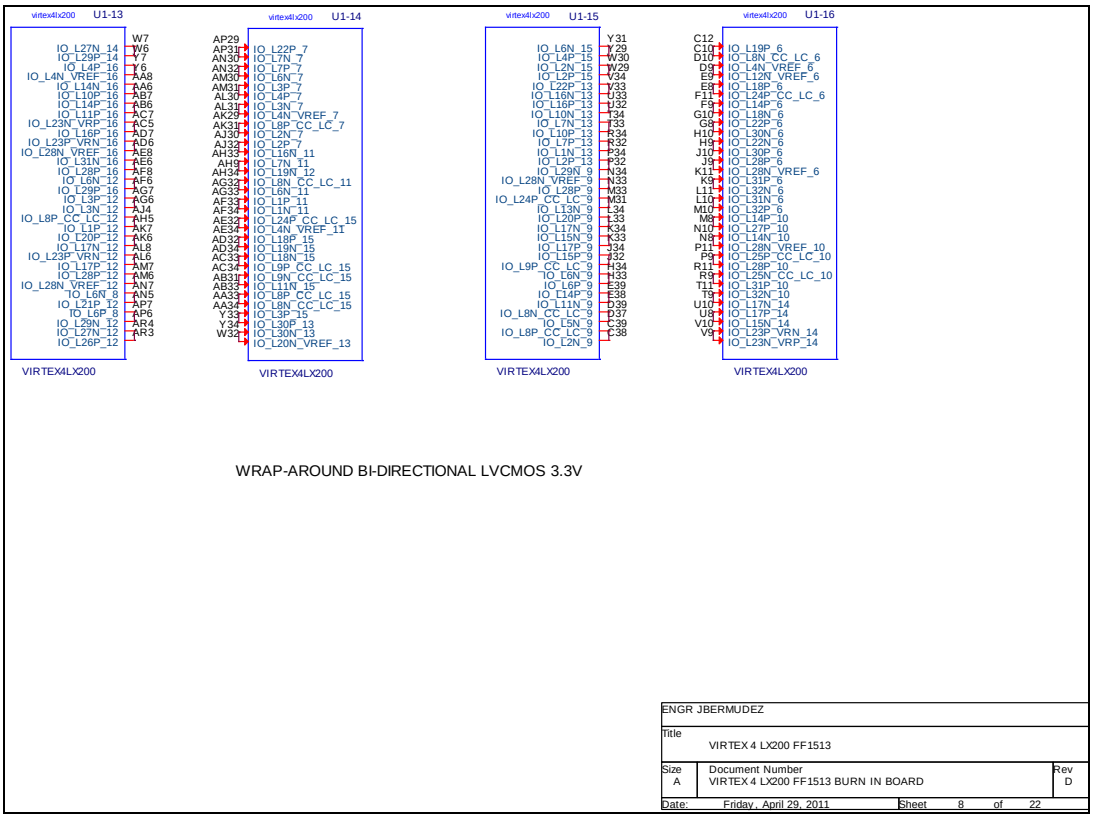
U1-13
U1-14
U1-15
U1-16
VIRTEX4LX200
WRAP-AROUND BI-DIRECTIONAL LVCMOS 3.3V
ENGR JBERMUDEZ
Title
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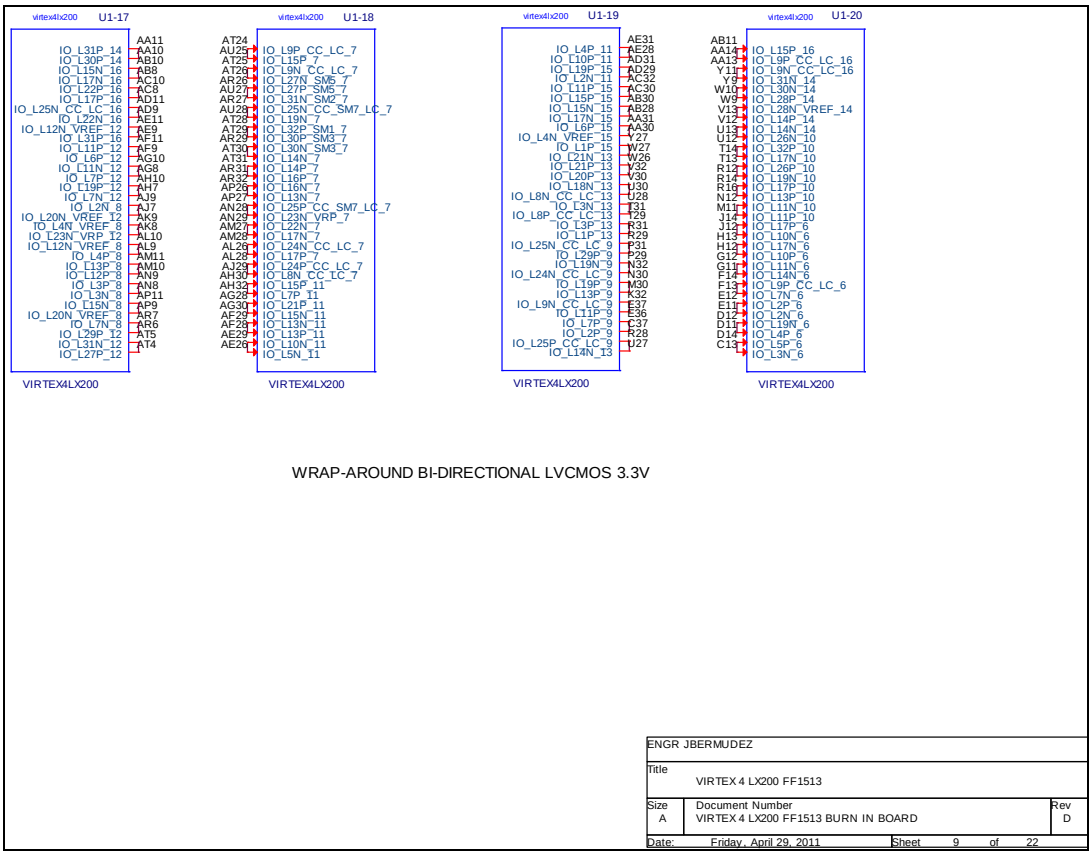
virtex4lx200 U1-17
IO_L31P_14 AA11
IO_L30P_14 AA10
IO_L15N_16 AB10
IO_L17N_16 AB8
IO_L22P_16 AC10
IO_L17P_16 AC8
IO_L25N_CC_LC_16 AD11
IO_L22N_16 AD9
IO_L12N_VREF_12 AE11
IO_L31P_16 AE9
IO_L11P_12 AF11
IO_L6P_12 AF9
IO_L11N_12 AG10
IO_L7P_12 AG8
IO_L19P_12 AH10
IO_L7N_12 AH7
IO_L2N_8 AJ9
IO_L20N_VREF_12 AJ7
IO_L4N_VREF_8 AK9
IO_L23N_VRP_12 AK8
IO_L12N_VREF_8 AL10
IO_L4P_8 AL9
IO_L13P_8 AM11
IO_L12P_8 AM10
IO_L3P_8 AN9
IO_L3N_8 AN8
IO_L15N_8 AP11
IO_L20N_VREF_8 AP9
IO_L7N_8 AR7
IO_L29P_12 AR6
IO_L31N_12 AT5
IO_L27P_12 AT4
VIRTEX4LX200
virtex4lx200 U1-18
AT24 IO_L9P_CC_LC_7
AU25 IO_L15P_7
AT25 IO_L9N_CC_LC_7
AT26 IO_L27N_SM5_7
AR26 IO_L27P_SM5_7
AU27 IO_L31N_SM2_7
AR27 IO_L25N_CC_SM7_LC_7
AU28 IO_L19N_7
AT28 IO_L32P_SM1_7
AT29 IO_L30P_SM3_7
AR29 IO_L30N_SM3_7
AT30 IO_L14N_7
AT31 IO_L14P_7
AR31 IO_L16P_7
AR32 IO_L16N_7
AP26 IO_L13N_7
AP27 IO_L25P_CC_SM7_LC_7
AN28 IO_L23N_VRP_7
AN29 IO_L22N_7
AM27 IO_L17N_7
AM28 IO_L24N_CC_LC_7
AL26 IO_L17P_7
AL28 IO_L24P_CC_LC_7
AJ29 IO_L8N_CC_LC_7
AH30 IO_L15P_11
AH32 IO_L7P_11
AG28 IO_L21P_11
AG30 IO_L15N_11
AF29 IO_L13N_11
AF28 IO_L13P_11
AE29 IO_L10N_11
AE26 IO_L5N_11
VIRTEX4LX200
virtex4lx200 U1-19
IO_L4P_11 AE31
IO_L10P_11 AE28
IO_L19P_15 AD31
IO_L2N_11 AD29
IO_L11P_15 AC32
IO_L15P_15 AC30
IO_L15N_15 AB30
IO_L17N_15 AB28
IO_L6P_15 AA31
IO_L4N_VREF_15 AA30
IO_L1P_15 Y27
IO_L21N_13 W27
IO_L21P_13 W26
IO_L20P_13 V32
IO_L18N_13 V30
IO_L8N_CC_LC_13 U30
IO_L3N_13 U28
IO_L8P_CC_LC_13 T31
IO_L3P_13 T29
IO_L1P_13 R31
IO_L25N_CC_LC_9 R29
IO_L29P_9 P31
IO_L19N_9 P29
IO_L24N_CC_LC_9 N32
IO_L19P_9 N30
IO_L13P_9 M30
IO_L9N_CC_LC_9 K32
IO_L11P_9 E37
IO_L7P_9 E36
IO_L2P_9 C37
IO_L25P_CC_LC_9 R28
IO_L14N_13 U27
VIRTEX4LX200
virtex4lx200 U1-20
AB11 IO_L15P_16
AA14 IO_L9P_CC_LC_16
AA13 IO_L9N_CC_LC_16
Y11 IO_L31N_14
Y9 IO_L30N_14
W10 IO_L28P_14
W9 IO_L28N_VREF_14
V13 IO_L14P_14
V12 IO_L14N_14
U13 IO_L26N_10
U12 IO_L32P_10
T14 IO_L17N_10
T13 IO_L26P_10
R12 IO_L19N_10
R14 IO_L17P_10
R16 IO_L13P_10
N12 IO_L11N_10
M11 IO_L11P_10
J14 IO_L17P_6
J12 IO_L10N_6
H13 IO_L17N_6
H12 IO_L10P_6
G12 IO_L11N_6
G11 IO_L14N_6
F14 IO_L9P_CC_LC_6
F13 IO_L7N_6
E12 IO_L2P_6
E11 IO_L2N_6
D12 IO_L19N_6
D11 IO_L4P_6
D14 IO_L5P_6
C13 IO_L3N_6
VIRTEX4LX200
WRAP-AROUND BI-DIRECTIONAL LVCMOS 3.3V
ENGR JBERMUDEZ
Title
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3.3 Parts List

The following is the parts list:

Table VIII. Parts List

Item	Type	Manufacturer	Name	Part#	Quantity	Part	Reference
1	Capacitor	AVX	CAP CER 2200PF 25V X7R 0306	03063C222KAT9A	1	.0022uf	C2
2	Capacitor	AVX	0.022 uF X7R 0402 Cap	04026C223KAT2A	138	0.022uf	C3,C4,C5,C8,C9,C10,C11, C12,C13,C14,C15,C16,C17, C18,C19,C20,C21,C32,C33, C34,C35,C36,C37,C38,C39, C40,C41,C42,C43,C44,C45, C56,C59,C60,C61,C62,C63, C64,C65,C66,C67,C68,C69, C70,C80,C81,C82,C83,C84, C85,C86,C87,C88,C95,C97, C98,C99,C100,C101,C102, C103,C104,C105,C113,C114, C115,C116,C117,C118,C119, C120,C121,C146,C147,C148, C149,C150,C151,C152,C153, C154,C155,C162,C163,C164, C165,C166,C167,C168,C169, C170,C171,C181,C182,C183, C184,C185,C186,C187,C188, C189,C197,C198,C199,C200, C201,C202,C203,C204,C205, C206,C215,C216,C217,C218, C219,C220,C221,C222,C223, C229,C230,C231,C232,C233, C234,C235,C236,C237,C243, C244,C245,C246,C247,C248, C249,C250,C251
3	Capacitor	AVX	0.22 uF X7R 0603 Cap	06036C224KAT2A	71	0.22uf	C6,C22,C23,C24,C25,C26, C27,C28,C46,C47,C48,C49, C50,C51,C52,C57,C71,C72, C73,C74,C75,C78,C89,C90, C91,C92,C93,C106,C107, C108,C109,C122,C123,C124, C125,C126,C145,C156,C157, C158,C159,C172,C173,C174, C175,C176,C190,C191,C192, C193,C194,C207,C208,C209, C210,C212,C224,C225,C226, C227,C228,C238,C239,C240, C241,C242,C252,C253,C254, C255,C256
4	Capacitor	AVX	2.2 uF X7R 0805 Cap	08056C225KAT2A	35	2.2uf	C7,C29,C30,C31,C53,C54, C55,C58,C76,C77,C79,C94, C96,C110,C111,C112,C128, C129,C130,C131,C132,C133, C134,C135,C160,C161,C177, C178,C179,C180,C195,C196, C211,C213,C214
5	Capacitor	AVX	CAP CER .10UF 6.3V X7R 0603	06036C104JAT2A	95	0.1uf	C127,C136,C265,C266,C267, C268,C279,C280,C281,C282,

Item	Type	Manufacturer	Name	Part#	Quantity	Part	Reference
							C293,C294,C295,C296,C307, C308,C309,C310,C321,C322, C323,C324,C327,C328,C329, C340,C341,C342,C343,C354, C355,C356,C357,C368,C369, C370,C371,C382,C383,C384, C385,C396,C405,C406,C407, C408,C419,C420,C421,C422, C433,C434,C435,C436,C447, C448,C449,C450,C461,C462, C463,C464,C536,C537,C538, C539,C540,C541,C542,C543, C544,C545,C546,C547,C548, C549,C550,C551,C552,C573, C574,C575,C576,C577,C579, C607,C608,C609,C610,C621, C622,C623,C624,C630,C632
6	Capacitor	AVX	CAP CER 10000PF 6.3V X7R 0402	04026C103KA72A	186	0.01uf	C257,C258,C259,C260,C261, C262,C263,C264,C271,C272, C273,C274,C275,C276,C277, C278,C285,C286,C287,C288, C289,C290,C291,C292,C299, C300,C301,C302,C303,C304, C305,C306,C313,C314,C315, C316,C317,C318,C319,C320, C332,C333,C334,C335,C336, C337,C338,C339,C346,C347, C348,C349,C350,C351,C352, C353,C360,C361,C362,C363, C364,C365,C366,C367,C374, C375,C376,C377,C378,C379, C380,C381,C388,C389,C390, C391,C392,C393,C394,C395, C397,C398,C399,C400,C401, C402,C403,C404,C411,C412, C413,C414,C415,C416,C417, C418,C425,C426,C427,C428, C429,C430,C431,C432,C439, C440,C441,C442,C443,C444, C445,C446,C453,C454,C455, C456,C457,C458,C459,C460, C502,C503,C504,C505,C506, C507,C508,C509,C510,C511, C512,C513,C514,C515,C516, C517,C518,C519,C520,C521, C522,C523,C524,C525,C526, C527,C528,C529,C530,C531, C532,C533,C534,C535,C560, C561,C563,C564,C565,C566, C567,C568,C569,C570,C571, C572,C587,C588,C589,C602, C603,C604,C605,C606,C613, C614,C615,C616,C617,C618,

Item	Type	Manufacturer	Name	Part#	Quantity	Part	Reference
							C619,C620,C627,C628,C629, C631
7	Capacitor	AVX	CAP CER 1.0UF 6.3V X7R 0805	08056C105MAT2A	46	1.0uf	C269,C270,C283,C284,C297, C298,C311,C312,C325,C326, C330,C331,C344,C345,C358, C359,C372,C373,C386,C387, C409,C410,C423,C424,C437, C438,C451,C452,C465,C466, C553,C554,C555,C556,C557, C558,C559,C562,C578,C580, C581,C611,C612,C625,C626, C633
8	Capacitor	AVX	CAP TANTALUM 47UF 6.3V 10% SMD	TAJB476K006RNJ	13	47uF	C582,C583,C584,C585,C590, C591,C592,C594,C595,C596, C598,C599,C600
9	Capacitor	AVX	CAP TANT LOESR 470UF 6.3V 10%SMD	TPME477K006R0018	4	470uF	C586,C593,C597,C601
10	Connector	FCI	CONN RECEPT 14POS DUAL SMD		1	HEADER 7X2	J4
11	Connector	Molex Connector Corporation	CONN RECEPT 20POS 1MM DUAL SMD	52365-2091	4	CON20	J6,J10,J12,J14
12	Connector	3M	CONN SOCKET SGL 9POS GOLD SMD	963109-2000-AR-TP	1	CON9	J11
13	Connector	SamTec Inc	CONN HEADER 8POS DUAL 2MM SMD	TMM-104-01-T-D-SM	1	HEADER 4X2	J13
14	Resisitor	Stackpole Electronics Inc	RES 4.75K OHM 1/4W 1% 1206 SMD	RMCF1206FT4K75	20	4.75K	R2,R3,R4,R8,R9,R10, R11,R12,R13,R14,R15, R16,R17,R18,R19, R20,R21,R22, R23,R26
15	Resisitor	Stackpole Electronics Inc	RES 1K OHM 1/4W 5% 1206 SMD	RMCF1206JT1K00	2	1K	R5,R6
16	Resisitor	Stackpole Electronics Inc	RES 330 OHM 1/4W 5% 1206 SMD	RMCF1206JT330R	1	330	R7
17	Resisitor	Stackpole Electronics Inc	RES 100 OHM 1/4W 1% 0805 SMD	RNCP0805FTD100R	2	100	R24,R25
18	FPGA	Xilinx Inc	IC FPGA VIRTEX-4LX 200K 1513FBGA	XC4VLX200-10FFG1513I	1	VIRTEX4LX200	U1
19	Temperature Sensor	National Semiconductor	LM86CIMM/NOPB	LM86CIMM/NOPB	1	LIM86CIM/SOIC	U2
20	Oscillator	Maxim Integrated Products	IC OSCILLATOR SIL SC70-3	MAX7375AXR425+T	1	MAX7375	U3

3.4 Software Interface

3.4.1 UART Protocol

The circuit design requires for an asynchronous UART implementation where data can be transmitted without a clock. Per protocol, a ZERO will be used as a "Start Bit" and ONE as an "STOP bit" and 8 bits of data in between.

After the Start Bit is sent, the individual bits of the word of data are sent, with the Least Significant Bit (LSB) being sent first. Each bit in the transmission is transmitted for exactly the same amount of time as all of the other bits. When the entire data word has been sent, the Stop bit is sent by the transmitter.

A parity bit could be sent on the transmission, and may be used by the receiver to perform simple error checking. This is not currently implemented in this design but it can be added later on if needed.

If the Stop Bit does not appear when it is supposed to, the UART considers the entire word to be garbled and will report a Framing Error to the host processor when the data word is read. The usual cause of a Framing Error is that the sender and receiver clocks were not running at the same speed, or that the signal was interrupted.

3.4.2 Command Structure

Software will interface with the Burn-in board via the serial communication port RS-232. The command structure consists of a minimum of 4 eight bit words. The Start word shall be set to 0x66 followed by the command word and immediately followed by the data word. To end the transmission after the last data word has been transmitted, the END WORD shall be transmitted with the characters 0xE7, which indicates that it is the last word transmitted. This protocol shall be followed for the command structure.

Table IX. Receive Data Structure

Start Word		Command Word								Data Word		End Word	
		RDWR_n	Test Type			Test Sub Type							
bit 7:4	bit 3:0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit 7:4	bit 3:0	bit 7:4	bit 3:0
6	6	x	x	x	x	x	x	x	x	xxxx	xxxx	E	7

3.4.2.1 Read and Write

Bit 7 shall be set to ONE if the command word indicates a READ command and it shall be set to ZERO if the command word indicates a WRITE command.

Table X. Read and Write bit

RDWR_n	bit7
WRITE	0
READ	1

3.4.2.2 Test Type

Bits 6 down to 4 are allocated for Test Type as shown in the following table:
If selected bits are equal to 1, then it is a Block RAM test, 2 is a DSP test and 3 is a DIO test.

Table XI. Test Type

Test Type	bit6	bit5	bit4
Test in Progress(RD)	0	0	0
RAM Block	0	0	1
DSP	0	1	0
IO Wrap	0	1	1
TBD	1	0	0
TBD	1	0	1
TBD	1	1	0
TBD	1	1	1

3.4.2.3 Test Sub-type

Bits 3, 2, 1 and 0 are use in the selection of the test subtype.

Table XII. Test Sub-Type

Test Sub Type	Test Sub Type	Test Sub Type				
IO Wrap-around	DSP	Block RAM & IO	bit3	bit2	bit1	bit0
Select	ADD	1x16K	0	0	0	0
	SUBTRACT	2x8K	0	0	0	1
	MULTIPLY	4x4K	0	0	1	0
	DIVIDE	9x2K	0	0	1	1

3.4.3 Status Structure

The Status is what the UUT sends to the PC at the conclusion of a test. The starting and end words are different that the ones used on the command structure. Also the RDWR_n is always set to zero. The rest of the words in the Status Word Structure follow the same configuration as the command structure.

Table XIII. Transmit Data Structure

		Status Word											
Start Word		RDWR_n	Test Type			Test Sub Type				Data Word		End Word	
bit 7:4	bit 3:0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit 7:4	bit 3:0	bit 7:4	bit 3:0
A	B	x	x	x	x	x	x	x	x	xxxx	xxxx	C	D

3.4.4 Baud Rate

The requirements specification states that the baud rate to be used on this implementation shall be 9600 bps.

Chapter 4 : Design Verification

Verification of this circuit is done following the test procedures of a VHDL implementation circuit design.
All logic blocks have been simulated and a loop back test was executed to verify the functionality of the receiver and the transmitter in a stand-alone basis.
No design verification has been done at the integration level at this point.

This circuit is broken down in several logic circuit blocks. The design verification is done in two steps. The first step is done for each one of the logic blocks independently and the second for all the circuit blocks interconnected.
The hierarchical tree of the circuit implementation is shown below

- V4LX200_TOP.VHD
  - UART_BAUD_GEN.VHD
  - UART_RX_CTL.VHD
  - UART_TX_CTL.VHD
  - LB_CTL.VHD
  - SERIAL_DATA_MEM_2KX8.VHD
  - RX_CMD_PARSER.VHD
  - XMITR_FIFO.VHD
  - 1X16K_BRAM_TEST.VHD
    - BRAM_1X16K.VHD
  - 2X8K_BRAM_TEST.VHD
    - BRAM_2X8K.VHD
  - 4X4K_BRAM_TEST.VHD
    - BRAM_4X4K.VHD
  - 8X2K_BRAM_TEST.VHD
    - BRAM_8X2K.VHD
  - ADD_TEST.VHD
    - ADD_16X16.VHD
  - SUB_TEST.VHD
    - SUB_16X16.VHD
  - MULT_TEST.VHD
    - MULT_16X16.VHD
  - DIV_TEST.VHD
    - DIV_16X16.VHD
  - TBD_TEST.VHD
    - TBD.VHD

Table XIV. Verification Matrix

Requirement		Verification Method			Comments
Number	**Title**	**Analysis**	**Simulation**	**Test**	
3.2.1.	Input Signals	X	X	X	
3.2.2	Output Signals	X	X	X	
3.2.3	Bidirectional Signals	X	X	X	
3.2.4	Power Supply	X		X	
3.2.5	ESD Protection			X	
3.2.6	EMI			X	
3.4.1	Interface Connector	X	X	X	
3.4.2	Baud Rate Generator	X	X	X	
3.4.3	UART	X	X	X	
3.4.3.1	Receiver	X	X	X	
3.4.3.2	Transmitter	X	X	X	
3.4.4	Test Process	X	X	X	
3.4.4.1	Test Vector Decode	X	X	X	
3.4.4.2	Test Vector Results Encode	X	X	X	
3.4.5	Discrete I/O Processing	X	X	X	
3.4.5.1	Discrete Input Data	X	X	X	
3.4.5.2	Discrete Output Data	X	X	X	

4.1 Analysis & Simulation

The source code, circuit simulation, timing analysis, implementation constrains along with circuit programming located at the end of this document on the Appendix section.
An electronic copy of the source code and programming file will be part of the release of this document.

4.2 Test

The following test subsets have been implemented by integrating this circuit with adapter board and the PC containing the Test command software.

4.2.1 Receive (RX) Test

This section will be updated upon design integration

4.2.2 Transmit (TX) Test

This section will be updated upon design integration

4.2.3 Test Vector Execution

This section will be updated upon design integration

Chapter 5 Test Requirements

5.1 Design Verification Test

5.1.1 Baud rate

This test will verify the baud rate. No data at this time. Verify during integration.

5.1.2 Word bit allocation

This test will validate the order of how the bit are placed in the received word and the transmit word

5.1.3 Command Data Structure

This test will verify the command data structure of the received command and the transmit status word.

5.1.4 Test Vector

The verification of the test vector results will be done at the PC side. The golden copy will be tested against the test result to verify the device under temperature stress.

5.2 In-Circuit Test

None.

Chapter 6 Packaging and Layout Requirements

The implementation of this circuit is by utilizing the XILINX XCV4LX200-10FFG1531I. The layout of the PWA has been done by another engineer taking in consideration the signal to pin allocation in such a way to mitigate simultaneous sequential switching output noise, the clock input has been selected to have it in a global input so the clock could be distributed across the circuit with minimum fan-out and skew issues.

Chapter 7 : Conclusion and Future Enhancements

7.1 Conclusion

The test verification proofs the design implementation. All requirements have been met and the logic implementation of the design is programmed in a FPGA
Further verification can be accomplished during integration to verify the hardware and software interface. By the conclusion of this report we were limited with budget constrains to verify the final step.

7.2 Future Enhancements

The current design features meet all the design requirements and provides the means to test components in the UUT, however there may be ways to improve the system design:

- Substituting the clock speed to higher frequencies will allow the use of the PLL function for clock generation that could be use for different baud rates. For this part the minimum clock to use PLL is above 33 MHz.
- Implementing more test to fully check all the features of the UUT.
- Synchronous interface will make an easier design implementation.

References

1. UG070 (v2.6), Virtex 4 FPGA User Guide from Xilinx.
2. Arbitrary Programmable Wave Generator w/ RS-232 UART Interface Sample project from the Xilinx ISE Design Suite.
3. HDL Chip Design. A Practical Guide for Designing, Synthesizing and Simulating ASIC and FPGAs using VHDL or Verilog by Douglas J. Smith.
4. RTL Hardware Design Using VHDL: Coding for Efficiency, Portability and Scalability by Pong P. Chu.