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Simulation of optically controlled GaN (Gallium Nitride) using analytical modeling of high frequency response and switching applications

A graduate project submitted in partial fulfillment of the requirements

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in Electrical Engineering.

By

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ABSTRACT

SIMULATION OF OPTICALLY CONTROLLED GALLIUM NITRIDE MESFET USING ANALYTICAL MODELING (MATLAB SOFTWARE) FOR HIGH FREQUENCY RESPONSE AND SWITCHING APPLICATIONS.

By

Naynesh Shah

Masters of Science in Electrical Engineering

In this project, an analytical modeling of optically controlled Gallium Nitride has been presented here for an analysis of extrinsic and intrinsic parameters such as, gate capacitances including both of the gate-source capacitances, gate-drain capacitances and switching speed under dark and illumination conditions. Different fabrication parameters such as ion dose, ion energy and ion range parameters, channel length and active channel depth has been incorporated in the model to understand the better effect of device performance at the dark intensity and illumination conditions. The switching speed of the device has been studied by changing the active channel depth, gate length and other electrical and fabrications parameters influenced by the dark and illumination conditions.

CHAPTER 1

1. Introduction:

GaN has become an attractive material for power transistors due to its wide band gap, high breakdown electric field strength, and high thermal conductivity. Also the material has a relatively high electron saturation drift velocity and low relative permittivity, implying potential for high frequency performance. Due to its wide band gap, GaN is a primary candidate for optoelectronic devices operating with blue to ultraviolet wavelengths and electronic devices operating at high temperatures and high power levels. Several GaN-based transistors, superlattices, and quantum well devices intended for both electronic and optoelectronic applications. Improved electron transport properties are one of the main targets in the ongoing study of GaN material and devices. It is considered reasonably well established that the electron drift velocity dependence on electric field has a region of negative differential conductivity [1].

The ability of Gallium Nitride (GaN) MESFET to operate over a wide temperature range requires accurate models to simulate the temperature dependence of various device parameters. This is a new temperature dependent analytical model for the threshold voltage of GaN MESFETs is introduced. The contributions from various temperature dependent material parameters are taken into account in order to develop an accurate I-V model along with the effect of gate leakage current on the threshold voltage of the device. The model is further extended to predict the temperature dependence of transconductance. The model shows excellent agreement with the published experimental results for a 0.25μm device [2].

An analytical model is proposed for an optically controlled Metal Semiconductor Field Effect Transistor (MESFET), known as Optical Field Effect Transistor (OPFET) considering the diffusion fabrication process. The electrical parameters such as threshold voltage, drain-source current, gate capacitances and switching response have been determined for the dark and various illuminated conditions. The Photovoltaic effect due to photogenerated carriers under illumination is shown to modulate the channel cross-section, which in turn significantly changes the threshold voltage, drain-source current, the gate capacitances and the device switching speed. Further the results show significant increase

in gate-source capacitance Cgs and gate-drain capacitance Cgd for optical illuminations, where the photo-induced voltage has a significant role on gate capacitances. The switching time τ of the OPFET device is computed for dark and illumination conditions. The switching time τ is greatly reduced by optical illumination and is also a function of device active layer thickness and corresponding impurity flux density QDiff. Thus it is shown that the diffusion process shows great potential for improvement of optoelectronic devices in quantum efficiency and other performance areas [3].

A perturbation technique is used to develop a more accurate model of the time varying characteristics of the optically illuminated ion-implanted metal semiconductor field-effect transistor (MESFET) OPFET. In this model, the carrier life time is considered as a function of the carrier concentration in the channel. The carrier concentration in the active channel is altered due to the absorption of the incident light, which affects the carrier life time. The influences of this effect on the device parameters and characteristics is studied and analyzed. Based on this model the current voltage characteristics, the gate-source capacitance, and the threshold voltage of the OPFET have been evaluated for different incident light power intensities. This model shows comparable results to other reported models [4].

The analytical modeling has been developed based on device physics to study the gate-source capacitance, gate-drain capacitance, transconductance of GaN MESFET to evaluate the cut-off frequency. The results of those intrinsic parameters such as gate-to-source capacitance and gate-to-source capacitance and transconductance indicate the excellent potential of the device for high frequency amplifier application for space and device communication. This excellent feature also allows this device to be applied in the field of communication in high temperature environment [5].

Wide bandgap GaN has long been sought for its applications to blue and UV emitters and high temperature high power electronic devices. GaN based electronic devices such as high power and heat tolerant heterojunction bipolar transistors (HBT's) can be important components of integrated systems designed for high frequency and high speed applications, for example, in satellites and all electric aircraft. GaN based field-effect

transistors (FET's) are projected to be highly useful for power amplification and switching in high temperature and high power environment. [6]

GaN based FET structures offer the potential of high speed, high frequency, high power and high temperature operation beyond that of Si and GaAs. Theoretical considerations concerning FETs predict an output power density in the range of 20W/mm, with a power density above 6 W/mm being obtained at three laboratories (Cree, Nitres, HRL) and 9.8 W/mm being the present record. Such high power densities may result in high channel temperatures and the thermal stability of the structure becomes important as well as the thermal management. Indicative for the thermal stability may be the materials Debye-temperature, which is approx. 750°C in the case of GaN [7].

In spite of this extensive experimental work there is still a lack in reliable device simulation and modeling of GaN-based electron devices. The device simulation models extend from the most general, fundamental physics based microscopic Monte Carlo (MC) approach to rather simple analytical (or charge control) methods, which incorporate the results of microscopic description of the electronic band structure and carrier transport in external electric field. It is worth mentioning that the drift-diffusion approach frequently needs input information such as low and high electric field mobility, which can be provided only by the microscopic investigation, i.e., by Monte Carlo carrier transport modeling. However, the lack of experimental data results in a high degree of uncertainty in the calculated conduction/valence band structure and electron/hole scattering rates [8].

1.1 Optically controlled MESFET (OPFET)

The optically-controlled MESFET (or OPFET) is of great importance because of its potential as a photo detector and pre-amplifier, r.f. switch and optically controlled actuator, etc. Different mechanisms which are responsible for the enhanced terminal properties of the optically-controlled MESFET are: 1) photo generated carriers below the gate [9], [10], 2) photo-induced voltage across the Schottky barrier [11], [12], and 3) photo conductivity effect in the source-gate and drain-gate regions and the change in the gate depletion width [13]. Further, the experimental observation [14] showed a positive voltage across the depletion region between the n-type channel and the semi-insulating substrate suggesting that the drain current enhancement is closely related to the channel width modulation of the device.

The first theoretical work on the optically-controlled ion implanted silicon MESFET reported by Singh [15] used photo generated carriers below the gate due to optical absorption through a transparent/semitransparent Schottky gate. An ion-implanted profile has been chosen because of its superior performance over other profiles as shown theoretically by Chattopadhyay and Pal [16].

Owing to the direct wide bandgap of GaN and the ease of fabrication and amenability to large-scale integration of metal semiconductor field effect transistors (MESFETs) the optical behavior of GaN MESFET is a matter of great interest. Optically biased GaN MESFET can effectively be used to realize high-power optoelectronic detectors and amplifiers to achieve high-performance standards at micro-wave frequencies and elevated temperatures. It also true that GaN has been viewed as a suitable material for optoelectronic applications such as blue/green LEDs, short wavelength lasers, and highly responsive, visible-blind UV photodetectors. It is observed that light of wavelength 0.3μm which is closer to cut-off wavelength (0.362μm) is suitable for optically biasing the GaN MESFET for optical results. The radiation enters the device through the semitransparent gate~90% and the spacing between the gate, drain, and source. Electron-hole pairs are thus generated, which widen the channel and decrease the parasitic resistances, hence elevating the device performance. The gate length modulation and photovoltaic effect are considered, along with the illumination dependence of the parasitic resistances and fringing charge, which lead to significant improvements in channel current, transconductance, and cut-off frequency of the device [17].

1.2 Defects in a bulk GaN:

Bulk GaN crystals of the wurtzite structure were grown from a solution of atomic nitrogen in liquid gallium under high nitrogen pressure (up to20 kbars) at temperatures in the range 1500 -1800 K. GaN crystals of platelet shape were typically of 1-3 mm in lateral size and 0.1-0.5 mm in thickness. They often had the shape of elongated hexagons with the longest dimension along axis and the surfaces of the platelets parallel to c-plane. The two platelet faces differ in their roughness: one is almost atomically flat while the opposite one can be very rough. In some cases a series of inverted pyramids terminated

the rough surface. However, about 70-90% of the total plate thickness was defect-free [18].

The more rough the surface, the higher was the defect density observed. Formation of SFs is considered as a growth mistake. The structure of basal and prismatic faults in wurtzite has been described by Blank. From a crystallography point of view the basal faults are equivalent to local transitions from the hexagonal to the cubic structure within a few (0001) atomic planes. In hexagonal GaN the bonds have mirror symmetry while in the cubic structure bonds are rotated 60^0 with respect to nearest neighbors. The local change of crystal symmetry is from 2H to 3C. Each bilayer of the cubic GaN is situated in one of three possible positions assigned as A, B, C with the ideal stacking sequence of ... ABCABC ... while in hexagonal GaN each bilayer has only two possible positions, A and B, with the perfect sequence being ..ABABAB.. . SFs locally change the bond arrangement and introduce a number of atomic planes with the zinc-blende structure (ABC) in the wurtzite GaN (AB) [19].

Defects in epitaxial GaN crystals:

While stacking faults are the predominant defects in bulk GaN crystals, dislocations lying almost parallel to the c-axis dominate in epitaxial GaN layers. Dislocations in the epitaxial GaN often are arranged as a network of small angle boundaries forming the columnar structure typical for epitaxial layers of hexagonal materials. The difference in defects for bulk as compared to epitaxial crystals is associated with the totally different growth conditions. Indeed, epitaxial GaN layers grow in the c-direction on top of the substrate with a high lattice and thermal mismatch. Therefore, most defects in epitaxial GaN layers are generated at the interface and then propagate in the growth direction. Due to a high density of vertical dislocations and the c-axis growth direction, SFs in the epilayer cannot propagate for long distances as was observed in bulk crystals, the lengths of SFs in epitaxial GaN were much smaller than those in the bulk crystals [20].

Most of the dislocation interactions resulting in annihilation of dislocations happen near the interface where dislocation density is high and spacing between them are relatively small. Threading dislocations can propagate from the substrate or can be formed during coalescence of 3D islands during the initial stages of the GaN growth.

Therefore, a buffer layer might decrease the dislocation density in the GaN layer. A buffer layer can reduce the roughness of the substrate surface and prevent the detoriation of GaN at the interface due to outdiffusion of nitrogen into the substrate. An AlN buffer layer typically has a "mosaic" structure with a high density of defects. It contains small crystalline sub-grains slightly disoriented around the c-axis, but perfectly oriented in the c-plane. The structure of the buffer layer influences the arrangement of threading dislocations in the GaN layer resulting in the formation of a network of small angle boundaries with both tilt and twist components. Some of threading dislocations bend into the basal plane to become segments of misfit dislocations parallel to the interface [21].

1.3 Ion Implantation

The technique of ion implantation is extremely attractive for the fabrication of GaN and SiC based devices because it can introduce a well-defined impurity concentration at a designed zone. In fabrication of such GaN-based devices, ion implantation represents a very attractive tool for several technological steps, such as electrical and optical selective-area doping, dry etching, electrical isolation, quantum well intermixing, and ion-cut. It is well-known that a successful application of ion implantation depends on understanding the production and annealing for curing radiation damage. Thus, detailed studies of ion implantation damage in GaN are not only important for investigating fundamental defect processes in solids under ion implantation but are also essential for the fast developing GaN industry. Ion implantation is preferred because of controlled, low or high dose can be introduced (10^{11} -10^{18} cm^{-2}), depth of implant can be controlled and slow impurity diffusion can be activated by high temperature annealing. Ion implantation can independently control the dopant concentration, junction depth. It is a low temperature, PR mask and anisotropic dopant profile. Up to now, several outstanding reviews have appeared in the literature addressing various aspects of ion implantation into GaN. However, very recently, the field of ion implantation into GaN has matured considerably. Before implantation can become a viable technology for 111-nitrides, it is essential that implantation properties such as ion disorder and its removal by thermal annealing and the ability to electrically activate implanted dopants are studied in detail. Such studies have been limited until quite recently when Zolper showed that GaN could be activated both n-type and p-type by Si implantation. In addition, Tan showed that ion disorder built up rather slowly in GaN with increasing Si ion dose even at liquid nitrogen temperatures as a

result of dynamic recovery of disorder during implantation. However, it is possible to amorphise GaN at extremely high implantation doses at liquid nitrogen temperatures

Ion implantation is an enabling technology for creating selective area doping and forming high resistance regions in device structures. For the development of ion implantation doping for advanced GaN-based electronics, it is important to understand the dopant activation process, and implantation-induced damage generation and removal. Recent studies have shown that quite good activation efficiency can be obtained by annealing at 1100^0 C anneal, but implantation damage cannot be significantly removed at this temperature. Annealing at temperatures $>1300^0$ C are suggested to fully remove the damage and further optimize the transport properties of implanted regions in GaN. Since these temperatures are beyond the capability of most rapid thermal annealing systems, new annealing apparatus must be developed. Consequently, there is an urgent need to carry out detailed studies on the dopant activation, impurity redistribution, defect removal, and surface degradation at these elevated temperatures. Efficient surface protection must be developed to prevent material decomposition and N_2 loss from the GaN surfaces.

Ion implantation is also attractive for inter-device isolation and producing current guiding. Efficient compensation has been achieved in the GaN materials by using N or He implantation. However, the isolation is not stable at high temperatures, i.e. typical implant damage compensation. Implantation in In-containing III-V nitrides has shown that InGaN, as used in LED, laser cavity, or transistor channel, is difficult to be rendered highly resistive. The defect level is usually high in the energy gap, not near midgap, as is ideal for implant isolation. There is a strong need for an understanding of the implant isolation process and mechanism in III-V nitride materials because of the emerging applications for high temperature, high power electronics based on this material system. In particular, attempts need to be made to explore thermally stable implant isolation in GaN, and significant compensation must be achieved in the In-containing nitrides [22].

CHAPTER 2

Theory on GaN Material

2.1 Evolution of Gallium Nitride

Recently, Group III nitride-based semiconductors have emerged as the leading material for the production of blue LEDs, blue laser diodes, and high-power, high-temperature electronics. The achievement of high brightness blue InGaN LEDs has basically caused a revolution in LED technology and opened up enormous new, previously inaccessible markets. The use of InGaN/GaN double heterostructures in LEDs in 1994 by Nakamura and the achievement of p-doping in GaN by Akasaki are widely credited with re-igniting the III-V nitride system. The historical evolution of GaN materials and device technology in Japan in the early 1990s is regarded as one of the key developments in solid-state devices today [23]. These remarkable advancements in GaN-based LED materials have depended on several key breakthroughs in materials synthesis and fabrication. The lack of p-n junctions in Group III nitrides and their poor crystal quality slowed research for many decades. The recent realization of blue lasers has taken over 20 years from the time the first optical pumped stimulated emission was observed in GaN crystals and the first LEDs were fabricated. The purpose of this chapter is to review the status of GaN materials technology in Japan.

2.2 GaN Material Properties:

2.2.1 GaN Structure and Material parameters:

The band gap in the (Al,Ga,In) N-based materials system ranges from 1.9 eV (InN) to 3.39 eV (GaN) to 6.2 eV (AlN). The band structure is currently thought to be a direct band gap across the entire alloy range. Therefore, almost the entire visible range of wavelengths is spanned in the Group III nitride alloy system. This direct band gap is especially fortuitous as it allows for high quantum efficiency light emitters to be fabricated in this system [24, 25].

	Units	GaN
Symmetry	-	Wurtzite/ zinc blende
Density	g/cm	6.15
Static Dielectric Constant		8.9
High-Frequency Dielectric Constant		5.35
Energy Gap (Valley)	eV	3.39
Effective Mass (Valley)	m_e	0.20
Polar Optical Phonon Energy	meV	91.2
Lattice Constant, a (c)	Å	3.189 (5.185)
Electron mobility	cm^2/Vs	1000
Hole mobility	cm^2/Vs	30
Saturation velocity	cm/s	2.5×10^7
Peak velocity	cm/s	3.1×10^7
Peak velocity field	kV/cm	150
Breakdown field	V/cm	$>5 \times 10^6$
Light hole mass	m_e	0.259
Thermal Conductivity	W/cm-K	1.5
Melting Temperature	^oC	2530

Table 1: GaN Material Parameters, Electrical Parameters and Transport Properties

The Table 1 shows the material and electrical parameters and transport properties showing the potential application to high power RF amplifier.

2.2.2 Crystal Structure of GaN:

Gallium nitride is a III-V semiconductor and can adopt the zinc-blend or wurzite crystal structures. A schematic of the zinc-blend crystal structure is shown in Figure 1. This is essentially the compound equivalent of the diamond crystal structure.

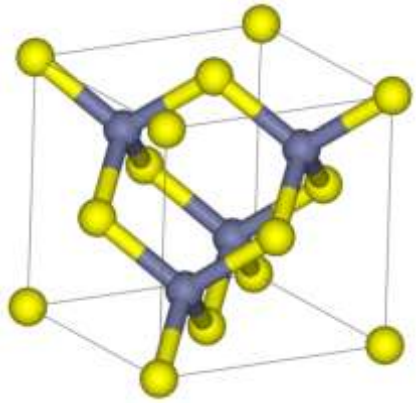

Figure 1 Three-Dimensional Structure of Gallium Nitride

2.2.3 GaN Physical Properties:

Group III nitrides possess several remarkable physical properties that make them particularly attractive for reliable solid state device applications. The wide band gap materials possess low dielectric constants with high thermal conductivity pathways. Group III nitrides exhibit fairly high bond strengths and very high melting temperatures. The large bond strengths could possibly inhibit dislocation motion and improve reliability in comparison to other II-VI and III-V materials. In addition, the nitrides are resistant to chemical etching and should allow GaN-based devices to be operated in harsh environments. These properties may lead to devices with superior reliability.

2.3 Nitride Materials Growth Issues:

2.3.1 MOCVD Growth:

MOCVD is a non-equilibrium growth technique that relies on vapor transport of the precursors and subsequent reactions of Group III alkyls and Group V hydrides in a heated zone. The MOCVD technique originated from the early research of Manasevit (1968) who demonstrated that triethylgallium (TEGa) and arsine deposited single crystal GaAs pyrolytically in an open tube, cold-wall reactor. The basic MOCVD reaction describing the GaN deposition process is:

$$Ga(CH_3)_{3(V)} + NH_{3(V)} \rightarrow GaN_{(S)} + 3CH_{4(V)}$$

However, the details of the reaction are not well known, and the intermediate reactions are thought to be complex. Further work is needed to understand the fundamentals of this crystal growth process.

Various researchers employ both atmospheric-pressure and low-pressure MOCVD reactors in the growth of GaN. The majority of research groups in Japan utilize atmospheric pressure reactors because of the high partial pressures of ammonia. Nakamura and his colleagues achieved the breakthrough in bright blue LEDs using a modified MOCVD system. Nichia Chemistries Inc. has employed a novel two-flow approach that yields excellent film quality.

MOCVD reactor designs for GaN growth must overcome problems presented by high growth temperatures, pre-reactions, and flow and film non-uniformity. Typically in GaN growth, very high temperatures are required because of the high bond-strength of the N-H bond in ammonia precursors. Compounding this fact is the thermodynamic tendency of ammonia to pre react with Group III metal organic compounds to form non-volatile adducts. These factors contribute to the difficulties currently facing researchers in the design and scale-up of III-V nitride deposition systems. Much research activity is needed in the scale-up and understanding of the mechanism of gallium nitride growth by MOCVD [26]. As shown in Figure 2, impurity sources are supplied in this DenBaars 19 reactor from a horizontal inlet and from a vertical sub-flow rather than driving the reactants to the growing film surface.

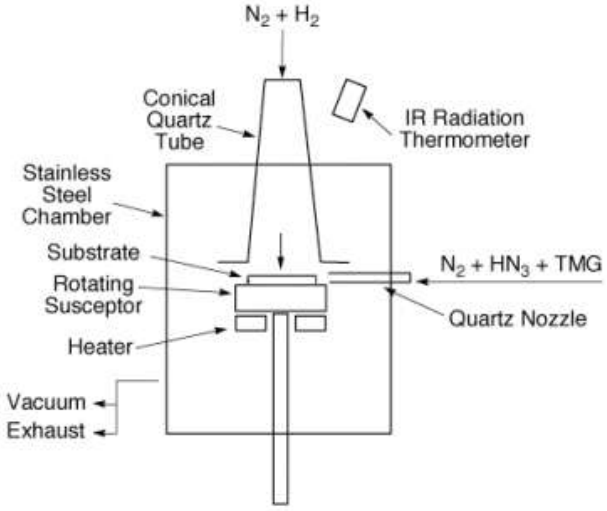

Figure 2 Two-Flow atmospheric pressure MOCVD approach at Nichia

2.3.2 Molecular Beam Epitaxy (MBE):

Several researchers in Japan have begun developing MBE for growth of III-V nitrides. Several approaches have been investigated for supplying an atomic source of nitrogen. RF plasma and electron cyclotron resonance (ECR) microwave plasma sources are the two most successful techniques discovered so far [27, 28]. In these RF plasma MBE systems, the plasma source is used to crack molecular nitrogen. These plasma sources use cylindrical cavity geometry to efficiently pump microwave energy into the nitrogen discharge area. The plasma stream is a complex mixture of atomic, molecular, and ionic N radicals. When using ECR sources, a tradeoff between growth rate and ion damage occurs [29]. Under normal ECR use, the flux of the low energy reactive N species is so low that only low growth rates of 500 Å/hr can be achieved. At higher microwave powers, higher growth rates can be achieved, but ion damage leading to deep levels and semi-insulating electrical properties occurs. A major advantage of MBE for nitride growth is the low growth temperature that can be achieved because of the atomic nitrogen source. This is in contrast to MOCVD, which must employ high growth temperatures (>1000°C) to crack the ammonia molecules.

The lower growth temperatures should result in lower thermal stress upon cooling, less diffusion, and reduced alloy segregation. This lower growth temperature is especially important in the AlGaN alloys that have a large mismatch in their thermal expansion coefficients [30].

2.3.3 GaN Bulk Crystal Growth:

In Poland, world-leading bulk GaN crystal growth is being achieved at Unipress Institute [27]. The Unipress Institute research group is located at the High Pressure Research Center (HPRC) in Warsaw, where they employ GaN bulk crystal growth from a melt. As shown in figure 3, pressure 10Kbar is required to growth GaN from a melt. One of the most impressive achievements the panel saw in Europe was the “defect free” bulk GaN wafers grown from melt under extremely high pressure. Dr. Isabel Gregory gave an overview of the high-pressure solution growth method used for depositing the bulk single crystals.

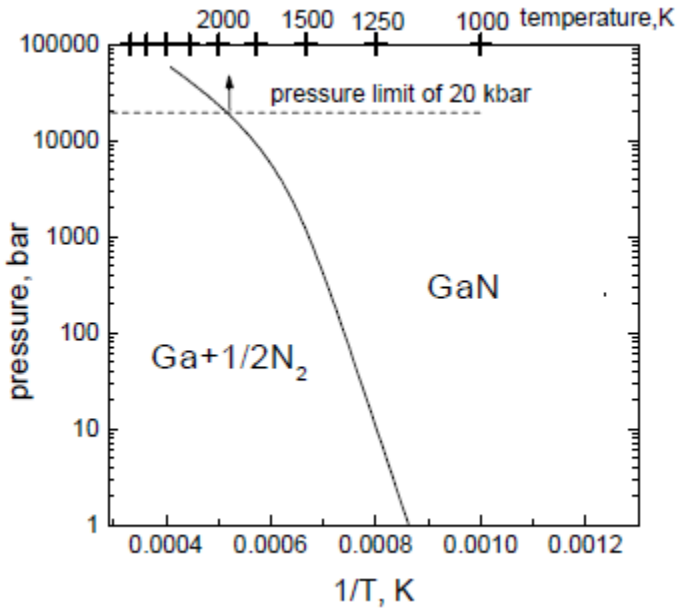

Figure 3 Nitrogen pressure vs. Growth temperature for bulk GaN substrate growth.

The size of the substrates has steadily increased up to 1cm in 1999 from 5mm in 1997. In comparison to GaN on sapphire technology which exhibits $1x10^{9}cm^{-2}$ defect densities, or ELO films which are in the $1x10^{6}cm^{-2}$ to $5x10^{5}cm^{-2}$ ranges the bulk GaN crystals possess 10 to 1 defect per square centimeter. These densities were estimated from etch pit counts and correlated to TEM measurements of higher defect densities found on standard GaN sapphire technology. The team was allowed to observe the bulk crystals under both optical microscopes and field emission SEM. Both n-type bulk crystals and semi-insulating bulk crystal have been grown. The semi-insulating substrates were highly resistive $1x10^{5}\Omega$-cm and could be used for thin film deposition of high power AlGaN/GaN microwave amplifiers. Very high quality homo-epitaxial growth of GaN by MOCVD was obtained on top of these substrates and the films exhibited narrow double-Crystal x-ray diffraction (DCXRD) line-widths as low as 21 arcsec. Figure 4 shows an image of a 1cm diameter crystal grown by the Unipress group [31-35].

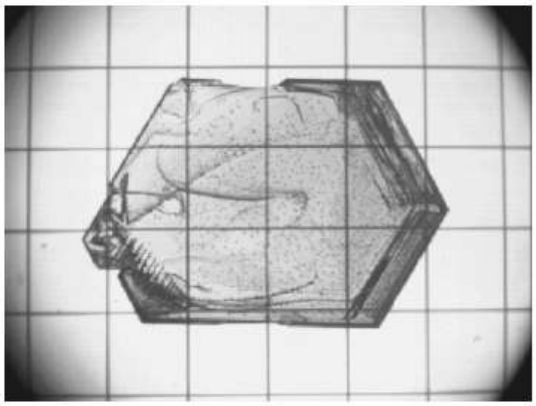

Figure 4 One-cm Diameter Bulk GaN Substrate

The group at University of Ulm in collaboration with Unipress has obtained thin films which exhibit the narrowest reported PL line widths at low temperature (0.1meV) which is indicative of the uniform high quality film [36]. MBE has also been performed on the bulk crystals. Both Ga-face and N-face polarity bulk substrates have been produced. The bulk crystals also display extremely smooth cleaved facets with RMS roughness of 5 angstroms which would make excellent laser facets.

2.3.4 Electronic Materials and Epitaxial Lateral Overgrowth:

Research on the electronic device applications of GaN is progressing more slowly in Japan than in the United States because there is less commercial need for such high power electronic devices. As of 1998, six groups in Japan were actively working on GaN electronic devices: Sony, NEC, Furukawa Electric, Meijo University, Electro technical Laboratories, and Kyoto University. However, many other groups the panel visited stated unofficially that they would begin efforts in the near future as soon as the materials properties improved. At most, group mobility's for bulk GaN have exceeded 600 cm^2/V-sec, and AlGaN/GaN 2-dimensional gas mobilities exceeding 900cm^2/V-sec have been obtained at the Sony Research Center. Sony, NEC, Furukawa, and Meijo University all demonstrated working high electron mobility transistors (HEMTs). At the time of the panel's visit, no RF power results had been reported in Japan. The strength that the panel saw was the dedication of several groups to basic materials research. Of particular note was the epitaxial lateral overall (ELO) growth method being developed at both Nichia and NEC for defect reduction in GaN on sapphire substrates? Lateral epitaxial

overgrowth (LEO) is an attractive method for producing GaN films with a low density of extended defects, which is beneficial both to studies of the fundamental properties of the GaInAlN materials system and to GaN-based device technology.

The basic concept is to reduce defect propagation in masked regions of the substrate where the laterally overgrowing GaN is defect free. This is illustrated in the transmission electron micrograph in Figure 5. Recent studies in Japan and in the United States have confirmed that the density of threading dislocations (TDs) is reduced by 3-4 orders of magnitude in LEO material grown on 6H-SiC substrates and Al_2O_3. The mechanisms of threading dislocations evolution during LEO have also been investigated. Studies of the optical properties of LEO GaN and InGaN quantum wells have revealed that TDs act as non-radioactive recombination centers [37].

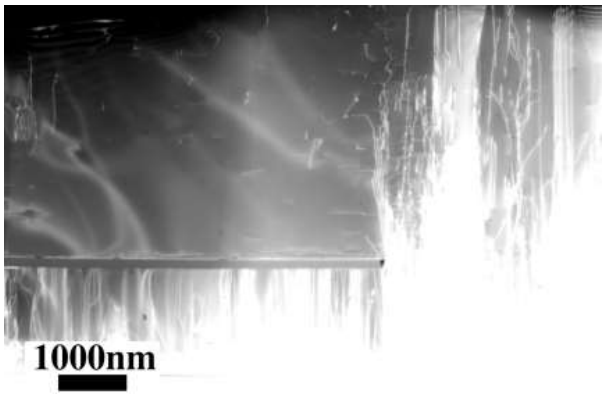

Figure 5 Cross-sectional GaN displaying large reduction of threading dislocation in lateral overgrown GaN region

However, the minority carrier diffusion length (<200 nm) is smaller than the average distance between TDs so that the emission mechanisms of the carriers that do recombine radioactively appear to be unaffected by moderate TD densities (~106-109 cm^{-2}).

On the other hand, reducing the TD density has been shown to reduce the reverse leakage current by ~3 orders of magnitude in GaN p-n junctions, in InGaN single and multiple quantum well light emitting diodes, and in GaN/AlGaN heterojunction field-effect transistors fabricated on LEO GaN. More recently, ultraviolet p-i-n photo detectors

fabricated on LEO AlGaN have exhibited a similar reduction of the reverse leakage current by up to 6 orders of magnitude. The use of LEO GaN has also resulted in marked improvements in the lifetime of InGaN/GaN laser diodes. At Nichia, a key development in obtaining reliable CW laser performance was defect reduction by using an epitaxial lateral overgrowth GaN (ELOG) substrate. In this technique, a silicon dioxide mask is used to block dislocation propagation, and a "defect free" film is achieved in the laterally overgrown region.

After hundred microns of growth, a fully coalesced GaN thin film are achieved, and a proprietary process removes the sapphire substrate. The ELO process is shown schematically in Figure 5. Laser diodes with InGaN/GaN multiple quantum well (MQW) active regions are then grown on top of this virtual bulk GaN substrate. The active regions are then defect free and can survive under high current operation ($3kA/cm^2$). At NEC, Dr. Usui has achieved remarkable success in pioneering defect reduction in GaN with the lateral epitaxial overgrowth (LEO) method. Dr. Usui calls this NEC process "facet initiated epitaxial lateral overgrowth" (FIELO) [38].

In this technique, defects are reduced by having the growing facet steer the edge defect parallel to the surface so that they cannot propagate on the surface. The defect density is reduced from $1x10^9/cm^2$ to less than $1x10^7/cm^2$. Dr. Usui has even made "bulk-like" GaN substrates by lifting thick GaN epitaxial films from the sapphire substrate using a proprietary technique. These bulk-like GaN films are 100 to 200 microns thick and 1 cm by 1 cm wide. These low defect films can be used to make conventional type edge-emitting lasers. Dr. Usui has developed a hydride vapor phase epitaxy (HVPE) method for depositing the thick LEO films on sapphire substrates. The films are grown at 1000ºC and are 100 to 200 microns thick after a few hours. The best X-ray line width is 150arcseconds, and mobilities of $863cm^{2/}$V-sec and 2780 cm^2/V-sec have been obtained at 300K and 77K, respectively [39-42].

The transport properties of GaN have been studied using analytical calculations and Monte Carlo simulations. These properties depend on materials quality, and the values given in Table 1 represent typical or theoretically predicted values.

CHAPTER 3

Physics of GaN- MESFET

3.1.1 Physical structure:

The schematic cross-section of GaN MESFET is shown in Figure 6. The light radiations having photon energy greater than or equal to bandgap energy are allowed to fall vertically on the semi-transparent gate metal.[43]

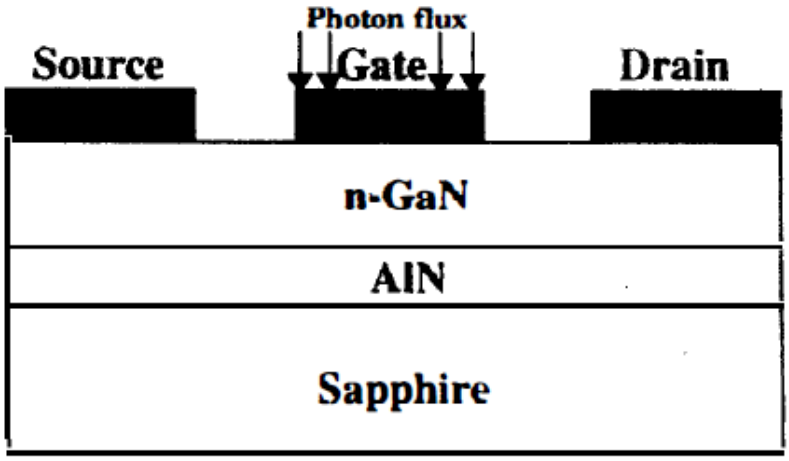

Figure 6 Schematic cross-section of GaN MESFET with optical illumination

A thin layer of n-type GaN is deposited on top of a semi-insulating Si substrate. The back face of the substrate is covered with a metal Au/Ge alloy, which is usually connected to the source terminal during measurements. Both drain and source are connected to the n-type layer through n+ ohmic contacts. The metal of the source and drain electrodes can be made of Au/Ge alloy, which is coated with Ti, Pt, and Au layers, respectively. The gate is a thin layer of metal, usually aluminum coated with Au, deposited on top of the n-type layer between drain and source. The metal semiconductor junction of the gate represents a Schottky barrier junction. This junction is used to control the height of the active channel layer beneath the gate by applying a bias voltage to the gate [44-47]. The area just beneath the gate is charge depleted as per the applied bias.

The most important dimensions of a MESFET device are the gate length (L), width (W) and active channel depth. Those dimensions usually characterize the device. For example, a device can be referred as 0.3x300 μm^2 when the gate length is equal to 0.3 μm and the gate width is equal to 300 μm. The gate length determines the maximum

frequency of operation [48]. As the gate length decreases, the maximum frequency increases. On the other hand, the gate width determines the performance of the device such as the maximum current capability [49-51]. The active channel translates the pinch-off voltage of MESFET device.

3.1.2 Principles of the GaN MESFET Operation:

A MESFET device is biased by applying two voltages: V_{GS} between gate and source and V_{DS} between drain and source. These voltages control the channel current between the drain and source by varying the depth of the gate-depletion region and the longitudinal electric field [52]. The operation can be explained qualitatively without going into deep physical analysis. Three cases can be recognized for the I_{DS}-V_{DS} characteristic curve of the MESFET, if V_{GS} is larger than the pinch-off voltageV_p,: low V_{DS} voltage where I_{DS} is linearly proportional to V_{DS}, high V_{DS} where the current is almost constant, and moderate V_{DS} where I_{ds} has nonlinear relationship of V_{DS}.

3.1.3 I-V Characteristics of Ga-N MESFET

The drain-source current against drain-source voltage (I_{DS} -V_{DS}) characteristic of the GaN MESFET on Si is shown in Figure 7

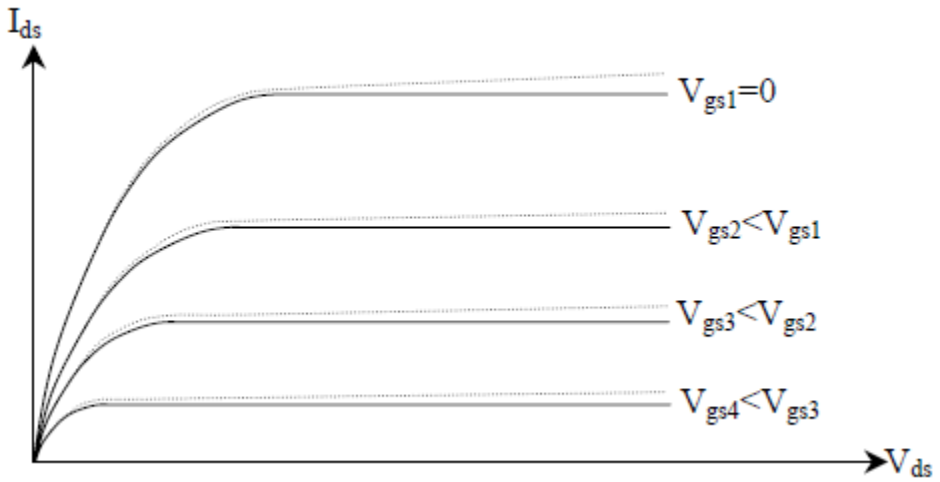

Figure 7 I_{dS} versus V_{dS} characteristic at different V_{GS} for GaN MESFET

I-V characteristic curves of a MESFET device are shown in Figure 7 for an ideal and actual MESFET. The curves are plotted for different values of V_{GS}. It is obvious that the actual I-V curve exhibits finite positive slope in the saturation region. Many reasons may

be responsible for this phenomenon. One of the most dominant reasons in a short gate device is the carrier injection into the semi-insulating substrate. This finite slope is the source of the finite output conductance in a MESFET model. Ideal current is drawn in solid curve while dashed curve indicates the actual current.

Imagine first that V_{GS}=0 and V_{DS} is raised from zero to some low value as shown in Figure 8(a). When V_{GS}=0, the depletion region under the Schottky-barrier gate is relatively narrow, and as V_{ds} is raised, a longitudinal electric field and current are established in the channel. Because of V_{DS}, the voltage across the depletion region is greater at the drain end than at the source end, so the depletion region becomes wider at the drain end [53].

The narrowing of the channel and the increased V_{DS} increase the electric field near the drain, causing the electrons to move faster. Although the channel depth, and in turn channel's conductive cross section, is reduced, the net effect is increased current. When V_{DS} is low, the current is approximately proportional to V_{DS}. However, if the gate reverse bias is increased while the drain bias is held constant, the depletion region widens and the conductive channel becomes narrower, reducing the current. When V_{GS}=V_p, the pinch-off voltage, the channel is fully depleted and the drain current is zero, regardless of the value of V_{DS} [54-58]. The active channel depth determines the pinch-off voltage, therefore the active channel depth is to be fixed during the fabrication process it is set to pinch-off voltage and breakdown voltage.

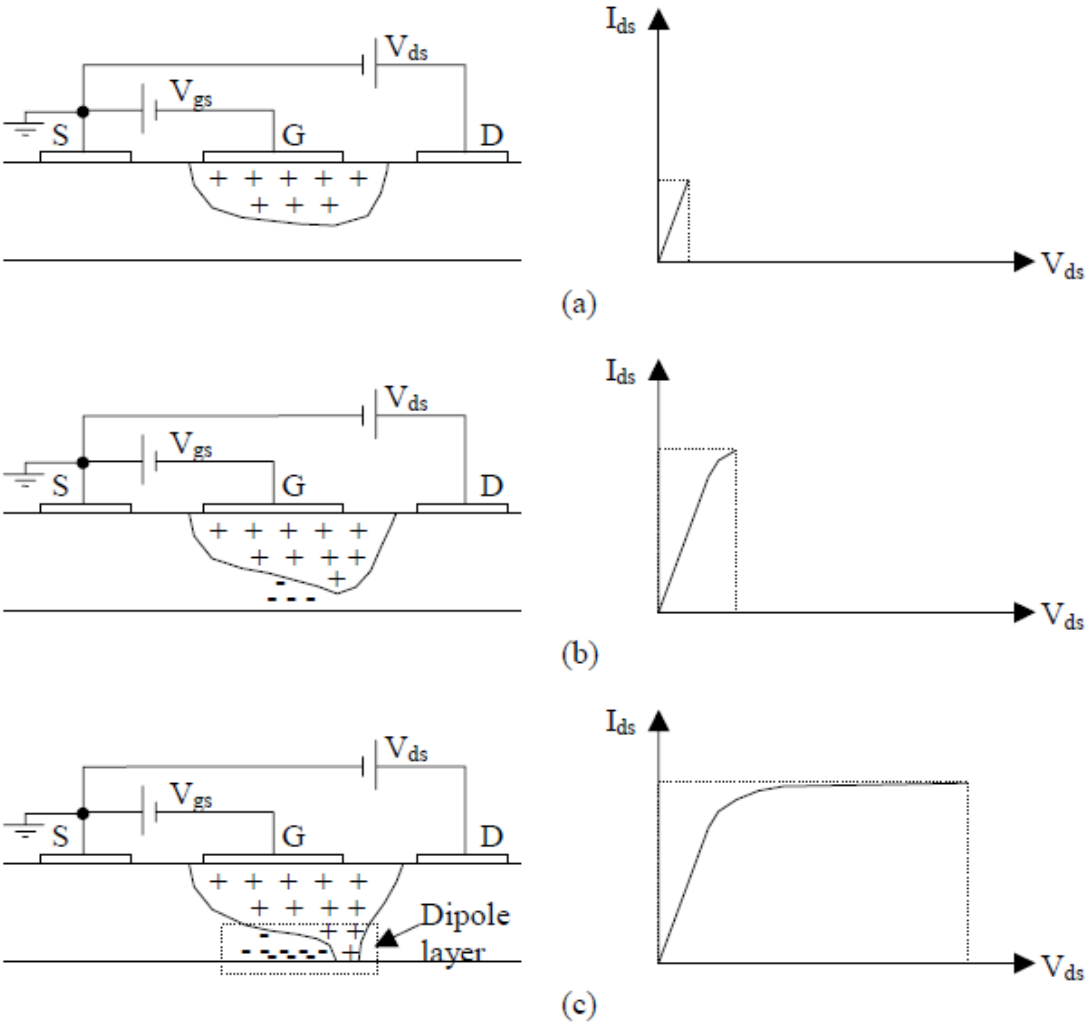

Figure 8 GaN MESFET operation under different V_{ds} biasing with $V_{gs} = 0$: (a) Linear region (V_{ds} is very low), (b) V_{ds} at the onset of saturation, (c) V_{ds} big.

If voltage from drain-to source (V_{ds}) is raised further, as shown in Figure 8(b), while Voltage from gate-to source (V_{gs}) is larger than the pinch-off voltage, the channel current increases, the depletion region becomes deeper at the drain end, and the conductive channel becomes narrower. The current clearly must be constant throughout the channel. As a result, and as long as the conductive channel near the drain becomes narrower, the electrons must move faster [59-62].

If V_{ds} is increased beyond the value that causes velocity saturation (usually only a few tenths of a volt), the electron concentration rather than velocity must increase in order to maintain current continuity. Accordingly, a region of electron accumulation

forms near the end of the gate. Conversely, after the electrons transit the channel and move at saturated velocity into the wide area between the gate and drain, an electron depletion region is formed. The depletion region is positively charged because of the positive donor ions remaining in the crystal [63-67]. As V_{ds} is increased further, as shown in Figure 8(c), progressively more of the voltage increase is dropped across this region to enforce the electrons to cross it and less is dropped across the unsaturated part of the channel. This region is called a dipole layer or charge domain. Eventually, a point is reached where further increase in V_{ds} is dropped entirely across the charge domain and does not substantially increase the drain current. At this point, the electrons move at saturated drift velocity over a large part of the channel length. When the MESFET is operated in this manner, which is the normal mode of operation for small-signal devices, it is said to be in its saturated region. Accurate models may include the effect of the charge domain in some way. Therefore, some models include a capacitor between the drain and the gate-source equivalent circuit to account for the charge domain

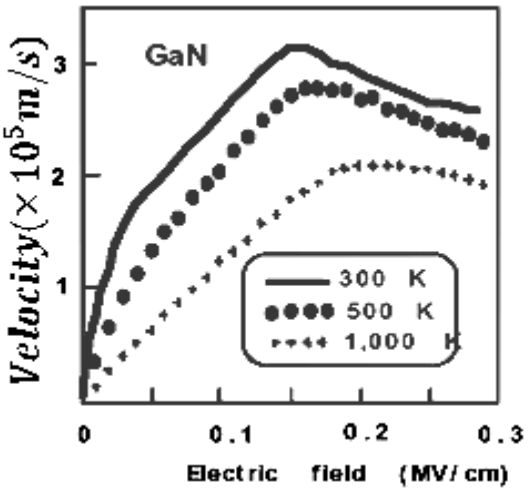

Figure 9 Drift Velocity versus Electric field

Figure 9 shows the Drift velocity versus electric field for different temperature. As temperature increases the drift velocity decreases and approaches saturation. However, the electron velocity cannot increase indefinitely; the average velocity of the electrons in GaN cannot exceed a velocity called the saturated drift velocity, approximately 1.3×10^7 cm/s.

3.1.4 Carrier Mobility in Gallium Nitride (GaN)

Carrier mobility is a function of temperature, electric field, doping concentration, and material quality of a semiconductor. Among them the latter depends on the substrate. Due to a large difference in lattice constant, nitride crystals grown on sapphire produce sometime cracks during cool down, and the Hall mobility is about 10-30 cm^2/Vs. The carrier mobility of the GaN film was consequently improved. As recorded by the Hall measurement, the improvement was about ten times to a value of 350-400 cm2Ns at room temperature [68-72].

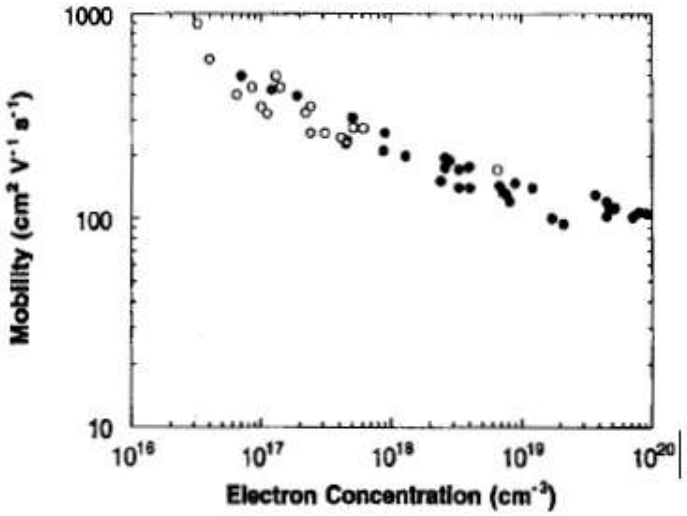

Figure 10 Mobility versus Electron concentration for GaN

the statistical average of data presented in Figure 10 suggest that electron mobility decreases in general with increase in the electronic concentration, no matter how thick the buffer layers are, and what substrate was used for the growth The very regular trend of this decrease indicates that it is rather exponential and not linear in nature. The small spread in values from various sources is probably due to insufficient growth optimization, differences in Hall measurement techniques, variations in the substrates and buffer layers used, and the differences in the growth temperature [73].

3.1.5 MESFET Models:

The large-signal model can be proposed based on the physical structure of the MESFET device. Most of the suggested models are based on the model shown

in Figure 11. Both large and small-signal models are shown in the same figure. The small- signal model can be derived directly from the large-signal model. The relationship between the physical structure and model elements are also indicated. This model is a lumped-element model which is valid over a frequency range of several tens of GHz.

The physical meaning of each element is clearly interpreted. R_g is the ohmic resistance of the gate while R_S and R_d are the source and drain ohmic resistances, respectively. L_g is the inductance of the gate while L_S and L_d are the inductances of the source and the drain metallization, respectively. R_i is the resistance of the semiconductor region under the gate, between the source and the channel.

C_{ds} the drain-source capacitance, which is dominated by geometric capacitance and is often, treated as a constant. C_{gs} and C_{gd} are the channel capacitances which in general are nonlinear [74].

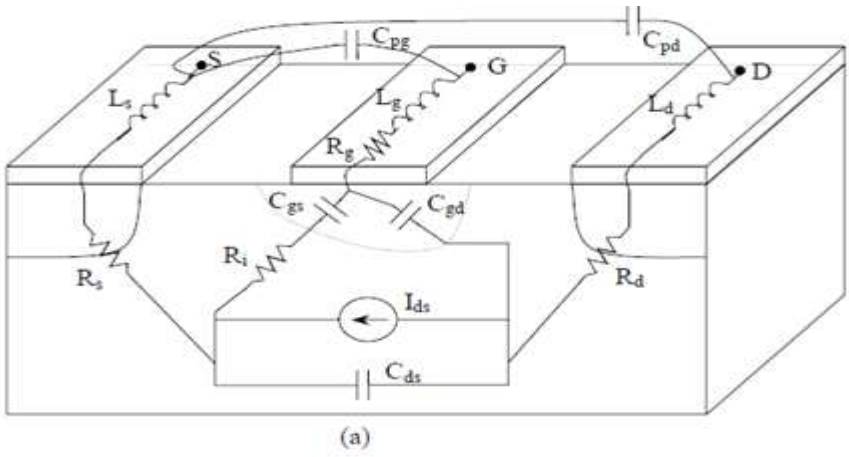

Figure 11 MESFET models showing physical origin of elements: (a) physical origin of each element.

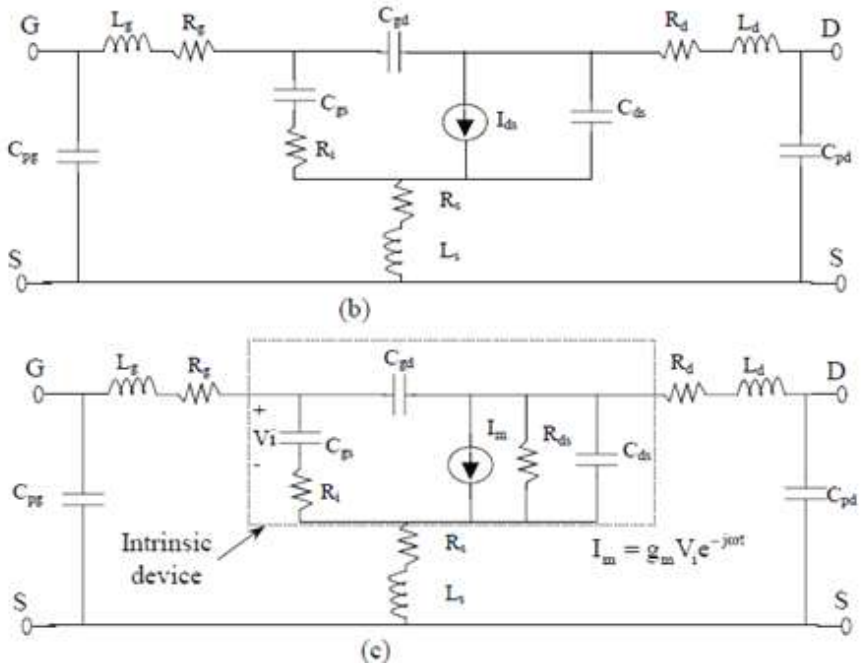

Figure 11 MESFET models showing physical origin of elements: (b) large signal model, (c) small signal model.

I_{ds} is the controlled drain-source current from which the transconductance g_m, transit time delay τ, and output resistance R_{ds} can be calculated. C_{pg} and C_{pd} are the pad capacitances of both gate and drain, respectively, on one side with respect to the source on the other side.

If voltages are expected to be great enough to forward–bias or reverse avalanche-breakdown the gate junction, one can include diodes in parallel with C_{gs} and C_{gd}. Such diodes are of limited practical value, however, because operation with gate-channel avalanche breakdown or high values of rectified gate current usually destroys the device. Some of the model elements are nonlinearly dependent on the internal voltages V_{gs} and V_{ds}. Others are linear, or can be approximated as linear elements. I_{ds}, C_{gs}, and C_{gd} are usually nonlinear elements for their strong dependence on V_{gs} and V_{ds} [75].

On the other hand, the circuit model can be divided into two parts: the extrinsic

parameters and the intrinsic parameters. The intrinsic parameters characterize the active region under the gate and are functions of biasing conditions, whereas the extrinsic parameters depend, at least to a first approximation, only on the technological parameters. The intrinsic parameters include C_{gs}, R_i, C_{gd}, g_m, R_{ds}, and C_{ds} whereas the extrinsic parameters include all other elements in the model C_{pg}, C_{pd}, R_g, R_d, R_S, L_g, L_d, and L_S. Some of the intrinsic elements can be assumed linear for their weak dependence on the internal voltages, those elements are R_i, , and C_{ds}. In contrast, some of the extrinsic elements may be nonlinear if their dependence on the internal voltages is significant.

3.2.1 Parasitic Inductances:

The parasitic inductances are the inductances of the extrinsic part of circuit model which include L_g, L_d, and L_S. Those inductances arise primarily from metal contact pads deposited on the device surface. For short gate length devices, the gate inductance is usually the largest of the three, although this is a function of the particular layout employed. Typically, L_g and L_d are on the order of 5 to 10 pH. The source inductance is often small, about 1 pH. Note that these inductances exist for the bare die device, so, any other inductances such as parasitic bond wire inductances or parasitic package inductances must also be accounted for in the complete circuit model of the packaged device. In many cases, bonding inductances are on the order of 0.1 to 0.3 nH and dominate the device parasitics.

3.2.2 Parasitic Resistances:

The parasitic resistances R_g, R_d, and R_S are also included in the extrinsic part of the circuit model. The resistances R_S and R_d are included to account for the contact resistance of the ohmic contacts between the metal electrodes and the n+-GaAs as well as any bulk resistance leading up to the active channel. The gate resistance R_g results from the metalization resistance of the gate Schottky contact. All three resistances are on the order of a few ohms. Although measurements of R_S and R_d indicate a slight bias dependence in these values, they are held constant in the large-signal models commonly available in the commercial simulators nowadays. However, accurate models should take

into consideration their bias dependence, especially if their values are significantly depends on the bias voltages. All parasitic resistance values can be estimated either from forward DC conduction measurements or directly from S-parameters using an optimization technique. However, the latter technique is preferable for more accurate results because it calculates the resistance values from typical high frequency data at the bias point of concern [76].

3.2.3 Pad Capacitances:

These capacitances are also included in the extrinsic part of the circuit model. The pad capacitances come from the stray capacitance between the metal pads. The pad capacitance consists of crossover capacitance of the metal lines and the capacitance between the pad and the back face of the semi-insulating substrate, which is usually connected to the source terminal. However, the crossover capacitance is usually much smaller than the substrate capacitance [77]. Two pad capacitances are often included in the circuit model: C_{pg} gate pad capacitance and C_{pd} drain pad capacitance. C_{pg} is the capacitance between gate and source pads whereas $C_{pd\ is}$ the capacitance between the drain and source pads. Although the pad capacitance between gate and drain pads can be included in the circuit model, it is usually neglected for its small value compared to other capacitance values in the model.

C_{pg} and C_{pd} are typically on the order of a few tens of fF. Nevertheless, they may be omitted from many models in the literature if their values are insignificant or if their effect can be accounted for throughout other capacitive elements in the circuit. On the other side, pad capacitances may be placed in two different positions in the model either on the most outer terminals of the model as seen in figure 11(a) or between the corresponding parasitic inductances and resistances. Pad capacitance values depend on the utilized layout. Pad capacitances can be estimated either from special structures without the active device or directly from S-parameter measurements using an optimization technique.

3.2.4 Intrinsic Capacitance:

Intrinsic capacitances are indicated in the model by C_{gs}, C_{gd}, and C_{ds}. C_{gs} and C_{gd} model the change in the depletion charge with respect to the gate-source and gate-drain voltages, respectively. Figure 12(a) and 12(b) shows the depletion region beneath the gate for a symmetric structure where the gate is located directly in the middle of the gap between the source and the drain terminals. Figure 12(a) represents the symmetric bias case in which $V_{gs}=V_{gd}$. Figure 12(b) represents the case in which the gate-drain reverse bias is greater than the gate-source reverse bias. This case represents the normal MESFET bias conditions in most applications. Figure 14 is only used to clarify the physics of both C_{gs} and C_{gd}. However, the discussion is also valid for any geometrical structure and bias conditions [78].

The distribution of the depletion charge is symmetric with respect to the drain and source in Figure 12(a). On the other hand, the depletion charge extends deeper at the drain end of the gate than at the source end of the gate, and it also extends closer to the drain than to the source. This charge redistribution in the depletion region with the bias voltage variation identifies the two depletion capacitances C_{gs} and C_{gd}. The charge of the depletion region is shared between C_{gs} and C_{gd}. Thus, they should be defined carefully as:

$$C_{gs} = \frac{dQ_q}{dV_{gs}}\Big| \longrightarrow V_{gd} = \text{constant} \quad (1a)$$

$$C_{gd} = \frac{dQ_q}{dV_{gd}}\Big| \longrightarrow V_{gs} = \text{constant} \quad (1b)$$

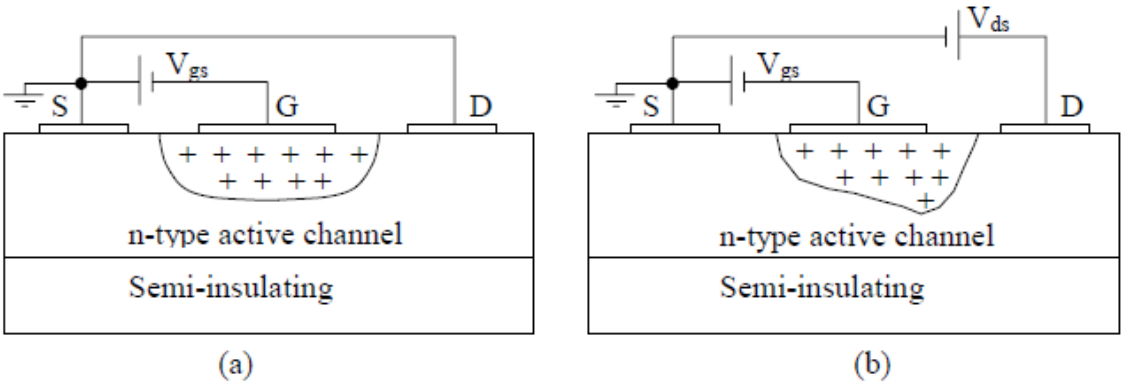

Figure 12 Depletion region shapes for different applied bias voltages: (a) gate-source voltage is equal to gate-drain voltage; (b) gate-drain reverse bias is greater than gate- source reverse bias.

Under normal operation conditions, V_{gs} and V_{ds} are the DC controlling bias voltages. For this reason, the gate to source capacitance is often defined as:

$$C_{gs} = \frac{dQ_q}{dV_{gs}}\Big| \longrightarrow V_{ds} = \text{constant} \qquad (1c)$$

Equations (1a) and (1b) are not equivalent, but slightly different quantities. The distinction is usually minor, but can be significant if calculations are based on a physically based model in which the depletion charge is defined by a mathematical expression. When capacitance is determined by measurements or derived from empirical models, the capacitance definition given by equations (1a) and (1b) are not applied. Instead, the capacitance values are defined in terms of an equivalent circuit, and so, the values are determined to accurately predict the device behavior [79].

Thus, it does not matter in our thesis which definition of C_{gs} should be taken because C_{gs} is calculated from S- parameter measurements. One might also have noticed that the voltages indicated in the capacitance definitions are the internal voltages, and not the external terminal voltages.

Under typical MESFET bias conditions, C_{gs} is larger than C_{gd} because it models the change in depletion charge resulting from fluctuations in the gate-source

voltage while the gate-source reverse bias voltage is less than the gate-drain reverse bias voltage. It is well known from depletion capacitance analysis that the depletion capacitance decreases as the reverse junction voltage increases. For this reason and under normal bias conditions, the gate-drain capacitance C_{gd} is considerably smaller in magnitude than C_{gs}; nevertheless, C_{gd} is critical to obtaining accurate S-parameter predictions [80].

The drain-source Capacitance C_{ds} is included in the equivalent circuit to account for geometric capacitance effects between the sources and drain electrodes. It is usually not considered to be bias dependent for the purposes of device modeling. Values for C_{gs} are typically on the order of 1 pF/mm gate width under normal MESFET bias conditions. The values of C_{gd} and C_{ds} are about one tenth of the value of C_{gs}. Moreover, because of symmetry, C_{gs} and C_{gd} are approximately equal for V_{ds}=0.

3.2.5 Charging Resistance R_i:

Although the charging resistance R_i represents the intrinsic resistance under the gate between the source and the channel, it is included primarily to improve the match to S_{11}. For many devices, however, the presence of R_g is sufficient to match the real part of S_{11}. So, R_i is difficult to extract and is of questionable physical significance.

3.2.6 Transconductance g_m:

The intrinsic gain mechanism of the MESFET is provided by the transconductance. The transconductance g_m is a measure of the incremental change in the output current I_{ds} for a given change in the internal input voltage V_{gs}. The internal input voltage is the voltage across the gate source junction. In other words, the device transconductance is defined as the slope of the I_{ds}-V_{gs} characteristics with the drain-source voltage held constant. The mathematical statement of this definition can be expressed as:

$$g_m = \frac{6I_{ds}}{6V_{gs}}\Big| \longrightarrow V_{ds} = \text{constant} \qquad (1d)$$

The transconductance of the device is one of the most important indicators of the device quality for microwave and millimeter wave applications. When all other characteristics are equal, a device with high transconductance will provide greater gains and superior high frequency performance [81-82]. The transconductance suffers from what is called low frequency dispersion. The low frequency dispersion is the phenomenon of a parameter variation at low frequencies. The low frequency dispersion takes place as a result of the deep levels in the device structure. So, it significantly depends on the semiconductor material quality and fabrication processes.

Therefore, the transconductance varies with frequency below a frequency of about 1 MHz. RF values of transconductance are typically 5 to 25% lower than DC values for a GaN MESFET. Transconductance values vary directly with gate width and inversely with gate length.

3.2.7 Transit Time τ.:

The time takes by electron to move from source to drain is called transit time. The transconductance cannot respond instantaneously to changes in the gate-source voltage. The delay inherent to this process is described by the transit time (transconductance delay) τ. physically, the transconductance delay represents the time it takes for the charge to redistribute itself after a fluctuation of the gate voltage. Typical values of τ are on the order of 1psec. From physical considerations, transit time is expected to decrease with decreasing gate length.

3.2.8 Output Resistance R_{ds}:

The output resistance R_{ds} is the incremental resistance between drain and source, and it is more convenient to be explained in terms of its reciprocal, the output conductance g_{ds}. The output conductance is a measure of the incremental change in output current I_{ds} with the output voltage V_{ds}. So, it can be defined as the slope of the I_{ds}-V_{ds} characteristics with the gate-source voltage held constant. Mathematically, the output conductance and resistance can be defined by:

$$g_{ds} = \frac{1}{\mathrm{Rds}} = \frac{6I_{ds}}{6V_{ds}}\Big| V_{gs}\text{=constant} \quad (1e)$$

The output conductance of the device is an important characteristic in analog applications. It plays a significant role in determining the maximum voltage gain attainable from a device and is extremely important for determining optimum output matching properties. In general, it is desirable to have a device with extremely high output resistance, or equivalently, low output conductance. Values of g_{ds} are on the order of 1 mS/mm gate width at typical MESFET amplifier biases [83]. Also, as gate length is reduced, output conductance tends to increase. The low frequency dispersion is more significant in output conductance than in the transconductance. The RF output conductance can be more than 100% higher than the DC output conductance [84].

CHAPTER FOUR

Numerical calculations:

4.1 Theory on the Model:

A schematic structure of OPFET device is shown in Figure 14. The transparent gate is made of indium tin oxide (ITO) material to form a Schottky rectifying contact with proper antireflection coating and all optical and electrical parameters of this model are assumed to be the ideal case [85]. Under optically illuminated condition a one-dimensional Poisson's equation can be expressed in the following form

$$\frac{d^2\varphi(y)}{dy^2} = \frac{q}{\epsilon}[N(y,t) - G\tau n] \qquad (4.1)$$

The photogenerated carrier at the steady state derived by the following equation

$$G\tau_n = \alpha\emptyset\tau_n e^{(-\alpha y)} \qquad (4.2)$$

Where ,

G= Optical carrier rate

τ_n= Lifetime of electrons

α = Optical absorption coefficient

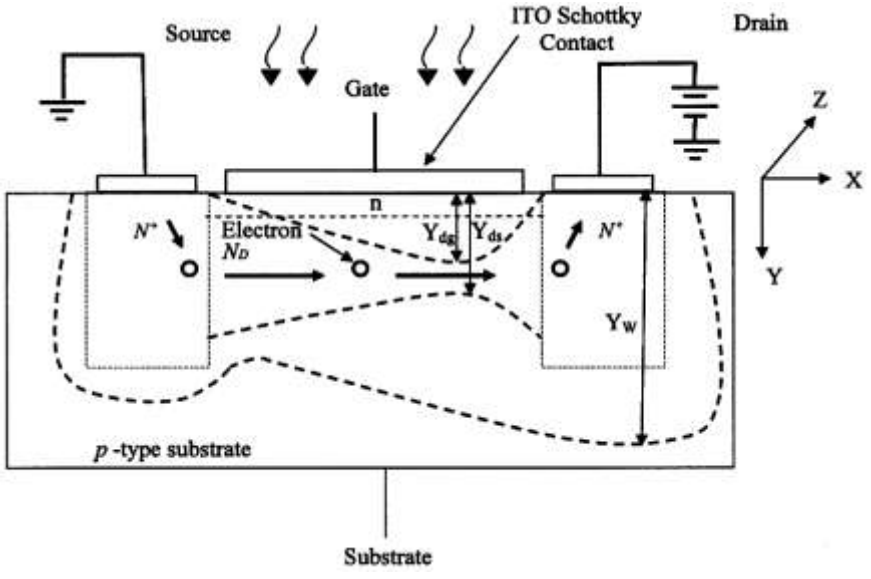

Figure 13 Cross-section of simulated GaN OPFET

The equivalent circuit parameters such as transconductance (g_m), output conductance (g_d) are taken as bias dependent whereas gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) are taken as both bias and frequency dependent. The frequency dependence of parasitic capacitances has been obtained by fitting the results obtained by simulations with second order polynomial.

In order to fabricate GaN MESFET, the ion implantation process is preferred due to higher temperature annealing causing impurity diffusion which will assist to activate the dopant. Therefore, the ion implantation is preferred over the diffusion process, where low diffusion coefficient is not able to activate the dopant impurities.

$$D=D_0 \times e^{(-EA/k\ Ta)} \quad (4.3)$$

Where,

K= Boltzmans constant = 1.38065 X $10^{-23} m^2 kg/s^2$

Annealing temperature Ta= 1473 K

Activation energy E_A=0.89 eV

Diffusion coefficient D_0=6.5x10^{-11}

Dopant	R_p Implant range parameter (cm).	σ Straggle parameter (cm).	D Diffusion coefficient (cm^2/s).	t Diffusion/annealing time (sec).	Q implant ion dose (cm^{-2}).
GaN	40×10^{-7}	20×10^{-7}	2.3×10^{-21}	45×60=2700	1×10^{13}

Table 2 Range Parameter and the corresponding straggle parameter

.

The information of the range parameter and the corresponding straggle parameter presented in the above Table 2 had been calculated using SRIM software and this model was incorporated an annealing time of 45 minutes. The diffusion constant and activation energy has been obtained from the journal study [84].

The derived equation for calculating gate-source capacitance (C_{GS}) is expressed below,

$$C_{GS} = \frac{qQionZL}{2}[M/(2\sqrt{(MR + A1)}) + \frac{\sqrt{N}}{2(\sqrt{N}-\sqrt{R})^2}(\frac{\sqrt{MN+A1}}{\sqrt{R}} - \frac{M(\sqrt{N}-\sqrt{R})}{\sqrt{MR+A1}} - \frac{\sqrt{MR+A1}}{\sqrt{R}} - \frac{qZL\tau n\phi S}{2\epsilon}(\frac{2(\sqrt{N}-\sqrt{R})}{\sqrt{R}} + \frac{Vds}{\sqrt{RN}}))] + \frac{\pi\varepsilon Z}{2} \quad (4.4)$$

Where,

N = phib-Vgs-delta-Vop 4.4(a)

R = phib-Vds-Vgs-delta-Vop 4.4(b)

$$M = \frac{4\alpha\varepsilon}{qQRp'} \quad 4.4(c)$$

$$A1 = \alpha^2 + A3 \quad 4.4(d)$$

$$\alpha = \frac{Rp'}{2\sqrt{\sigma^2+2Dt}}(\sqrt{\frac{\pi}{2}}) \quad 4.4(e)$$

$$A2 = erf(\frac{Rp'}{2\sqrt{\sigma^2+2Dt}}) - \alpha \quad 4.4(f)$$

$$A3 = 1 - exp(-(\frac{Rp'}{2\sqrt{\sigma^2+2Dt}})^2) - 2\alpha\, erf(\frac{Rp'}{2\sqrt{\sigma^2+2Dt}}) \quad 4.4(g)$$

Where,

C_{GS}= Capacitance from Gate to-Source.

q = Electronic charge.

Q_{ion} = Implant dose.

Z = Device width.

L= Channel length.

R_p= Implant range parameter.

phib =.Barrier height.

Vgs = Gate to-source.

σ = Straggle parameter.

Vop = Photo induced voltage.

Φ = Photon flux density.

ϵ = Permittivity of semiconductor.

Vds = Drain to-source.

Delta= Depth of Fermi level below the Conduction band.

Similarly, we can also derive the gate-drain capacitance for Gallium Nitride ion-implanted MESFET.

$$C_{GD} = \frac{qZQionL}{2}[M/(2\sqrt{(MN + A1)}) + \frac{\sqrt{R}}{2(\sqrt{N}-\sqrt{R})^2}(\frac{\sqrt{MR+A1}}{\sqrt{N}} - \frac{M(\sqrt{N}-\sqrt{R})}{\sqrt{MN+A1}} - \frac{\sqrt{MR+A1}}{\sqrt{N}} - \frac{qZL\tau n\phi S}{2\epsilon}(\frac{2(\sqrt{N}-\sqrt{R})}{\sqrt{R}} - \frac{Vds}{\sqrt{RN}}))] + \frac{\pi\varepsilon Z}{2} \quad (4.5)$$

Where,

C_{GD}= Capacitance from Gate to-Source.

4.2 Switching Characteristics

The switching time of an OPFET depends on the active layer thickness and active channel length of the ion implantation process. Switching time τ is computed for different active layer thickness and active channel length expressed by following equations (4.6) and 4.6(a) [85-86].

$$\tau = \frac{L\sqrt{\frac{2\epsilon(0.7 - Vop - Vg)}{qNdavg}}}{VsA - \sqrt{\frac{2\epsilon(0.7 - Vop - Vg)}{qNdavg}}} \quad (4.6)$$

Ndavg is calculated from the following equation

$$Ndavg = \frac{\emptyset}{\sqrt{2\pi(\sigma^2 + 2Dt)}} \exp\left[\frac{-Rp^2}{2(\sigma^2 + 2Dt)}\right] \quad 4.6(a)$$

Where,

τ = Switching time.

Vg = Gate voltage

L= Active Channel length

Vop= Photon induced voltage

Ndavg = Average channel doping concentration.

D= Diffusion constant

t = Annealing time

R_p = Range parameter.

σ = Straggle parameter.

Φ = Photon flux density.

Vs= Saturation velocity.

CHAPTER 5

Results and Discussions:

The analytical modeling has been developed based on device physics to study the gate-source capacitance, gate-drain capacitance, switching time of GaN OPFET for high frequency and switching applications. Ion implantation technique is applied to fabricate the GaN MESFET to study the effect of light intensity under dark and optical conditions and various observations are as follows

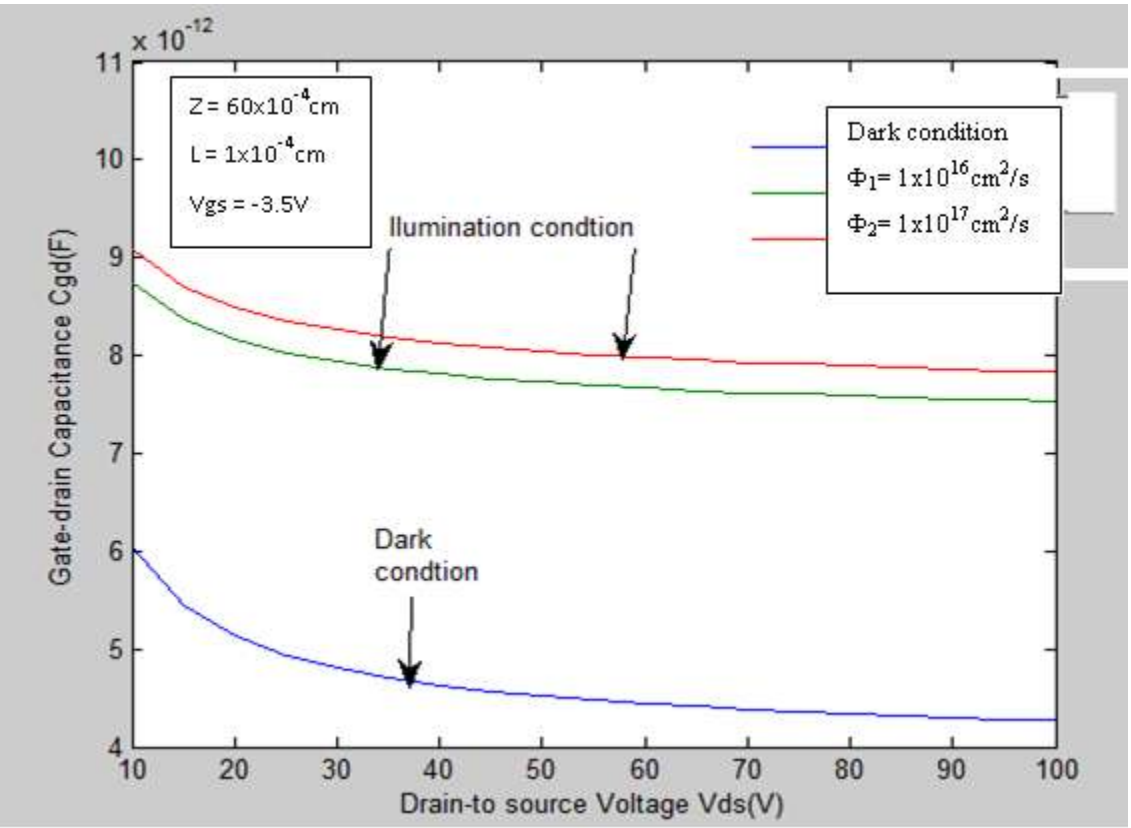

Figure 14 Plot of Gate-to-Drain Capacitance (C_{DS}) vs. Drain-to-Source Voltage (V_{DS}) at different flux density

Figure 14 shows the gate-to-drain capacitance versus drain-to-source voltage for dark condition and different light illumination with light flux density (ϕ) of $2.0x10^{16}$, and $1x10^{17}$ /cm^2.s respectively. The capacitance in the dark condition shows the value of $6x10^{-12}$f at the drain-source voltage of 10V and the capacitance value exponentially decreases to the value of $4.3x10^{-12}$f for successive decreasing of drain-source voltage up to 100V. The capacitances in the light illumination condition for flux density of $1.0x10^{16}$

/cm^2.s, 1.0x10^{17} /cm^2.s follow the same nature. The photo response in the flux density of 2.0x10^{16} cm^{-2}.s and 1x10^{17} cm^{-2}.s densities of shows that the capacitances of 9.1x10^{-13}f and 8.8x10^{-13}f at V_{DS} = 10V exponentially decay up to 7.8x10^{-13}f and 7.5x10^{-13}f at V_{DS} = 100V. The excess carrier has been generated due to the light illumination and therefore the increment charge results in higher capacitance value compared to the dark condition.

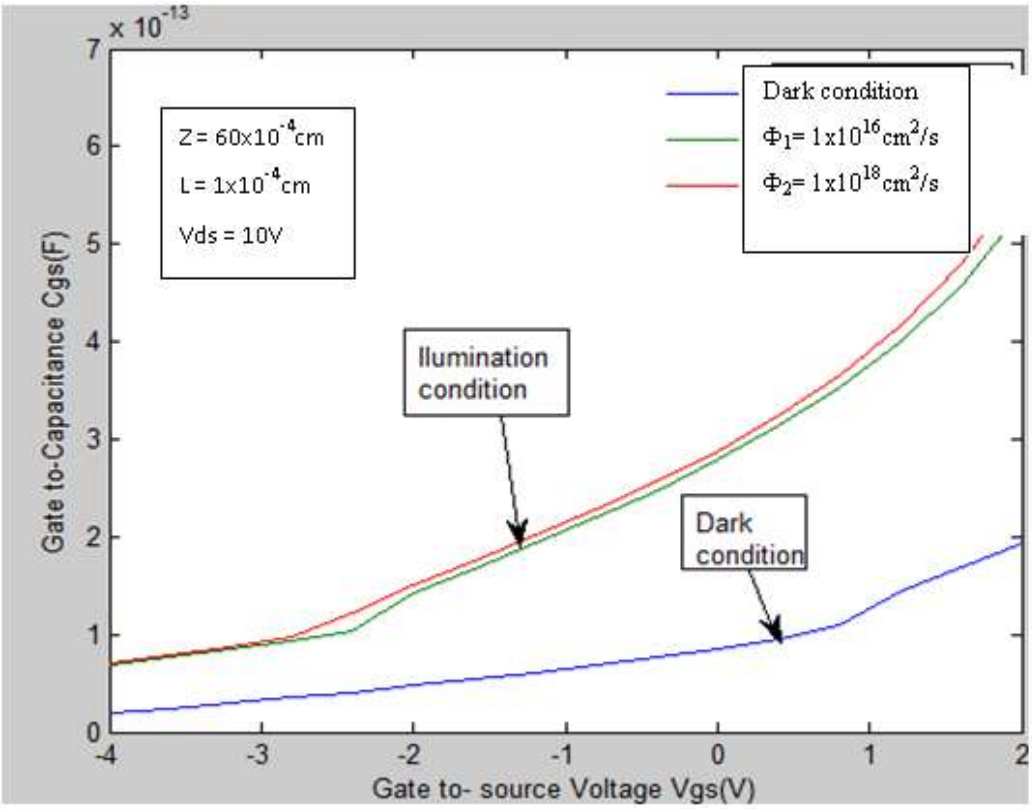

Figure 15 Plot of Gate-to-Source Capacitance (C_{GS}) vs. Gate-to-Source Voltage (V_{GS}) at different flux densities

The Figure 15 shows a plot of gate-to-source capacitance (C_{GS}) versus gate-to-source voltage (V_{GS}) at dark condition and different flux densities ϕ_L = 1x10^{16} and 1x10^{18} /cm^2.s and the plot has been obtained by using the equation (4d). At dark condition, the gate-to-source capacitance (C_{GS}) shows the value of 0.25x10^{-13}f at gate-source voltage (V_{GS}) = -4.0V and the capacitance exponentially increases up to 1.95x10^{-14}f for successive increment of gate-source voltage up to V_{GS} = 2V. The obtained values of gate-to-source capacitance (C_{GS}) at different flux densities ϕ_L = 1x10^{16} and 1x10^{18} /cm^2.s are approximately in the range of .85x10^{-13}f at gate-source voltage (V_{GS}) = -4.0V. The gate-to-source capacitances (C_{GS}) at different flux densities exponentially increase to the value

of $5.6x10^{-13}$f and $5.3x10^{-13}$f up to the gate-to-source voltage (V_{GS}) increasing up to 2V. The capacitance increment in the illumination conditions happens due to the generation of carrier, which in-turn increases the carrier charge to increase more capacitance compared to the dark condition.

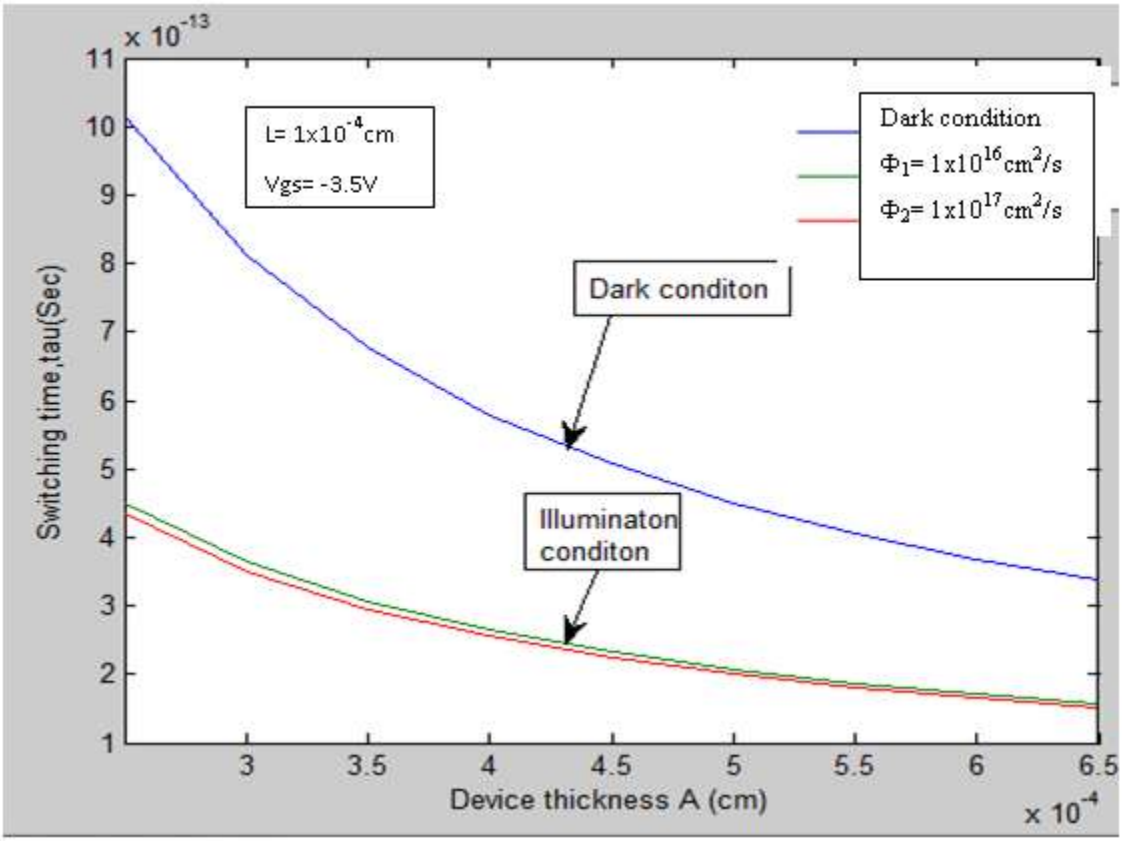

Figure 16 Plot of Switching time (τ) vs. Device thickness (A) for dark condition at different flux densities

The figure 16 shows a plot of switching time (τ) versus device thickness (A) for dark condition and different flux densities $\phi = 1x10^{16}$ $cm^{-2}s$ and $1x10^{17}$ $cm^{-2}s$ and the plot has been generated by using the equation (4k). The switching time shows the value of $10.1x\ 10^{-13}$sec and $3.4x10^{-13}$sec for device channel thickness (A) in the range of $1x10^{-4}$ cm – $6.5x10^{-4}$cm respectively at the dark condition. The switching times more decreases in the presence of light illumination at $\phi = 1x10^{16}$ $cm^{-2}s$ and $1x10^{17}$ $cm^{-2}s$ compared to the dark condition. The switching time shows the value in the range of $4.451x\ 10^{-13}$sec - $1.75x10^{-13}$sec and $4.2x\ 10^{-13}$sec - $1.5x10^{-13}$sec respectively for device channel thickness (A) in the rage of $1x10^{-4}$ cm – $6.5x10^{-4}$cm. The switching time for both dark and illumination

conditions exponentially decreases for different active channel thicknesses in the range of $1x10^{-4}$ cm – $6.5x10^{-4}$cm. The photogenerated carriers incorporate the photovoltaic effect, which is mainly responsible to increase the switching speed. The highest switching speed has been observed for high light flux density $\phi = 1x10^{17}$ $cm^{-2}s$ because large number of photogenerated carriers, which is translated to high photovoltaic effect.

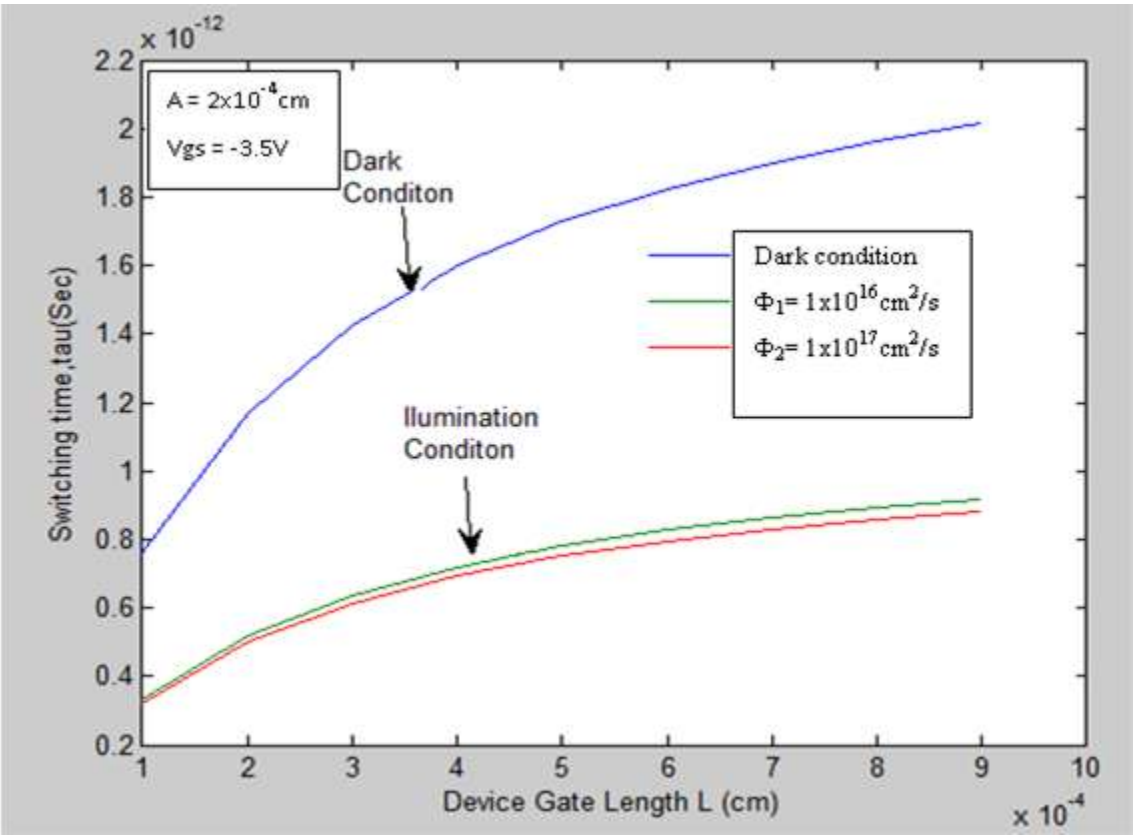

Figure 17 Plot of Switching time (τ) vs. Device Gate Length (L) at different flux densities

Figure 17 presents a plot of switching time (τ) versus MESFET device gate Length (L) for dark condition and illumination condition with different flux density $\phi = 1x10^{16}$ $cm^{-2}s$ and $1x10^{17}$ $cm^{-2}s$ and the plot has been drawn using the equation (4k). The switching time at dark condition for gate length value $1x10^{-4}$cm shows the value of $0.78x10^{-12}$sec, which exponentially increases up to $2x10^{-12}$sec with increment of gate length up to $10x10^{-4}$cm. The switching time increases with the increment of gate length variation of $1x10^{-4}$cm $-10x10^{-4}$cm for dark and illumination conditions, which shows the opposite nature of previous plot. The switching time increases with the increase of gate length because the transit time increases with the increment of gate length.

CHAPTER 6

Conclusion

Analytical modeling based on device physics has been carried out for the evaluation of intrinsic parameters such as gate capacitances at dark and optical conditions and the switching time is obtained for different device active layer thickness and active channel length of GaN MESFET.

The results of those intrinsic parameters such as gate-to-source capacitance and gate-to-source capacitance and switching time indicate the excellent potential of the device for high frequency amplifier application for space and device communication. This excellent feature also allows this device to be applied in the field of communication in high temperature environment.

The present analytical model offers an avenue of accurate optimization of the device physical design and fabrication process design suitable for optoelectronic devices fabrication.

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APPENDIX – A

Notations and Symbols Used:

Rp: Effective ion Implant Range Parameter

σ: Implant Straggle Parameter

ε: SiC Dielectric Constant/Permittivity of SiC

K: Boltzmann constant

q: Electronic charge

T: Absolute temperature at 300K

Z: Device length

L: Channel length

μ: Carrier mobility in SiC

Φb: Metal-Semiconductor Work function difference/Titanium Schottky barrier height

Vbs: Substrate to source voltage

Vgs: Gate-Source voltage

Vds: Drain-Source voltage

Vt: Threshold voltage

Vbi: Build in Voltage of active channel and Substrate junction

Vp: Pinch-off Voltage

N(x,t): Impurity doping concentration of diffused active layer

Na: Substrate doping concentration

Nd: Effective average channel doping concentration

Xdg: Distance from surface to edge of gate depletion region in the channel

Xds: Distance from surface to edge of substrate depletion region in the channel

a: Active layer thickness

Q: Ion Implant Dose

Δ: Depth of Fermi level below the Conduction band

kT/q: Thermal Voltage = 0.0259V at T = 300 K;

t: Annealing time

Cgd: Gate-Drain capacitance

Cgs: Gate-Source capacitance

$g_{m:}$ Transconductance

t_{gs}, t_{gd} : time constants

T_t: Total time constant(t_{gs}+t_{gd})

Ndavg: Average Channel doping concentration

APPENDIX – B

MATLAB Codes

MatLab code for Gate-Drain capacitance (Cgd) Vs Drain-Source voltage (Vds) at different ion doses

```
clc;

Na=0.5e18;

sigma=20e-7;

Vbs=0;

phib=0.8;

Vp=5.0;

eps=78.80e-14;

q=1.60218e-19;

u=900;

Z=1000e-4;

Rp=40e-7;

L=1e-4;

K1 = 1.3806e-23;

T1 = 300;

D=2.3e-21;

x = 0.1e-4;

t=7.5e6;

Vds=10:5:100;

ni = 1.9e-10;

Vgs=-3.5;

alpha=(Rp/(2*sigma))*(sqrt(3.14/2));

delta=0.018;
```

```
tn=1e-8;

A3=1-exp(-((Rp/sqrt(2*((sigma*sigma)+(2*D*t))))^2)) -
((2*alpha*erf(Rp/sqrt(2*((sigma*sigma)+(2*D*t))))));

A1=(alpha*alpha)+A3;

Ndavg=1.5e16;

S=sqrt((q*Ndavg)/(2*eps));

Qion=1.5e13;

%Impurity flux phi1=0 dark condition

phi1=0;

deltap1 = (phi1*alpha)* exp (-alpha*x);

p11 = (ni*ni)/Na;

P21= p11 + deltap1;

Vop1 = (0.0259*log(P21/p11));

N1=phib-Vgs-delta-Vop1;

R1=phib+Vds-Vgs-delta-Vop1;

M1=(4*alpha*eps)/(q*Qion*Rp);

x11=(q*Qion*Z*L)/2;

x21=(M1)./(2.*sqrt((M1.*N1)+A1));

x31=sqrt(R1)./(2.*(sqrt(N1)-sqrt(R1)).*(sqrt(N1)-sqrt(R1)));

x41=sqrt(((M1*R1)+A1)./N1);

x51=(M1.*(sqrt(N1)-sqrt(R1))./sqrt((M1.*N1)+A1));

x61=(sqrt((M1.*R1)+A1))./sqrt(N1);

%z71=(1/Qion)*(sqrt((2*Na*eps)/q));

x71=(q*Z*L*tn*phi1*S)./(2*alpha);

x81=(2.*(sqrt(N1)-sqrt(R1)))/(sqrt(R1));
```

```
x91=(Vds)/(sqrt(R1.*N1));

W1=(x11).*(x21+x31.*(x41-x51-x61-x71.*(x81-x91)))+((3.14*eps*Z)./2);


phi2=1e16;

deltap2 = (phi2*alpha)* exp (-alpha*x);

p11 = (ni*ni)/Na;

Q21= p11 + deltap2;

Vop2 = (0.0259*log(Q21/p11));

N2=phib-Vgs-delta-Vop2;

R2=phib+Vds-Vgs-delta-Vop2;

M1=(4*alpha*eps)/(q*Qion*Rp);

a11=(q*Qion*Z*L)/2;

a21=(M1)./(2.*sqrt((M1.*N2)+A1));

a31=sqrt(R2)./(2.*(sqrt(N2)-sqrt(R2)).*(sqrt(N2)-sqrt(R2)));

a41=sqrt(((M1*R2)+A1)./N2);

a51=(M1.*(sqrt(N2)-sqrt(R2))./sqrt((M1.*N2)+A1));

a61=(sqrt((M1.*R2)+A1))./sqrt(N2);

%z71=(1/Qion)*(sqrt((2*Na*eps)/q));

a71=(q*Z*L*tn*phi2*S)./(2*alpha);

a81=(2.*(sqrt(N2)-sqrt(R2)))/(sqrt(R2));

a91=(Vds)/(sqrt(R2.*N2));

W2=(a11).*(a21+a31.*(a41-a51-a61-a71.*(a81-a91)))+((3.14*eps*Z)./2);


phi3=1e17;

deltap3 = (phi3*alpha)* exp (-alpha*x);

p11 = (ni*ni)/Na;
```

```
U21= p11 + deltap3;

Vop3 = (0.0259*log(U21/p11));

N3=phib-Vgs-delta-Vop3;

R3=phib+Vds-Vgs-delta-Vop3;

M1=(4*alpha*eps)/(q*Qion*Rp);

b11=(q*Qion*Z*L)/2;

b21=(M1)./(2.*sqrt((M1.*N3)+A1));

b31=sqrt(R3)./(2.*(sqrt(N3)-sqrt(R3)).*(sqrt(N3)-sqrt(R3)));

b41=sqrt(((M1*R3)+A1)./N3);

b51=(M1.*(sqrt(N3)-sqrt(R3))./sqrt((M1.*N3)+A1));

b61=(sqrt((M1.*R2)+A1))./sqrt(N2);

%z71=(1/Qion)*(sqrt((2*Na*eps)/q));

b71=(q*Z*L*tn*phi3*S)./(2*alpha);

b81=(2.*(sqrt(N3)-sqrt(R3)))/(sqrt(R3));

b91=(Vds)/(sqrt(R3.*N3));

W3=(b11).*(b21+b31.*(b41-b51-b61-b71.*(b81-a91)))+((3.14*eps*Z)./2);

plot(Vds,W1,Vds,W2,Vds,W3);

xlabel('Drain-to source Voltage Vds(V)');
ylabel('Gate-drain Capacitance Cgd(F)');
legend('0/cm^2','1e16/cm^2','1e17/cm^2','Location','northeast');
```

Matlab code for Gate-to-Source Capacitance (C_{GS}) vs. Gate-to-Source Voltage (V_{GS}) at different ion doses.

```
clc;

Na=0.5e18;

sigma=20e-7;
```

```
%Vbs = 0;

Vds=10;

Vbi=3.1728;

%Vp=5.0;

eps=78.80e-14;

q=1.60218e-19;

ni=1.9e-10;

tn=1e-7;
phib=0.8;

%u=900;

Z=60e-4;

Rp=40e-7;

L=1e-4;

D = 2.3e-21;

t=7.5e6;

Vgs=-4:0.4:2;

alpha=(Rp/(2*sqrt((sigma*sigma)+(2*D*t))))*sqrt(3.14/2);

a=exp(((Rp/sqrt(2*((sigma*sigma)+(2*D*t)))))*((Rp/sqrt(2*((sigma*sigma)+(2*D*t))))));

b=erf(Rp/sqrt(2*((sigma*sigma)+(2*D*t))));

A3=a-(2*alpha*b);

A1=(alpha*alpha)+A3;

delta=0.018;

x= 0.1e-4;

Ndavg=1.5e16;

Qion=1.5e13;
```

```
S=sqrt((q*Ndavg)/(2*eps));


%dark condition phi=0;
phi1=0;

deltap1 = (phi1*alpha)* exp (-alpha*x);

p11 = (ni*ni)/Na;

P21= p11 + deltap1;

Vop1 = (0.0259*log(P21/p11));

N1=phib-Vgs-delta-Vop1;

R1=phib-Vds-Vgs-delta-Vop1;

M1=(4*alpha*eps)/(q*Qion*Rp);

c11=(q*Qion*Z*L)/2;

c21=(M1)./(2.*sqrt((M1*R1)+A1));

c31=(sqrt(N1))./(2.*(sqrt(N1)-sqrt(R1)).^2);

c41=sqrt(((M1.*N1)+A1)/R1);

c51=(M1.*(sqrt(N1)-sqrt(R1))./(sqrt((M1*R1)+A1));

c61=sqrt(((M1*R1)+A1)/R1);

c71=(q*Z*L*tn*phi1*S)./(2*alpha);

%c71=(1/Qion)*(sqrt((2*Na*eps)/q))-t71;

c81=(2.*(sqrt(N1)-sqrt(R1)))/(sqrt(R1));

c91=(Vds)./(sqrt(R1.*N1));

Y1=(c11).*(c21+(c31.*(c41-c51-c61-c71.*(c81-c91))))+((1.57*eps*Z));


phi1=1e16;

deltap2 = (phi2*alpha)* exp (-alpha*x);

p11 = (ni*ni)/Na;
```

```
Q21= p11 + deltap2;

Vop2 = (0.0259*log(Q21/p11));

N2=phib-Vgs-delta-Vop2;

R2=phib-Vds-Vgs-delta-Vop2;

M1=(4*alpha*eps)/(q*Qion*Rp);

b11=(q*Qion*Z*L)/2;

b21=(M1)./(2.*sqrt((M1*R2)+A1));

b31=(sqrt(N2))./(2.*(sqrt(N2)-sqrt(R2)).^2);

b41=sqrt(((M1.*N2)+A1)/R2);

b51=(M1.*(sqrt(N2)-sqrt(R2)))./(sqrt((M1*R2)+A1));

b61=sqrt(((M1*R2)+A1)/R2);

b71=(q*Z*L*tn*phi2*S)./(2*alpha);

%b71=(1/Qion)*(sqrt((2*Na*eps)/q))-t71;

b81=(2.*(sqrt(N2)-sqrt(R2)))/(sqrt(R2));

b91=(Vds)./(sqrt(R2.*N2));

Y2=(b11).*(b21+(b31.*(b41-b51-b61-b71.*(b81-b91))))+((1.57*eps*Z));


phi3=1e18;

deltap3 = (phi3*alpha)* exp (-alpha*x);

p11 = (ni*ni)/Na;

R21= p11 + deltap3;

Vop3 = (0.0259*log(R21/p11));

N3=phib-Vgs-delta-Vop3;

R3=phib-Vds-Vgs-delta-Vop3;

M1=(4*alpha*eps)/(q*Qion*Rp);
```

```
a11=(q*Qion*Z*L)/2;

a21=(M1)./(2.*sqrt((M1*R3)+A1));

a31=(sqrt(N3))./(2.*(sqrt(N3)-sqrt(R3)).^2);

a41=sqrt(((M1.*N3)+A1)/R3);

a51=(M1.*(sqrt(N3)-sqrt(R3)))./(sqrt((M1*R3)+A1));

a61=sqrt(((M1*R3)+A1)/R3);

a71=(q*Z*L*tn*phi1*S)./(2*alpha);

%a71=(1/Qion)*(sqrt((2*Na*eps)/q))-t71;

a81=(2.*(sqrt(N3)-sqrt(R3)))/(sqrt(R3));

a91=(Vds)./(sqrt(R3.*N3));

Y3=(a11).*(a21+(a31.*(a41-a51-a61-a71.*(a81-a91))))+((1.57*eps*Z));


p=plot(Vgs,Y1,Vgs,Y2,Vgs,Y3);
xlabel('Gate to- source Voltage Vgs(V)');
ylabel('Gate to-Capacitance Cgs(F)');
legend('0/cm^2','1e16/cm^2','1e18/cm^2','Location','northeast');
```

Matlab code for Calculating Ndavg to determine switching time against Active layer thickness (A) and channel length (L)

```
clc;

Na=1e15;

sigma=20e-7;

Vbs=0;

Vgs=3.5;

Vbi=3.178;

Vp=0.8117;

epso=78.80e-14;
```

```
q=1.60218e-19;

u=1000;

Z=600e-4;

Rp=40e-7;

L=10e-4;

D = 2.3*10^(-21);

t=2.7e3;

phi = 3e10;

pi = 3.14;

n11 = sqrt(2*pi);

n21 = sigma*sigma + (2*D*t);

n31 = sqrt(n21);

n41 = n11*n31;

n51 = -Rp/2*n21;

n61= exp(n51);

Ndavrg = (phi/n31)* n61;

display(Ndavrg);
```

Matlab code for Switching time (τ) vs. Device thickness (A) at different flux density

```
clc;

pi=3.14;

%phib = 0.94;

q = 1.6e-19;

L=1e-4;

epselon = 78.80e-14;

sigma = 20e-7;

D = 2.3e-21;

phibn =0.8;
```

```
Ndavg = 1.5e16;


Vs= 25e6 ;
Rp = 40e-7;
alpha = 1e-4;
Tn = 1e-7;
ni = 1.9e-10;
T = 1473;
T1 = 300;
Na = 0.5e18;


%A = 2e-4:1e-4:10e-4;
A = 2.5e-4:0.5e-4:6.5e-4;
%A = 2.1e-4: 0.2e-4:3.8e-4;
K1 = 1.3806e-23;
Nc = 1.2e18;
x = 0.1e-4;
Vgs = -3.5;
t=2.7e3;
Vg = -3.2;

phi1 = 0;
deltap1 = (phi1*alpha)* exp (-alpha*x);
p11 = (ni*ni)/Na;
P21= p11 + deltap1;
Vop1 = ((K1*T1)/(q))*log(P21/p11);

c0= 0.7-Vop1-Vg;
d0= q*Ndavg;
e0= 2*epselon*c0;
a0= sqrt(e0/d0);
```

```
f0= A-a0;
g0= L*a0;
h0= Vs*f0;
tau1= g0./h0;

phi2 = 1e16:1e16:9e16;
deltap2 = (phi2*alpha)*exp (-alpha*x);
q11 = (ni*ni)/Na;
Q21= q11 + deltap2;
Vop2 = ((K1*T1)/(q))*log(Q21/q11);
c1= 0.7-Vop2-Vg;
d1= q*Ndavg;
e1= 2*epselon*c1;
a1= sqrt(e1/d1);
f1= A-a1;
g1= L*a1;
h1= Vs*f1;
tau2= g1./h1;

phi3 = 1e17:1e17:9e17;
deltap3 = (phi3*alpha)*exp (-alpha*x);
r11 = (ni*ni)/Na;
R21= q11 + deltap3;
Vop3 = ((K1*T1)/(q))*log(R21/r11);
c2= 0.7-Vop3-Vg;
d2= q*Ndavg;
e2= 2*epselon*c2;
a2= sqrt(e2/d2);
f2= A-a2;
g2= L*a2;
h2= Vs*f2;
tau3= g2./h2;
```

```
% plot(A,tau1);
% plot(A,tau2);
% plot(A,tau3);
plot(A,tau1,A,tau2,A,tau3);
 xlabel('Device thickness A (cm)');
 ylabel('Switching time,tau(Sec)');
legend('0/cm^2','1.0e16/cm^2','1.0e17/cm^2','Location','northeast');
```

Matlab code for Switching time (τ) vs. Active Channel length (L) at different flux density

```
clc;
pi=3.14;
%phib = 0.94;
q = 1.6e-19;

epselon = 78.80e-14;
sigma = 20e-7;
D = 2.3e-21;
phibn =0.8;
Ndavg = 3.8e16;
Vs= 25e6 ;
Rp = 40e-7;
alpha = 1e-4;
Tn = 1e-7;
ni = 1.9e-10;
T = 1473;
T1 = 300;
Na = 0.5e18;

A = 2e-4:0.5e-4:6e-4;
%A = 1.2e-4;
L = 1e-4:1e-4:9e-4;
```

```
%A = 2.1e-4: 0.2e-4:3.8e-4;
K1 = 1.3806e-23;
Nc = 1.2e18;
x = 0.1e-4;
Vgs = -3.5;
t=7.5e6;
Vg = -3.2;
phi1 = 0
deltap1 = (phi1*alpha)* exp (-alpha*x);
p11 = (ni*ni)/Na;
P21= p11 + deltap1;
Vop1 = ((K1*T1)/(q))*log(P21/p11);

c0= 0.7-Vop1-Vg;
d0= q*Ndavg;
e0= 2*epselon*c0;
a0= sqrt(e0/d0);
f0= A-a0;
g0= L.*a0;
h0= Vs*f0;
tau1= g0./h0;

phi2 = 1e17:1e17:9e17;
deltap2 = (phi2*alpha)*exp (-alpha*x);
q11 = (ni*ni)/Na;
Q21= q11 + deltap2;
Vop2 = ((K1*T1)/(q))*log(Q21/q11);
c1= 0.7-Vop2-Vg;
d1= q*Ndavg;
e1= 2*epselon*c1;
a1= sqrt(e1/d1);
f1= A-a1;
g1= L.*a1;
```

```
h1= Vs*f1;
tau2= g1./h1;

phi3 = 1e18:1e18:9e18;
deltap3 = (phi3*alpha)*exp (-alpha*x);
r11 = (ni*ni)/Na;
R21= q11 + deltap3;
Vop3 = ((K1*T1)/(q))*log(R21/r11);
c2= 0.7-Vop3-Vg;
d2= q*Ndavg;
e2= 2*epselon*c2;
a2= sqrt(e2/d2);
f2= A-a2;
g2= L.*a2;
h2= Vs*f2;
tau3= g2./h2;

% plot(A,tau1);
% plot(A,tau2);
% plot(A,tau3);
plot(L,tau1,L,tau2,L,tau3);
 xlabel('Active Device Length A (cm)');
 ylabel('Switching time,tau(Sec)');
legend('0/cm^2','1.0e17/cm^2','1.0e18/cm^2','Location','northeast');
```