CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

Simulation of Si CMES Using Synopsys Sentaurus TCAD Tools

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By
Malav Shah

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The graduate project of Malav Shah is approved:

_____	_____
Dr. Ramin Roosta	Date
_____	_____
Dr. Emad A Elwakil	Date
_____	_____
Dr. Somnath Chattopadhyay, Chair	Date

California State University, Northridge

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ABSTRACT

Simulation of Si CMES Using Synopsys Sentaurus TCAD Tools.

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This paper is concentrated on the development of a complete complementary silicon MESFET technology. The basic difference between MOS and MES are pointed out and design criteria for CMES inverters using are elaborated. The completely theory that include non-uniform channel doping analysis and ion-implantation model analysis would be presented. Physics of the MESFET includes the Schottky barrier, and the charge sheet phenomena in the channel of the MESFET device. At present, nano-meter grid CMOS suffers from hot electron effect, drain induced barrier lowering (DIBL), (GIDL), etc. and this is main reason blocking of CMOS roadmap for nano-meter scaled CMOS. CMES showed potential application to surmount this barrier to deliver nano-scaled digital logic. Further, the TCAD tool has been used for the semiconductor device simulation. Simulation of Fabrication steps for complementary MESFET device is done in Sentaurus Sprocess simulator. Structure for p-MES and n-MES is also developed in Sprocess simulator. The design process has been performed step-by-step and it would be helpful for reader to do well with this TCAD tools software. In-order to demonstrate the simulation results of a complementary silicon MESFET device, the drain current versus gate-source voltage, drain current versus drain voltage and transient response analysis of CMES device has been presented. Complementary silicon MESFET technology could provide a VLSI and ULSI alternative which as a radiation hardness approaching that of GaAs with the integration density of silicon technology.

CHAPTER 1

Introduction

In current scenario of semiconductor technology, scaling down of the devices is more and more progressing. As a result, the simulation of submicron semiconductor devices requires advanced transport models. Because of highly variable varying electric fields, phenomena happen which cannot be described by the common well-known drift-diffusion models, which does not include energy as a dynamical member variable. Because of the same generalization has been sought in order to obtain more precise models such as hydrodynamical and energy-transport models. In-case of energy transport models which are currently implemented in commercial simulators are mostly based on phenomenological constitutive equations for the particle flux and energy flux depending on a series of the set of parameters which are fitted to homogeneous bulk material Monte Carlo simulations [1].

The leading device used in modern VLSI circuits today is the MOS transistor. It is well known that improvements in MOSFET operation occur with reductions in device dimensions. As technology has advanced several limitations of MOSFET's have become apparent such as hot electron effects with their known associated threshold voltage shifts, short channel effects, and also the practical technological problems of shrinking junctions and growing high integrity, low defect, thin gate oxides [2]. Effective carrier mobility in MOSFET's is often on the order of half the bulk mobility. The decrease is caused by various scattering mechanisms, such as: phonon, Columbic, and surface roughness scattering [3]**.** As devices scale, higher perpendicular electric fields give rise to increased scattering, particularly by surface roughness. In scaled devices, where the normal electric field can reach several megavolts per centimeter, the electron and hole mobilities are reduced to less than 300 and 100 cm^2/V - s, respectively [4]. Present MOS technology relies almost exclusively upon polysilicon as the gate material and local interconnect medium. Due to the high resistivity of polysilicon and the problems with

scaled interconnects, low resistivity silicides or metals are sometimes used for local interconnects [5-7]. These low-resistivity materials, however, form an inferior interface with SiO_2; greatly reduced gate oxide breakdown voltages are encountered. This has led to complex layered structures in which a low-resistivity metal or silicide is placed or reacted directly on the poly-silicon gate to shunt the resistance which increases process complexity. This technique works well at present integration levels; however, as scaling continues, the resistivity of the gate interconnect must be reduced further. Further reduction of polysilicon interconnect resistance by forming a thicker silicide layer will further compromise gate breakdown voltages [8]. MESFET's, with their absence of gate oxides, naturally low-resistivity gate interconnect, and bulk mobility circumvent many of these problems.

1.1 State-of-art CMES

The metal semiconductor field effect transistor (MESFET) was proposed by Mead in 1966 and was eventually fabricated on a GaAs epitaxial layer [9]. The absence of a gate oxide makes the MESFET structure naturally immune to radiation and hot-carrier-induced threshold-voltage shifts or transconductance degradations.

Circuit speed is one of the most important performance parameters in the operation of an integrated circuit. Speed is predominantly determined by the intrinsic device speed and its current drive capability. To maximize these, the intrinsic transconductance of the device must be maximized and the parasitic resistance of the device and circuit minimized. Until recently, the current drive of MESFET's suffered relative to MOSFET's due to an inability to implant self-aligned source/drain regions. This inability complicated the fabrication of MESFET's. In 1976, MESFET's were fabricated by lithographically defining the gate and source/drain regions separately [10]. This gave transconductances of about 5 mS/mm for a 2-μm gate length. A few years later, Texas Instruments employed a type of self-aligned process with an

intermediate doping region between the channel and source/drain regions to decrease the extrinsic channel parasitic resistance. Ultra short gate lengths were fabricated in this study [11], but for 2-μm device gate lengths, this technique only slightly improved the transconductance.

The first truly self-aligned MESFET was fabricated by using SiO_2 sidewall spacers alongside the Schottky-gate contact [12]. This enabled the source/drain regions to be implanted in the same self-aligned fashion as MOSFET's, simplifying fabrication and providing excellent control of the source/drain offset distance. However, since the gate structure of the MESFET makes intimate contact with the silicon surface, thermal cycling after gate formation (and thus source/drain implant) must be minimized to prevent excessive gate material/silicon reactions. This may not allow full activation of the source/drain implant. Thus though a large reduction in the channel extension resistance is accomplished with this process, it is partially offset by an increase in the resistance of the source/drain contacts and diffusions. A transconductance value of about 8 mS/mm is estimated for a 2-μm device [13].

1.2 Performance limits of CMOS versus CMES.

As CMOS based VLSI technology has advanced for VLSI, the limitations of CMOS have become evident, including: hot carriers, velocity saturation, parasitic source-drain series resistance, finite channel thickness [14] drain-induced barrier lowering (DIBL) [15], short channel effect due to charge sharing in channel, punch–through, and tunneling currents [16]. Gate leakage current is a well-recognized challenge to continued MOSFET scaling. Scaling effects on direct tunneling gate leakage current was analyzed by utilizing 3D device simulation. The results show that the scaling of the gate width cannot suppress the gate leakage [17]. Due to deep submicron scaling in CMOS devices, the effective gate length decreases have lead to leakage currents such as subthreshold leakage due to threshold voltage reduction, gate

edge-direct-tunneling leakage and gate-induced drain-leakage (GIDL) due to reduced gate oxide thickness, and band to band tunneling leakage current due to LDD increase to degrade the device performance [18]. Despite current efforts to produce gate dielectric material formed by oxynitrided SiO_2 and even high-k dielectrics, several potential limitations could be challenging for continued scaling of all gate dielectric, regardless of the material. The decreasing oxide thickness for scaling CMOS increases the effective electric field in the channel pulling the carriers in the channel closer against the dielectric interface, which increases the phonon scattering and thereby decreases the channel carrier mobility [19]. The effect of High-k gate dielectric on deep submicrometer CMOS devices has been studied by 2-D device and Monte Carlo Simulation and the result shows that the lower parasitic outer fringe capacitance is beneficial to circuit performance, but the increase in internal fringe capacitance will degrade the short channel performance, contributing to higher DIBL (drain induced barrier lowering), drain leakage, and low noise margin [20]. Several areas of investigation may be required before HFO2-based MOS technology is ready for the harsh environments encountered in space exploration because atomic scale defects were found by radiation damage [21]. MESFETs do not require thin gate oxides and are therefore not susceptible to the problems of threshold voltage shifts and transconductance degradation due to the hot carrier effects.

1.3 MESFET immune to Radiation effect

The radiation of neutrons originate from spallation reactions, initiated when galactic cosmic rays and solar particles collide with nuclei of oxygen and nitrogen in the atmosphere and produce pions, muons, electrons, gamma rays, protons, and neutrons [22]. The galactic cosmic radiation submerges the earth with the composition of about 88% protons, 9% helium ions, 1% heavier particles, and 2% electrons [23]. Thus the resultant radiations are of great concern in space and earth in terms of the impact of single event upsets (SEUs) on CMOS based memory and microprocessor chips. Detailed descriptions of the impact of single event

effects (SEEs) on semiconductor devices in avionics have been presented by the Boeing Radiation Effects lab [24]. SEUs that cause soft errors are generated by cosmic particles, energetic neutron and proton and alpha particles hitting the surface of silicon devices. After 24-GeV proton irradiation on 0.13-μm CMOS devices, large negative shifts in the threshold voltage and large drops in the maximum transconductance were observed in P-MOSFETs, whereas comparatively smaller effects were present in N-MOSFETs [25]. CMOS devices and circuits can fail in space [26- 27] because of radiation-induced (RI) oxide-trap/ interface-trap charge buildup [28] and RI leakage currents [29-31], threshold voltage shift [28, 32-35], flat-band voltage, transconductance reduction [36], propagation delay increase [37], and radiation-induced latch-up [38, 39]. RI breakdown in oxynitrided gate oxide [40] is mainly responsible for CMOS device failures. At a total dose of 100 Mrad (GaAs), slight shifts in the threshold voltage of GaAs MESFET (approximately 5 mV) and insignificant reduction of transconductance have been observed, whereas the threshold voltage shift amount to volts for MOSFET has been observed due to charge buildup in the oxide under radiation effect [41-42]. The radiation dose and threshold voltage shift (ΔV_T) with each failure mode in a commercial CMOS circuit has been observed as $8x10^{12}$ rad(Si): ΔV_T = -0.2V, $5x10^{13}$ rad(Si): ΔV_T = - 1.0 V, $1x10^{14}$ rad(Si): ΔV_T = - 2.0 V and $3x10^{14}$ rad(Si): ΔV_T = - 4.0 V [43].

On the basis of different I-V characterization under high fluence of ~60MeV protons, the radiation response of 90 nm CMOS with physical gate oxide thickness of 1.75 to 2.30 nm, under +ve gate bias of 1.2V, showed a catastrophic failure [44]. The radiation induced leakage current and SEU cross-section, versus LET of CMOS from the advanced commercial foundry technology, showed the failure dose of different foundries [45]. No degradation has been observed in the DC characteristics of GaAs MESFET up to the total dose of 55Mrad; variations in DC properties have been observed for CMOS devices under ionizing radiation [46]. Three possible ion induced charge collection mechanisms for GaAs MESFET fabricated on a SI substrate were found to originate from (1) drift of carriers within the channel depletion region,

(2) a bipolar-gain mechanism and (3) back-channel modulation [47]. One solution that has been proposed to minimize the effects of these mechanisms is to fabricate the MESFET on low temperature (LT) grown GaAs substrates [48-50]. The following SEU cross-section (SEUCS) values have been reported for five E/D MESFET GaAs logic families [51] and presented in table 1.

Family	SEUCS range (cm^2)	LET Range (MeV-cm^2/mg)
DCFL	5x10^-8 - 6x10^-6	0.8 – 4
SDFL	4x10^-8 - 4x10^-6	0.8 – 4
FFL	1x10^-7 - 5x10^-6	0.3 – 4
BFL	1x10^-7 - 8x10^-6	0.3 – 4
LPFL	1x10^-7 - 5x10^-5	0.3 – 4

Table 1

Whereas SEUCS of 10^{-7}-10^{-4} cm^2 for LET 18 – 60 MeV-cm^2/mg was observed from CD 54HHCT 174F CMOS SEU test report [52].

1.4 Noise performance

Noise phenomena in nanoscale MOSFET consist of the distributed gate and substrate resistance noise [53, 54], substrate current supershot noise, 1/f noise originating from higher density oxide trapping [55], excess channel thermal noise due to hot electron effect [56], flicker noise originating from interaction between free carriers and oxide traps charge via surface states [57], effects of radiation [58], gate induced and gate current shot noise due to gate capacitance and gate leakage current [59]. For low noise amplifier applications, the PHEMT is generally recognized as the best choice, followed by the MESFET. Recent results obtained on GaAs MESFETs have demonstrated that the cut-off frequency of MESFET can be

equal or higher than that of HEMT, and noise performance is comparable to that of HEMT with the same geometry, but at higher cost [60-63]. The main source of noise in FETs is thermal-diffusion, as a result of random variations in carrier speed in the device channel, leading to current variations. Of particular importance is the presence of capacitive coupling between the gate and the channel, which results in the overall noise being determined by subtracting part of the gate noise from the drain noise. This is a unique property of FETs, which leads to very low-noise performance [64]. The trap generation-recombination in a depletion region was found to be a dominant source of low frequency noise in MESFETs [65], which seems to be old growth process technology causing trap centers. However, the present technology for growth process of GaAs has matured considerably, minimizing such trap centers. The hot electron noise in GaAs MESFET is significantly important at microwave and millimeter wave range [66, 67] but has no effect on digital applications. Improvement in the noise figure results from the decrease in gate length and from choosing unit gate width sufficiently shorter to minimize gate resistance [68]. Hence, noise performance of GaAs MESFET should be much lower than MOS and bipolar devices.

1.5 Power-delay products and speed performance

MESFETs are faster and more power efficient as compared to MOSFETs under fair ground comparison of oxide thickness and gate length stated below. The delay times of ring oscillators using 25nm CMOS (doping concentration = 2.0×10^{18} cm^{-3}, oxide thickness = 30Å and threshold voltage = 0.4V) and 75nm MESFET (doping concentration = 5.0×10^{18} cm^{-3}, Schottky barrier height = 0.9 and threshold voltage = 0.2V) are obtained as 6.37ps and 2.44ps respectively, whereas the device transit times and power-delay products are 0.36ps and 0.3ps respectively and 1.75fJ and 0.85fJ [69]. MESFET, with three times greater gate length than that of CMOS, showed 2.5 times less time delay time when compared to CMOS. The propagation delay and power dissipation per gate of CMOS is found roughly in the range of

1-10ns and 30microwatt-1mW respectively, whereas GaAs CMES shows less propagation delay and power dissipation per gate indicated in Fig. 1.1 [70].

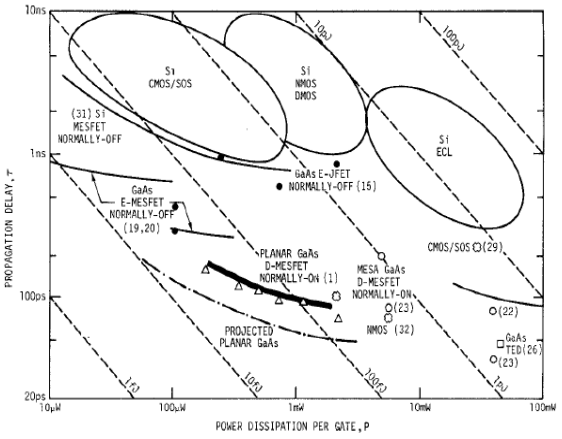


Fig. 1.1 Map of propagation delay versus power dissipation per gate comparing published results for GaAs and Si IC technologies [71-80]

Comparison of the steady-state velocity field characteristics for electrons in silicon MOS channel and GaAs MESFET channel showed that the steady-state electron velocities in GaAs are much higher than those in silicon MOSFET channels [81]. The mobility in the MESFET channel is approximately twice as large as that of peak MOSFET mobility, while in subthreshold regime (sheet density $<10^{11}cm^{-2}$) it is approximately five times larger [81]. Although n-channel GaAs DCFL circuits have demonstrated impressive speed results [82], a complementary p- and n-channel GaAs logic similar to CMOS seems to be preferable for higher integration levels because of low noise, much reduced power dissipation and high radiation tolerances. D-MESFET GaAs ICs have shown propagation delay as low at τ_d = 75ps for Lg = 1 micron, while E-MESFET circuits have shown speed-power products as low as 30fJ at τ_d = 300ps switching speed, where the standard value of dynamic switching energies or speed-power product ($P_D\tau_d$) should stay at less than 0.1pJ to 0.01pJ for practical high speed VLSI and ULSI circuits. Hence, the integration of GaAs based n-MESFET and p-MESFET has strong potentiality to be realized for VLSI and ULSI CMES [82]. The recent development of advanced VLSI GaAs processes allows the realization of gate arrays with 350k gate [83].

GaAs based CMES circuits utilizing both p- and n-channel transistors offer great advantages over CMOS circuits with respect to speed performance, radiation hardness, noise margin, power dissipation, and therefore circuit integration level for VLSI applications.

1.6 Propagation Delay

The digital logic gate using the configuration of buffered FET logic (BFL), Schottky diode FET logic (SDFL) and direct coupled FET logic (DCFL) was successfully developed using the discrete MESFET devices for high speed inverter, NOR and NAND gates described below. BFL is the fastest form of MESFET logic with gate propagation delays of around 50ps being reported for 0.5 μm gate length. These gates used a fairly large number of FETs and a substantial layout area per gate. NAND and NOR gates were built by implementations of BFL [84]. GaAs DCFL uses a depletion MESFET as the active load, and enhancement MESFET as driver to implement ultra fast logic functions in inverter and NOR gates. Propagation delays as short as 15ps were reported using self-aligned 0.6 micron GaAs MESFETs [85]. The propagation delay per gate versus supply voltage and power dissipation for a five stage ring oscillator using DCFL configuration are shown in Figure 1.2 and Figure 1.3 [86-88].

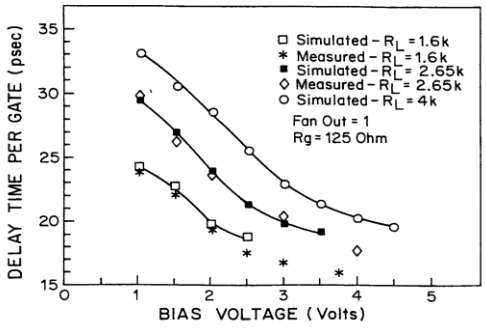


Fig. 1.2 Propagation delay/gate versus supply voltage

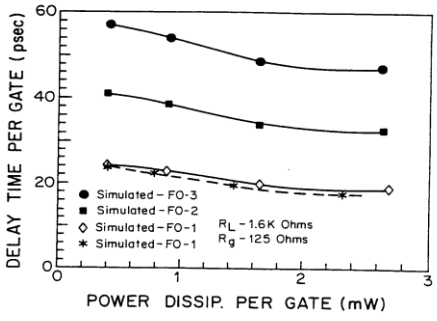


Fig. 1.3 Propagation delay/gate versus power dissipation

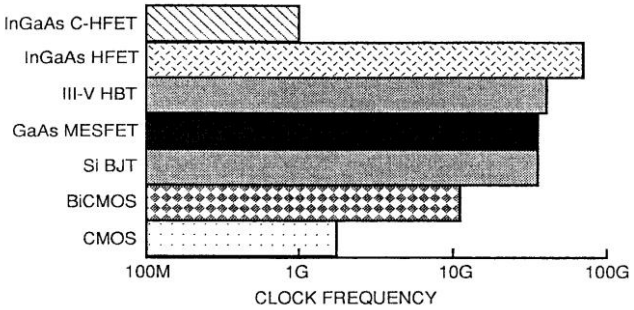


Fig.1.4 Summary of highest clock frequencies reported for several digital IC technologies.

Figure 1.4 shows maximum clock frequency operation depending on the material and device. The operating clock frequency range for GaAs MESFET is higher than BiCMOS and CMOS but lower than HBT and HFET transistors [89]. Complementary GaAs logic is currently being explored with HIGFET [90] and MODFET [91] technologies, but the heterostructure devices are complicated to fabricate and generally require cryogenic cooling to achieve high performance. Based on these reports, our hands-on experience of analytical device modeling and 2D-simulation Synopsys Sentaurus TCAD, and practical device fabrication, the proposed research anticipates a positive outcome for GaAs CMES with high radiation hardness, high speed switching, low propagation delay and low dissipation, and low noise performance.

1.7 Performance limitation of CMOS

Hot carrier effects

If a MOS transistor is operated under pinch-off condition, also known as “saturated case”, hot carriers traveling with saturation velocity can cause parasitic effects at the drain side of the channel known as ``Hot Carrier Effects" (HCE). These carriers have sufficient energy to generate electron-hole pairs by Impact Ionization (II).The generated bulk minority carriers can either be collected by the drain or injected into the gate oxide. The generated majority carriers create a bulk current which can be used as a measurable quantity to determine the level of impact ionization [92]. Carrier injection into the gate oxide can lead to hot carrier degradation effects such as threshold voltage changes due to occupied traps in the oxide. Hot carriers can

also generate traps at the silicon-oxide interface known as ``fast surface states'' leading to subthreshold swing deterioration and stress-induced drain leakage. In general, these degradation effects set a limit to the lifetime of a transistor, therefore they have to be controlled as well as possible. Bulk currents are comparatively unimportant as long as the parasitic series resistance of the bulk does not establish a drastically increased bulk potential which can lead to threshold voltage reduction or even more serious effects like snap-back or latch-up. The energy of the hot carriers depends mainly on the electric field in the pinch-off region. Since, in the past, the scaling of supply voltage has not been as aggressive as the device geometry scaling, the electric field has been permanently rising [93].

Punch through

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device. Punch through current is strongly dependent on Drain-Induced Barrier Lowering (DIBL). It adds to the subthreshold leakage current leading to an increased power consumption [94].

Velocity saturation

As devices are reduced in size, the electric field typically also increases and the carriers in the channel have an increased velocity. However at high fields there is no longer a linear relation between the electric field and the velocity as the velocity gradually saturates reaching the saturation velocity. This velocity saturation is caused by the increased scattering rate of highly energetic electrons, primarily due to optical phonon emission. This effect increases the transit

time of carriers through the channel. In sub-micron MOSFETs one finds that the average electron velocity is larger than in bulk material so that velocity saturation is not quite as much of a restriction as initially thought [94].

Drain induced barrier lowering (DIBL)

Drain induced barrier lowering (DIBL) is the effect the drain voltage on the output conductance and measured threshold voltage. This effect occurs in devices where only the gate length is reduced without properly scaling the other dimensions. It is observed as a variation of the measured threshold voltage with reduced gate length. The threshold variation is caused by the increased current with increased drain voltage as the applied drain voltage controls the inversion layer charge at the drain, thereby competing with the gate voltage. This effect is due to the two-dimensional field distribution at the drain end and can typically be eliminated by properly scaling the drain and source depths while increasing the substrate doping density [94].

Gate-Induced Drain Leakage (GIDL)

When the MOSFET is in off-state, a significant leakage current passing through the drain electrode can be detected at drain voltage much lower than the breakdown voltage. This drain leakage current is caused by the gate-induced high electric field in the gate-to-drain overlap region. Many researchers have attributed the leakage current to the band-to-band tunneling occurring in the overlap region and named the phenomenon gate-induced drain leakage current (GIDL). This leakage has actually been observed in DRAM trench transistor cells, and identified as the dominant leakage mechanism in discharging the storage node. The dependence of this leakage on the fabrication process and device parameters has been reported. The exact oxide thickness and doping profiles in the gate-to-drain overlap region are found to play important roles in the GIDL current. The GIDL and its degradation have restricted the scaling of oxide thickness and power supply voltage. In addition, the band-to-band tunneling

induced hot-electron injection is proposed to be a programming method for flash memory cells and an erase operation for EEPROM memory cells. For these reasons, it is very important to have a good understanding and an accurate physical model of band-to-band tunneling current [95].

1.8 Advantages and Disadvantages of MESFET in CMES

The GaAs MESFET is mostly based on ion implantation into the semi insulating substrates, which is least expensive concerning raw material cost, since no epitaxial layers are required. GaAs FET can easily achieve noise figures below 1dB in the 1-2 GHz frequency range [96]. The low thermal conductivity of GaAs inhibits an efficient cooling of active devices, which may cause a significant self-heating effect (SHE). SHE manifests itself as a reduced drain current, and even a negative differential conductance at high power inputs. The disadvantage of the conventional SOS MESFET lies in the large source-gate resistance arising from the low electron mobility of electrons in n-type SOS films. The large source-gate resistance reduces the mutual transconductance and hence the high frequency figure of merit. However, MESFETs fabricated on SOS film have the advantages of reduced parasitic source (drain) capacitances, perfect device isolation, and better radiation hardness. The MESFET device fabricated on thin SOI film interests us because it gains the benefit of SOI structure while bypassing the gate oxide related reliability issues of MOSFETs. SOI MESFET presents very small short gate length effect and is the most promising device for future ULSI technology. The subthreshold current is of great concern since it has consequences for the bias and logic levels in digital operation as well as for the holding time in dynamic circuits. The short gate length effect can be minimized using the technique proposed by TriQuint Semiconductor Inc. [97]. The CMES device can be produced in the lab, but also has great scalability potential beyond the lab using high precision equipment in semiconductor industries. The technology is well tested, increasing its likelihood for success.

Others, too, have demonstrated MESFET's potential, producing GaAs MESFETs with gate lengths ranging from 260nm to 30nm, which showed short channel effect on subthreshold current, DC transconductance and threshold voltage [98]. Successful fabrication of GaAs MESFETs with gate length of 30 nm showed DC transconductances of up to 710ms/mm and unity gain cut-off frequencies of up to 150 GHz with desirable I-V characteristics, where poor pinch-off and output conductance characteristics indicated significant carrier injection into the buffer layer [99]. Due to diminishing aspect ratio, GaAs MESFETs with gate lengths ranging from 25nm to 80nm showed transconductance degradation as a function of effective gate length [100]. Sub-threshold silicon MESFETs with 25nm gate length was fabricated and ultra high speed/low power and cut-off frequencies significantly higher than the ITRS roadmap predicted [101]. Indeed, the ITRS roadmap shows 9nm technology can be achieved. MESFETs are possible solutions beyond 9nm CMES with simple fabrication, better device performance, low power consumption and better device scalability for VLSI and ULSI integration.

1.9 History of Silicon

Attention was first drawn to quartz as the possible oxide of a fundamental chemical element by Antoine Lavoisier, in 1787. In 1811, Gay-Lussac and Thenard are thought to have prepared impure amorphous silicon, through the heating of recently isolated potassium metal with silicon tetrafluoride, but they did not purify and characterize the product, nor identify it as a new element. In 1824, Berzelius prepared amorphous silicon using approximately the same method as Gay-Lussac (potassium metal and potassium fluorosilicate), but purifying the product to a brown powder by repeatedly washing it. He named the product silicium from the Latin silex, silicis for flint, flints, and adding the "-ium" ending because he believed it was a metal. As a result he is usually given credit for element's discovery. Silicon was given its present name in 1831 by Scottish chemist Thomas Thomson. He retained part of Berzelius's name but added "-on" because he believed silicon a nonmetal more similar to boron and carbon.

Silicon in its more common crystalline form was not prepared until 31 years later, by Deville. By electrolyzing impure sodium-aluminum chloride containing approximately 10% silicon, he was able to obtain a slightly impure allotrope of silicon in 1854. Later, more cost-effective methods have been developed to isolate silicon in several allotrope forms. Because silicon is an important element in semiconductors and high-technology devices, many places in the world bear its name. For example, Silicon Valley in California, since it is the base for a number of technology related industries, bears the name silicon [102].

Physical Characteristics

Silicon is a solid at room temperature, with relatively high melting and boiling points of approximately 1,400 and 2,800 degrees Celsius respectively. Interestingly, silicon has a greater density in a liquid state than a solid state. Therefore, it does not contract when it freezes like most substances, but expands, similar to how ice is less dense than water and has less mass per unit of volume than liquid water. With a relatively high thermal conductivity of 149 $W \cdot m^{-1} \cdot K^{-1}$, silicon conducts heat well and as a result is not often used to insulate hot objects. In its crystalline form, pure silicon has a gray color and a metallic luster. Like germanium, silicon is rather strong, very brittle, and prone to chipping. Silicon, like carbon and germanium, crystallizes in a diamond cubic crystal structure, with a lattice spacing of approximately 0.5430710 nm (5.430710 Å).The outer electron orbital of silicon, like that of carbon, has four valence electrons. The 1s,2s,2p and 3s subshells are completely filled while the 3p subshell contains two electrons out of a possible six. Pure silicon has a negative temperature coefficient of resistance, since the number of free charge carriers increases with temperature. The electrical resistance of single crystal silicon significantly changes under the application of mechanical stress due to the piezoresistive effect [102].

Usage of Silicon in Electronics Devices

Since most elemental silicon produced remains as ferrosilicon alloy, only a relatively small amount (20%) of the elemental silicon produced is refined to metallurgical grade purity (a total of 1.3–1.5 million metric tons/year). The fraction of silicon metal which is further refined to semiconductor purity is estimated at only 15% of the world production of metallurgical grade silicon. However, the economic importance of this small very high-purity fraction (especially the ~ 5% which is processed to monocrystalline silicon for use in integrated circuits) is disproportionately large. Pure monocrystalline silicon is used to produce silicon wafers used in the semiconductor industry, in electronics and in some high-cost and high-efficiency photovoltaic applications. In terms of charge conduction, pure silicon is an intrinsic semiconductor which means that unlike metals it conducts electron holes and electrons which may be released from atoms within the crystal by heat, and thus increase silicon's electrical conductance with higher temperatures. Pure silicon has too low a conductance to be used as a circuit element in electronics without being doped with small concentrations of certain other elements. This process greatly increases its conductivity and adjusts its electrical response by controlling the number and charge (positive or negative) of activated carriers. Such control is necessary for transistors, solar cells, semiconductor detectors and other semiconductor devices, which are used in the computer industry and other technical applications. For example, in silicon photonics, silicon can be used as a continuous wave Raman laser medium to produce coherent light, though it is ineffective as an everyday light source [102].

In common integrated circuits, a wafer of monocrystalline silicon serves as a mechanical support for the circuits, which are created by doping, and insulated from each other by thin layers of silicon oxide, an insulator which is easily produced by exposing the element to oxygen under the proper conditions. Silicon has become the most popular material to build both high power semiconductors and integrated circuits, because of all the elements, silicon is

the semiconductor which can withstand the highest powers and temperatures without becoming dysfunctional due to avalanche breakdown, a process an electron avalanche is created by a chain reaction process where heat produces free electrons and holes, which in turn produce more current which produces more heat. In addition, the insulating oxide of silicon is not soluble in water, which gives it an advantage over germanium (an element with similar properties which can also be used in semiconductor devices) in certain type of fabrication techniques [102].

Monocrystalline silicon is expensive to produce, and is usually only justified in production of integrated circuits, where tiny crystal imperfections can interfere with tiny circuit paths. For other uses, other types of pure silicon which do not exist as single crystals may be employed. These include hydrogenated amorphous silicon and upgraded metallurgical-grade silicon (UMG-Si) which are used in the production of low-cost, large-area electronics in applications such as Liquid crystal displays, and of large-area, low-cost, thin-film solar cells. Such semiconductor grades of silicon which are either slightly less pure than those used in integrated circuits, or which are produced in polycrystalline rather than monocrystalline form, make up roughly similar amount of silicon as are produced for the monocrystalline silicon semiconductor industry, or 75,000 to 150,000 metric tons per year. However, production of such materials is growing more quickly than silicon for the integrated circuit market. By 2013 polycrystalline silicon production, used mostly in solar cells, is projected to reach 200,000 metric tons per year, while monocrystalline semiconductor silicon production (used in computer microchips) remains below 50,000 tons/year. [102]

In this graduate thesis, an attempt has been made to substitute the CMOS by CMES device. The CMES device structure, process evaluation and device electrical parameter have been presented in the next chapter. The schematic diagram of CMOS device shows in the figure 1.5, where the process technology for CMES is extremely simpler compared to CMOS and the yield becomes high due to the absence of gate-oxide integrity question.

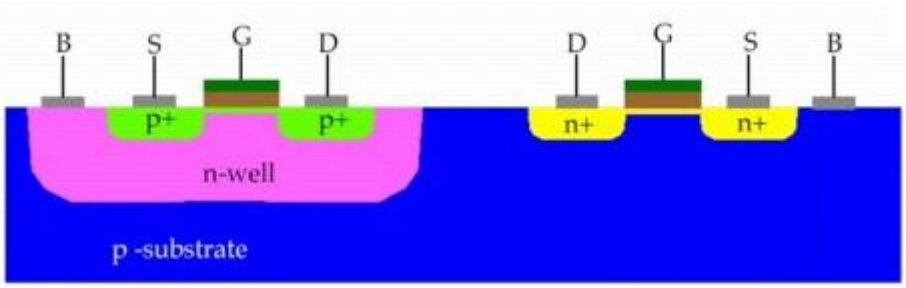


Figure 1.5 CMOS structure

CHAPTER 2

Complementary MESFET

2.1 Introduction

A semiconductor device referred to as complementary metal semiconductor (CMES) has p-type and n-type silicon MESFETs interconnected on a substrate with an n-type barrier enhancement implanted into the p-channel of the p-type MESFET. The structure and method of fabrication are provided for forming a CMES logic inverter which has characteristics of very low power, low voltage, low noise and high speed [103].

A method is provided for a barrier enhanced semiconductor structure comprising the steps of forming a twin well MESFET structure on a silicon wafer having a p-channel FET in an n-well and an n-channel FET in a p-well, forming a window in a photoresist layer disposed over the surface of the twin well MESFET structure to expose the p-channel in the n-well, implanting an n-type barrier enhancement layer into the p-channel, removing the photoresist layer, disposing a layer of silicon dioxide over the surface of the wafer, forming a mask over the silicon dioxide layer having a plurality of windows, bringing an etchant into contact with portions of the silicon dioxide exposed by the windows formed in the mask to selectively remove the portions of the silicon dioxide layer exposed by such windows to expose contact areas to a source, drain and channel of the p-channel and the n-channel MESFETS, disposing a layer of platinum over the surface of the wafer, heating the silicon wafer such that a thin region of platinum silicide forms on the silicon areas exposed to the platinum, chemically removing residual platinum from the silicon dioxide layer, depositing a layer of metal over the wafer, and patterning the deposited layer of metal for providing circuit contact connections [103].

The dominant device used in modern VLSI circuits today is the MOS transistor. As technology has advanced several limitations of MOSFETs have become apparent: hot electron effects with their associated threshold voltage shifts, short channel effects, and also the practical

technological problems of shrinking junctions and growing high integrity, low defect, thin gate oxides. MESFETs do not require thin gate oxides and hence are not susceptible to the problems of obtaining reliable thin gate oxides or to threshold voltage shifts due to hot carriers. Also, MESFETs are best suited to low voltage operation which is a common feature of most advanced VLSI technologies. In addition, MESFET devices have been shown to be quite radiation hard compared to other technologies. Finally, the MESFET can achieve bulk carrier mobility whereas MOSFETs are often restricted to less than half this value due to their surface conduction. The limited use of MESFETs for VLSI in the past has been due in part to their power requirements and limited variety of circuit configurations. The development of a complementary MESFET process not only reduces their power requirement and increases circuit flexibility, but also results in an improved speed performance thus improving their viability for VLSI applications [103].

2.2 MESFET Operation and Previous Work

To date, virtually all MESFET's built in both Si and GaAs have been n-channel devices. The reasons for this are twofold: 1) n-type material has a higher carrier mobility, and 2) higher Schottky-barrier heights (for the gate contacts) can be formed. Complementary MESFET's are attractive due to the increase in speed, decrease in power dissipation, and increase in circuit flexibility as displayed by CMOS [104].

Circuit speed is one of the most important performance parameters in the operation of an integrated circuit. Speed is predominantly determined by the intrinsic device speed and its current drive capability. To maximize these, the intrinsic transconductance of the device must be maximized and the parasitic resistance of the device and circuit minimized. The first truly self-aligned MESFET was fabricated by using SiO_2 sidewall spacers alongside the Schottky-gate contact. This enabled the source/drain regions to be implanted in the same self-aligned fashion as MOSFET's, simplifying fabrication and providing excellent control of

the source/drain offset distance. However, since the gate structure of the MESFET makes intimate contact with the silicon surface, thermal cycling after gate formation (and thus source/drain implant) must be minimized to prevent excessive gate material/silicon reactions. This may not allow full activation of the source/drain implant. Thus though a large reduction in the channel extension resistance is accomplished with this process, it is partially offset by an increase in the resistance of the source/drain contacts and diffusions. A transconductance value of about 8 mS/mm is estimated for a 2-pm device [104].

Due to the difficulty of growing or depositing a high quality insulating layer on GaAs, this technology has basically relied upon the use of MESFET's. To date, the only LSI fabrication effort made in GaAs has been with MESFET's. One of the major problems GaAs MESFET circuit designers face is that of backgating. This effect causes a modulation of the depletion layer width at the n channel to substrate which results in larger threshold-voltage variances. Other material and processing problems in GaAs also impact the device electrical characteristics. Variations in threshold voltage of MESFET's have been observed due to variations in gate orientation (piezoelectric effect). High source/drain contact resistances result from poor alloyed ohmic contacts which impose limitations on the temperature of successive processing steps. These problems have been largely overcome today, with the result that a commercial GaAs MESFET industry has developed [104].

2.3 Present CMESFET Efforts

Results from three other complementary MESFET efforts have been reported; in Japan at the Toshiba corporation, at the Honeywell Physical Science Center, and at the University of Uppsala, Sweden. The first two efforts involve the development of GaAs complementary MESFET's. The group at Toshiba has fabricated p-channel GaAs MESFET's by using a WN**,** gate with rapid thermal annealing to achieve barrier heights to p-type GaAs of 0.68eV. SPICE

circuit simulations of 1.2-pm p- and n-channel GaAs MESFET inverters show potential switching speeds of 164ps with a power dissipation of 54pW**.** The adverse effect of heating the WN**,** Schottky contact to p-type GaAs is expected to be a limitation. This low-temperature, short time limitation does not allow for adequate source/drain implant activation. The lack of activation results in large parasitic resistances which limits the maximum transconductance for the 2-pm p-channel device to only 4.2 mS/mm. The group at the Honeywell Physical Science Center have reported impressive device drives for p-channel GaAs MESFET's using self-aligned source/drain implants. They have further improved the performance of these devices by employing a gate barrier enhancing technique as in. Due to the large disparity in mobilities between the two carriers in GaAs, the *W/L* ratio for the p-channel device needs to be increased by a factor of five to ten. This results in larger device capacitances than those for n-channel devices and therefore reduced switching speed. The com plementary design is primarily useful in GaAs when power consumption must be reduced. In silicon, effective electron and hole mobilities are more evenly matched which makes silicon complementary circuits more attractive for high-speed operation [104].

2.4 Device Structure

The structure of the p-channel MESFET and the n-channel device is completely similar, except, of course, that the doping polarities are reversed. The SiO_2, sidewall spacers reduce parasitics by allowing self-aligned source/drain implants in addition to allowing the source/drain regions themselves to be silicided. The gate region of the devices is composed of cosputtered $TiSi_2$. Shannon implants for both the p- and n-channel devices are employed to increase the effective barrier height of the Schottky-gate contacts. This configuration for the gates of the devices provides thermally stable, high barrier heights in a manner which is easy to implement into the overall complementary MESFET process.

Note the presence of the oxide cap over the gate. This structure prevents the source/drain implant from doping the TiSi, gate of the devices. Since the gate material makes intimate contact with the silicon surface, dopant within the gate may out diffuse into the channel during subsequent anneals. This out-diffusion would not only reduce the effective barrier height of the Schottky contact, but would alter the threshold voltage of the device [104].

The oxide cap structure eases the formation of the self-aligned silicidation as well. The source/drain silicidation technique has been applied to MOSFET's, however, it has not been applied to MESFET's. One of the major failure modes for the self-aligned silicidation technique in MOSFET's is shorting of the gate to the self-aligned source/drain contact. The presence of the nonreactive cap restricts the formation of the silicide to the source/drain regions, thus preventing possible shorts to the underlying electrical gate [104].

2.5 Process Flow

Due to the MOS-like structure developed in this work for MESFET's, and the utilization of a single-gate material for both polarity devices, the developed complementary MESFET process is very similar to a CMOS fabrication process. This development allowed the use of a CMOS mask set, with a slight modification in mask order for the fabrication of the complementary MESFET's. An extensive collection of CMOS test chips has been developed at Stanford for purposes of process evaluation. The test vehicles developed in the CMOS work served as excellent vehicles for the complementary MESFET process as well [104].

2.6 Theories for the MESFET device

The Metal Semiconductor Field Effect Transistor(MESFET) is a well know device for it negative temperature characteristic, temperature stable ability, and the good parallel connected ability in the integrated circuit application. Usually, MESFET made by GaAs or InP because of the high mobility, high switching speed and high cut off frequency properties elements. The

main structure of the MESFET device is show in Figure 2.1.

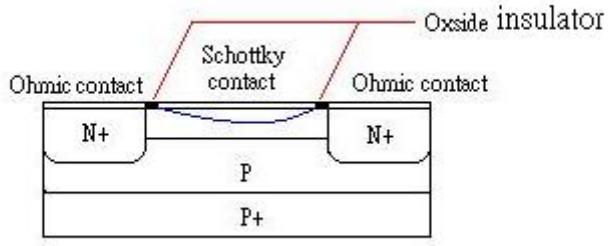


Figure 2.1

The main structure of MESFET consists of one Schottky contact at the gate terminal and Ohmic contacts at drain and source terminal. Also, MEFSET can work with majority carrier in the channel region because of fast response of Schottky contact as gate structure and pre-channeled. For source and drain electrode node, it is forming by the ohmic contact structure because of it low resistance property. However, the key technique of MESFET device might be the schottky gate structure. The Schottky contact is discussed below.

2.7 Metal Semiconductor contact

The basic Schottky contact was formed by growing metal on the low impurity doping semiconductor surface, basically like one side abrupt junction. This kind of contact has rectified ability. The energy band diagram of non-contact is shown in Figure 2.2a.

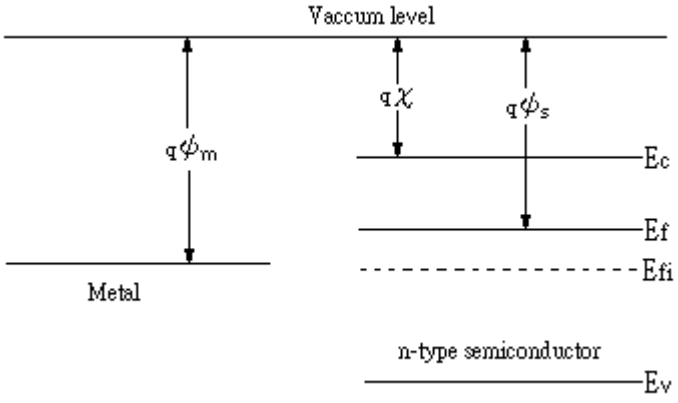


Figure 2.2a Energy band diagram under non-contact situation

Where

ψ_m = work function of metal,

ψ_s = work function of semiconductor.

χ = electron affinity of semiconductor.

After contact of metal and semiconductor, the Schottky contact formed and the energy band diagram shows in Figure 2.2b.

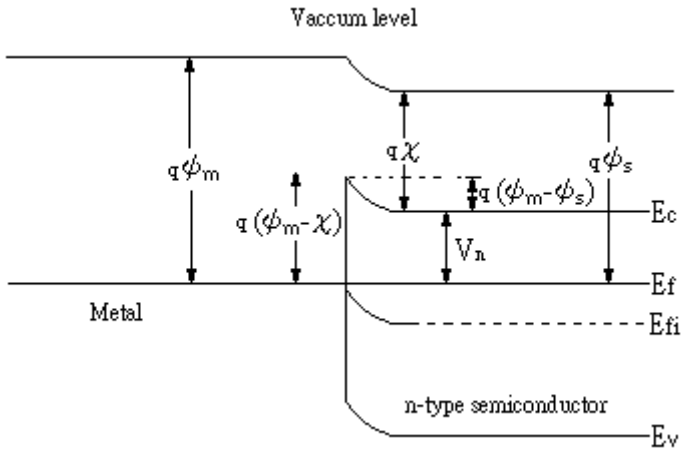


Figure 2.2b Energy band diagram under zero biasing situation.

Here, Schottky barrier of the n-type semiconductor ψ_{BN},

$$\psi_{BN} = q(\psi_m - \psi_s) \quad (1)$$

And define V_{bi} as build-in potential,

$$V_{bi} = q(\psi_m - \psi_s) = \psi_{BN} - Vn \quad (2)$$

Where

Vn = Depth of Fermi level below conduction band.

From this energy band diagram, It shows that Schottky barrier heights is portion to the metal work function.

2.8 Depletion region width

According to the Poisson's equation, the electric field can be shown in equation 4:

$$\rho = qND \tag{3}$$

$$\frac{d^2v}{dX^2} = \frac{\rho}{\epsilon_s} \tag{4}$$

$$\frac{dE}{dX} = \frac{\rho}{\epsilon_s} \tag{5}$$

$$dE = \frac{\rho}{\epsilon_s}\, dx \tag{6}$$

$$\text{->} \quad \int_{E(x)}^{E(x_n)} dE = \int_{E(x)}^{E(x_n)} \frac{\rho}{\epsilon_s}\, dx \tag{7}$$

$$E(X_n) - E(X) = \frac{\rho}{\epsilon_s}(x_n - x\ ) \tag{8}$$

Boundary condition for electric field at edge of the depletion region should be zero so

$E(X_n) = 0.$

When x = 0 (at surface of the semiconductor), the maximum electric field will occur and express equation 9

$$E(0) = E(max) = -\ \frac{\rho}{\epsilon_s} x_n \tag{9}$$

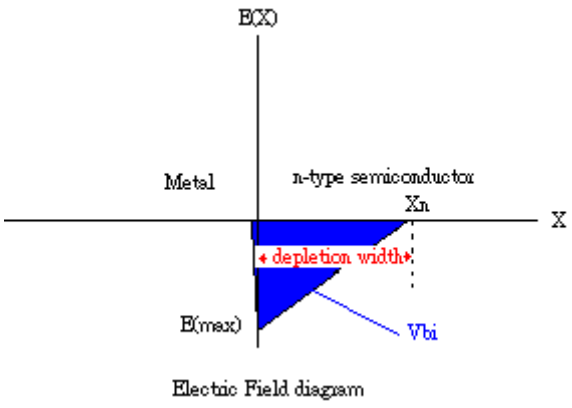
Where$\rho = qN_A$

Recalling formula

$$-E(X) = \frac{\rho}{\epsilon_s}(x_n - x) \tag{10}$$

Incorporate with E(max) into this equation and obtained on equation 11

$$E(X) = -\frac{\rho}{\epsilon_s} x_n + \frac{\rho}{\epsilon_s} X \text{ -> } E(X) = -E(max) + \frac{\rho}{\epsilon_s} X \tag{11}$$



Electric Field diagram

Figure 2.3

According to the Electric Field diagram shows in Figure 2.3, it can be determined the potential across the semiconductor can be expressed in equation 12 by obtaining the area of the Electric field. So, potential Vbi :

$$Vbi = \frac{1}{2} E(max)x_n \quad (12)$$

Then E(max) is brought into this equation and than the equation become:

$$Vbi = \frac{\rho}{\epsilon_s} x_n \frac{X_n}{2} \quad (13)$$

$$Vbi \frac{2\epsilon_s}{\rho} = X_n{}^2 \quad (14)$$

So we get the depletion width formula as show below:

$$X_n = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(Vbi)} \quad (15)$$

In X_n formula, we use $(Vbi - V)$ instead Vbi term, V means external applied voltage on the Metal terminal.

For Schottky contact case at the interface of schottky junction, the majority part of depletion region is occurred at low doped n-type semiconductor substrate, so the depletion region in the metal can be ignored. So the approximation of the total space width can be expressed in equation 16:

$$X_n \cong W = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(Vbi - V)} \quad (16)$$

2.9 Junction Capacitance

In order to determine the junction capacitance of the Schottky contact, let find out the total charge in the depletion region :

$$Q = qN_D W \quad (17)$$

Where, $W = \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(Vbi - V)}$ substitute equation 17 and obtained:

$$Q = qN_D\sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(Vbi - V)} \quad (18a)$$

$$= \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(Vbi - V)q^2{N_D}^2} \quad (18b)$$

$$= \sqrt{2\epsilon_s qN_D(Vbi - V)} \quad (18c)$$

According to the basic definition the Capacitance, the capacitance can be expressed in equation (19).

$$C = \frac{Q}{V} \quad (19)$$

$$C = \frac{dQ}{dV} = \frac{d\sqrt{2\epsilon_s qN_D Vbi - 2\epsilon_s qN_D V}}{dV} \quad (20)$$

$$= \frac{1}{2}(2\epsilon_s qN_D Vbi - 2\epsilon_s qN_D V)^{-\frac{1}{2}}(-2\epsilon_s qN_D) \quad (21a)$$

$$= \frac{\epsilon_s}{\sqrt{\frac{2\epsilon_s}{qN_D}(Vbi - V)}} \quad (21b)$$

So the junction capacitance can be expressed in equation 22

$$C = \frac{\epsilon_s}{W} \quad (22)$$

For the Schottky contact, the doping concentration of semiconductor usually smaller than DOS(Density of states) in the conduction band.

2.10 Ohmic contact

Ohmic contact plays an important role in MESFET device to form source and drain electrode. It is basically consist of metal which provided a negligible contact resistance. When metal contact on highly doped semiconductor, the tunneling current can be estimated in equation 23

$$I \cong \exp\left[-2w\sqrt{\frac{2m_n(q\Phi_B - qV)}{h^2}}\right] \quad (23)$$

Where $w \cong \sqrt{\frac{2\epsilon_s}{q}\frac{1}{N_D}(\Phi_B - V)}$

And we have:

$$I \cong \exp\left[-2\sqrt{\frac{2m_n(\Phi_B - V)q}{h^2}\frac{2\epsilon_s}{q}\frac{1}{N_D}(\Phi_{BN} - V)}\right] \quad (24a)$$

$$= \exp\left[-4\sqrt{\frac{\epsilon_s}{N_D}\frac{m_n(\Phi_B - V)^2}{h^2}}\right] \quad (24b)$$

$$= \exp\left[-4\frac{m_n(\Phi_B - V)}{h}\sqrt{\frac{\epsilon_s}{N_D}}\right] \quad (24c)$$

According ohmic laws, $R = \frac{dI}{dV}^{-1}$, Channel resistance R_c can be expressed in equation 23a or equation 25b.

$$R_c = \frac{dI}{dV}^{-1} = \left[\exp[-\frac{4\sqrt{\epsilon_s m_n}}{h\sqrt{N_D}}(\Phi_B - V)]4\frac{\sqrt{\varepsilon\epsilon_s m_n}}{h\sqrt{N_D}}\right]^{-1} \quad (25a)$$

$$R_c = \frac{h\sqrt{N_D}}{4\sqrt{\epsilon_s m_n}}\exp[\frac{4\sqrt{\epsilon_s m_n}}{h\sqrt{N_D}}(\Phi_B - V)] \quad (25b)$$

From this formula, it is well understood that R_c is affected by the doping concentration N_D, when N_D increase, R_c decrease.

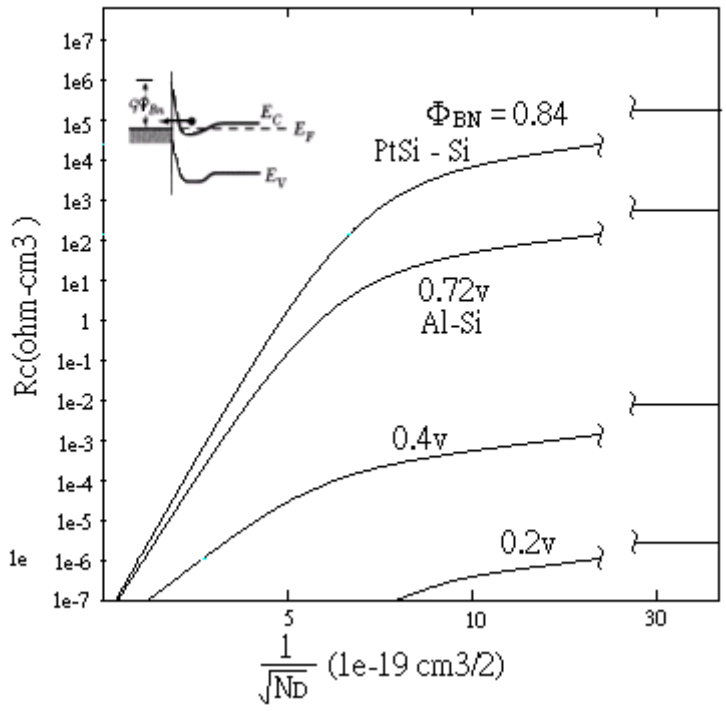


Figure 2.4 Impurity concentration versus R_c

Figure 2.4 is roughly present that the relationship between impurity N_D and resistance R_c. As a brief summary for Schottky and Ohmic contact is that the key part of difference between Schottky contact and Ohmic contact is doping concentration. High doping concentration is associated with Ohmic contact, and the low doping concentration is related to form the Schottky contact and the concentration is usually smaller than the DOS in the conduction band of the substrate material.

2.11 Metal-Semiconductor Field Effect Transistor(MESFET)

There are three key features for MESFET device, first of all, MESFET device is usually made by III-V compound because of it high electron mobility, high electron mobility would helps for minimized the serious resistance. Beside, high saturation velocity helps increase the cutoff frequency. In addition, MESFET usually fabricated on the epitaxial layer for minimize the parasite capacitance. Typically, it gate length made from 0.1-1.0 μm, and the thickness of the

channel is typically one-third or one-fifth of the gate length. The three dimensional structure is showed in Figure 2.5a, Figure 2.5b.

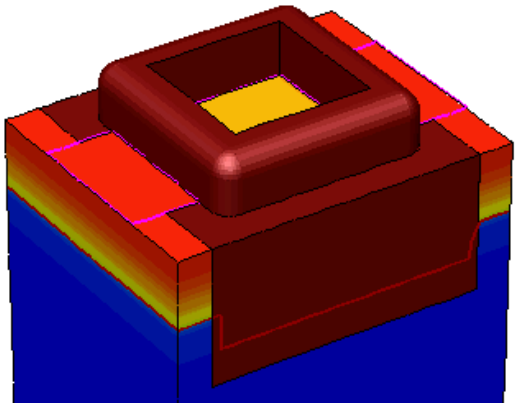


Figure 2.5a 3D structure meshing by SDE and show in Tecplot360

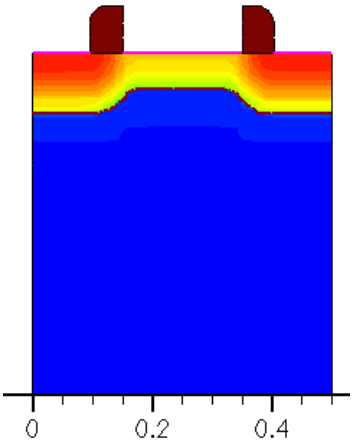


Figure 2.5b The cross section view of the MESFET by tecplot360

2.12 Operation of the MESFET device

Like the majority transistors, MESFET has the similar working area under different biasing situation, such as active region, saturation region and the break down region. For this structure, device is normally on because of the channel has already existed and the space charge region did not occupy the whole channel yet. The basic idea to control the channel on or shut down is depending on the gate voltage and the drain voltage, the current handling ability associated with the gate width “z” parameter, the wider gate width might increase the maxim limitation of

current. The space charge illustration is shown in Figure 2.6.

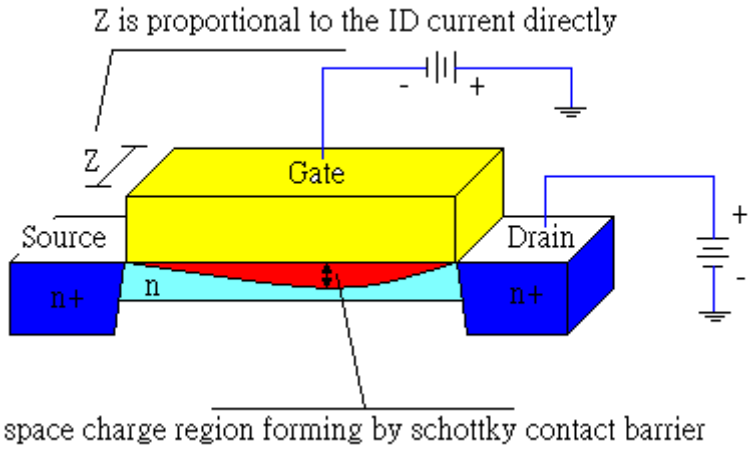


Figure 2.6 Space charge illustration.

2.13 Working in the non-saturation region

For this study, the n-channel MESFET with epitaxial layer of 0.1μm has been used, at this structure, Schottky barrier is not thick enough to shut down the channel. To discussed the linear region physic. First of all, let Vs and Vg equal to zero, add a positive voltage on the drain terminal, the passing charges that from the source terminal through the channel to the drain terminal are increasing, and that means the current is increasing with almost no interruption of depletion from gate terminal. But at the same time, the depletion region of drain side increase gradually because of that some of electrons are inducted and released from the channel to drain area show in Figure 2.7. In non-saturation region, drain current is linearly proportional the drain voltage is shown in Figure 2.8.

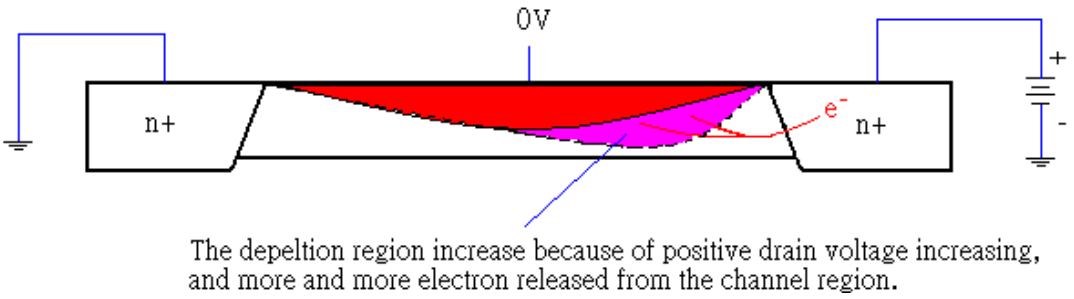


Figure 2.7

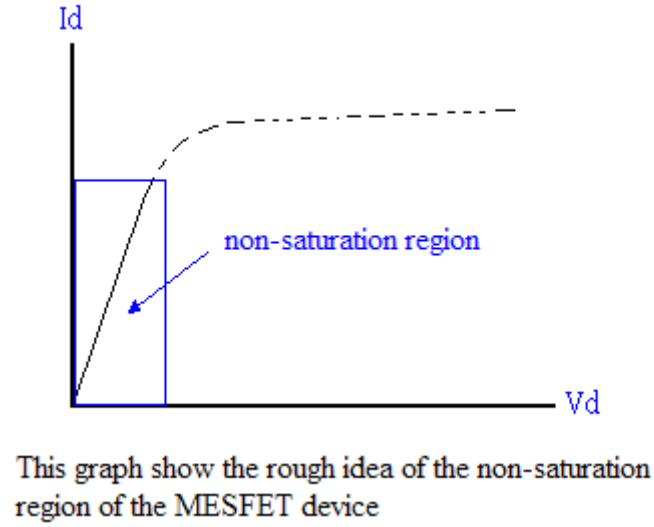


Figure 2.8

2.14 The Pinch off area

Lets us continue from previous biasing situation, Vg still keep zero, Vd increase more, at the same time, the depletion region area increases and approaches the bottom of the channel edge. Right on this voltage of Vd, the whole channel would be pinch-off by the depletion layer shown in Figure 2.9. When pinch-off occurs, the passing charge in the channel would seriously curb by the pinch-off effect. However, charges still own the very high energy because of high electric field applied on the drain side.[104]

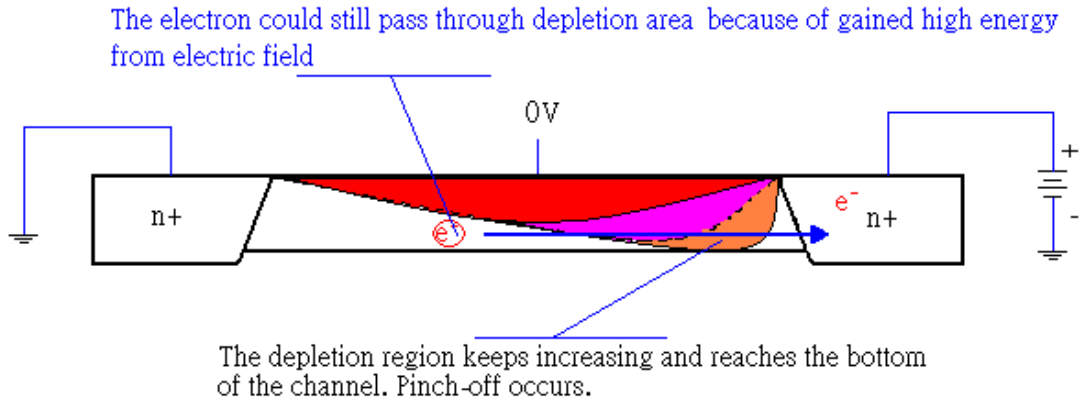


Figure 2.9

As a result, the high energy charge could still pass through the depletion region and form the

drain current. Under pinch-off situation, drain current would not increase anymore and keep like constant current ideally(as know as saturation current), but in the real case, the behavior of saturation current is very similar to MOSFET device. The saturation current would increase gradually in the pinch-off area. Here, which pinch off voltage can be defined as saturation drain voltage "V_{DSAT}". According to the electric field diagram as shown in Figure 2.10, V_{DSAT} can be visible at blue region in Figure 2.10.

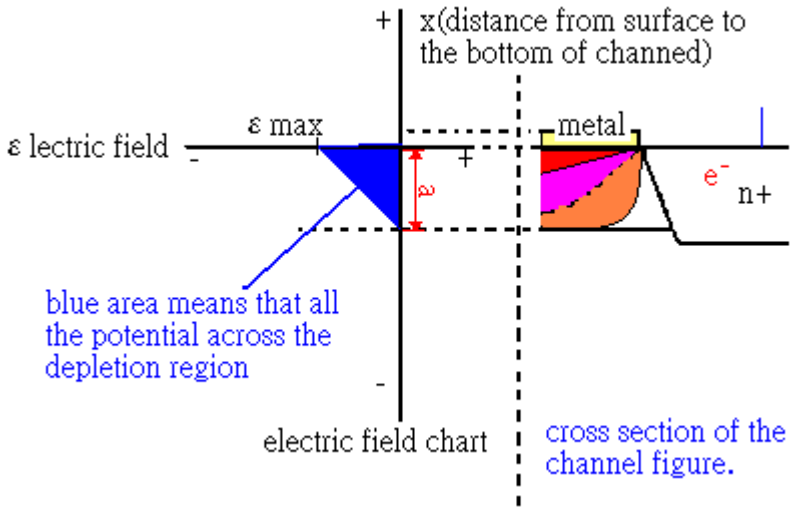


Figure 2.10

Because under pinch off situation, the depletion region must be the maxim (orange region as shown in Figure 10)value and so do the potential of depletion region, so at this point, the total potential drop on this depletion region include build-in potential and added potential of the drain terminal(Red + purple + orange region as shown in Figure 2.10).

$$V_{drop} = \frac{\varepsilon_{max}\, a}{2} \tag{26}$$

where

$$\varepsilon_{max} = \frac{qN_D}{\epsilon_s} x_n = \frac{qN_D}{\epsilon_s} a, \tag{27}$$

a =achive channel depth and the channel depth can be defined:

$$W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)(V_{bi} + V)}$$

ε_{max} = maxim electric field

Substute ε_{max} (maxim electric field) into the V_{drop} formula (equation 26) than one can obtain:

$$\frac{qN_Da^2}{2\epsilon_s} = V_{drop} = (V_{bi} + V) \quad (28)$$

At this point of operation (Vg = 0), we could see V as saturation voltage (shown in Figure 2.11) that applied on drain terminal and it can be derived:

$$V_{DSAT} = \frac{qN_Da^2}{2\epsilon_s} - V_{bi} \quad (29)$$

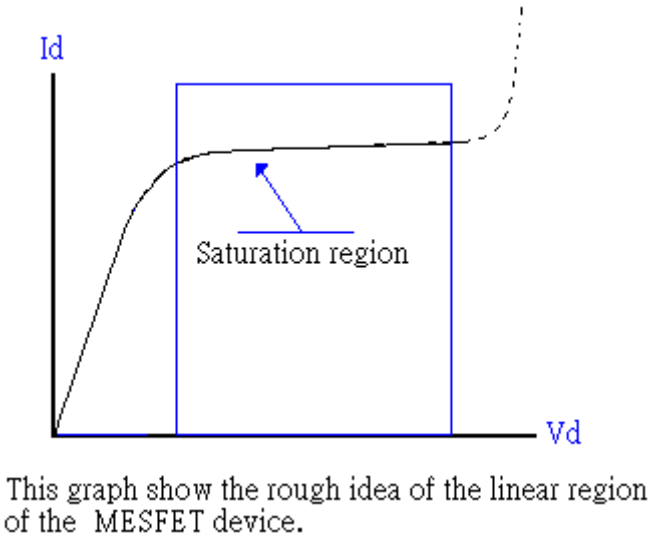


Figure 2.11

After V_{Dsat} voltage point, the potential drop in the channel keeps the same. But when the drain applied voltage keep increasing, the depletion region will move toward to the source side and it will take whole channel shown in Figure 2.12.

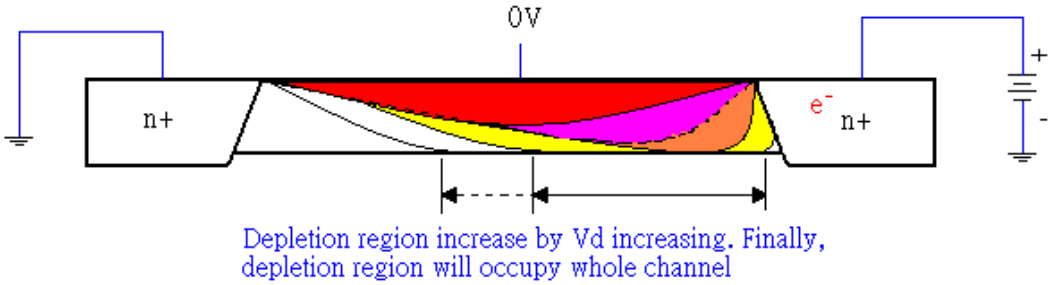


Figure 2.12

2.15 Current – Voltage characteristic

The basic idea of the drain current determination is to calculate the total resistance of channel and use Ohm's law, dV= Id dR, to determine the current. For this purpose, lets us start with a little cubic in the channel region and with uniform model as shown in Figure 2.13.

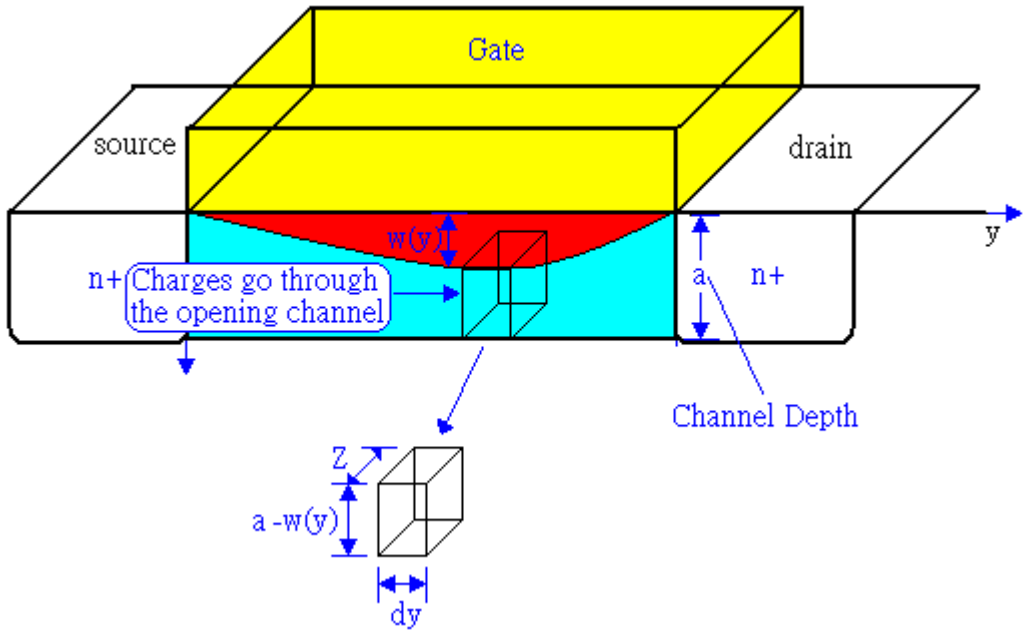


Figure 2.13

Let us define the parameter first, in the opening channel region, z as a channel width, w(y) as a depletion depth function vary with y axis, v(y) as a voltage that vary with y axis, "a" as physical channel depth. Parameter "dy" as a very short distance in the open channel (non-depleted region). Let us find out the resistance of the cubic first:

$$dR = \rho \frac{L}{A} = \rho \frac{dy}{Z(a-w(y))} \quad (30)$$

where ρ is resistivity

A = cross sectional area

L = Z

After derive the resistance of this cubic, lets find out potential drop on this cubic dV.

Basically, vary of w(y) associate with three factors.

1. The Schottky barrier Vbi.
2. Gate applied potential.
3. Drain applied potential.

Here, gate potential set as a constant. The changes of w(y) depend on the change of drain applied voltage directly.

$$W(y) = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)\left(V_{bi} + V_G + V(y)\right)} \tag{31}$$

If $V(y) = V_D$, than $W(y)$ will be W_D

$$W_D = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)(V_{bi} + V_G + V_D)} \tag{32}$$

The variation of W_D associated with V_D can be derived by differentiation.

$$\frac{dW_D}{dV_D} = \left(\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)(V_{bi} + V_G + V_D)\right)^{-\frac{1}{2}}\frac{1}{2}\left(\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)\right) \tag{33}$$

Equation 34 can be expressed in equation 34

$$\frac{1}{dV_D} = \left(\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)(V_{bi} + V_G + V_D)\right)^{-\frac{1}{2}}\frac{1}{2}\left(\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)\right)\frac{1}{dW_D} \tag{34}$$

Where

$W_D = \left(\frac{2\epsilon_s}{q}\left(\frac{1}{N_D}\right)(V_{bi} + V_G + V_D)\right)^{-\frac{1}{2}}$, So W_D can substitute into equation 35.

$$dV_D = W_D\frac{q}{\epsilon_s}N_D dW_D \tag{35}$$

Again, substitute equation 35 into equation dV= Id dR, one can obtain:

$$W_D \frac{q}{\epsilon_s} N_D dW_D = Id\ \rho\ \frac{dy}{Z(a-w(y))} \tag{36}$$

Where, the resistivity as know as $\frac{1}{qN_D\mu_n}$

$$W_D \frac{q}{\epsilon_s} N_D dW_D = Id\ \frac{1}{qN_D\mu_n}\ \frac{dy}{Z(a-w(y))} \tag{37}$$

Organize equation 37, w(y) at Drain point = W_D

$$Id\ dy = W_D \frac{q}{\epsilon_s} N_D\ qN_D\mu_n\ Z(a - W_D)dW_D \tag{38}$$

To integrate equation 39 for channel length through 0 to L (Channel length) with boundary condition, drain current can be evaluated on line Baovin of abrupt junction. For depletion region, the boundary condition is defined (it can be shown in Figure 2.14) from source to drain side. W_1 is the channel depth on source side, W_2 is the channel depth on drain side.

Figure 2.14

$$\int_0^L Id\ dy = \int_{W_1}^{W_2} \frac{q^2 {N_D}^2 \mu_n}{\epsilon_s} Z W_D(a - W_D)dW_D \tag{39}$$

$$Id(L - 0) = \frac{q^2 {N_D}^2 \mu_n}{\epsilon_s} Z \int_{w_1}^{w_2} W_D a - {W_D}^2\, dW_D \tag{40}$$

$$Id = \frac{q^2 {N_D}^2 \mu_n}{\epsilon_s} \frac{Z}{L}\left(\frac{1}{2}a\left({W_2}^2 - {W_1}^2\right) - \frac{1}{3}\left({W_2}^3 - {W_1}^3\right)\right) \tag{41}$$

Finally, the drain current formula can be expressed in equation 41.

CHAPTER 3

CMES Ion-implantation analysis

The structure of NMESFET and PMESFET is similar except that the doping polarities are reversed. Ion-implant method would be used to form channel between drain and source region. Concept remains same for both n and p-type MESFET. In order to determine characteristic of MESFET device, one has to consider non-uniform donor distribution in channel region. For fulfill this purpose, Gaussian distribution will be used for IDs current analysis. As a result, all of the parameters include threshold voltage, pinch off voltage, source-drain current will be changed. Let us start the non-uniform doping analysis [105].

There are several steps for device analysis. First, determine channel electric field and potential equations. Second, determine the relationship between channel and bulk and find out the approximation equation. Third, determine the threshold voltage and Pinch off voltage. Fourth, determine the characteristic of drain current to drain voltage.

First of all, consider a non-uniform doping profile MESFET device. It is consist of two high donor regions for source and drain, a low N doped for channel and a P type substrate. The structure can be shown in Figure 3.1

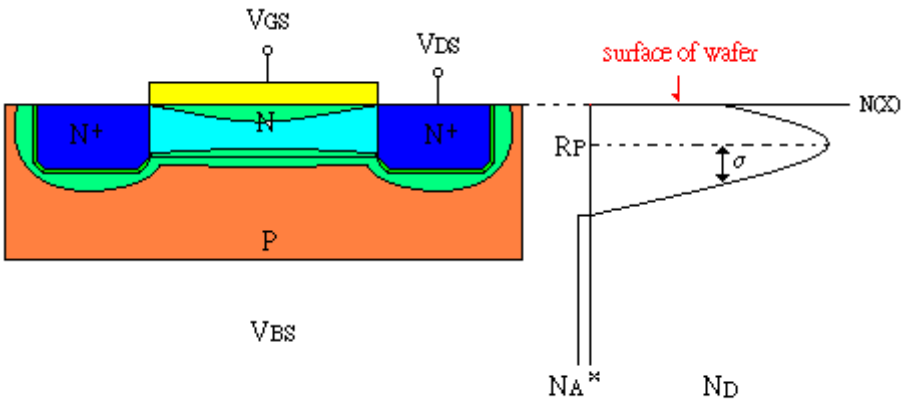


Figure 3.1 A MESFET structure and corresponding channel doping profile.

The channel concentration can be described in equation (42)

$$N(x) = \frac{Q}{\sqrt{2}\sigma} \exp\left[-\frac{(X-R_p)}{\sqrt{2}\sigma}\right]^2 - Na \quad (42)$$

The energy band diagram from gate to substrate can be shown in Figure 3.2.

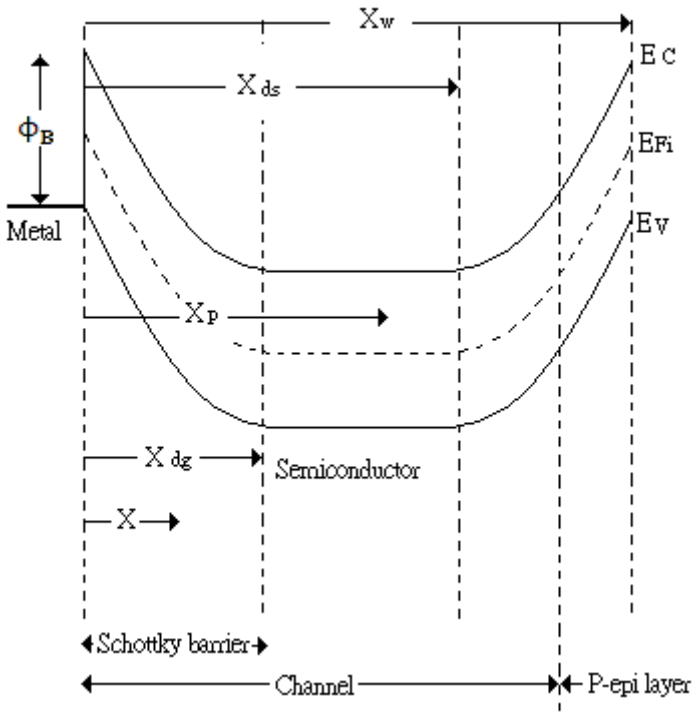


Figure 3.2 Energy band diagram under channel

In order to find the electric field and potential, one dimensional POISSON's equation is expressed below.

$$\frac{d^2V}{dx^2} = \frac{dE}{dx} = -\frac{\rho}{\epsilon} = \frac{qN(x)}{\epsilon} \quad (43)$$

3.1 Channel electric field and electron potential

Consider the surface to channel potential first. the electric field should equal to zero at the depletion edge, so the surface electric field at edge Xdg $E(X_{dg})$ should be zero. And the surface potential $\phi(0)$ should equal to gate voltage minus Schottky barrier. So the boundary conditions can be shown in equation (44), (45) and (46):

$$\phi(0) = V_G - \phi_B \quad (44)$$

$$E(X_{dg}) = 0 \tag{45}$$

$$\phi(X_{dg}) = V(y) - \Delta \tag{46}$$

where $\emptyset_B$ is the metal-semiconductor work function difference,

$\emptyset(0)$ is the surface potential,

Δ is the depth of the Fermi level below the conduction band in the undepleted channel region,

X_{dg} is the position of the depletion region edge in the channel.

The illustration of target electric field can be show in Figure 3.3

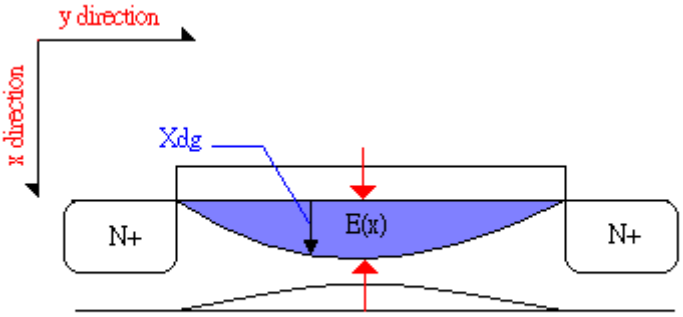


Figure 3.3 Electric field shows in purple region.

Bring Na into Poisson's equation and do integrate then the electric field can be shown in equation(47)

$$\int_{E(x_{dg})}^{E(x)} -dE = \int_{x_{dg}}^{x} \frac{eQ}{\varepsilon\sqrt{2\pi}\sigma} \exp\left(-\frac{(X-R_p)^2}{2\pi\sigma^2}\right) - \frac{e}{\varepsilon} N_A \, dx \tag{47}$$

Solving the integration on both sides of equation - 47

$$-\left(E(x) - E(x_{dg})\right) = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left|\operatorname{erf}\left(\frac{X-R_p}{\sqrt{2\pi}\sigma}\right)\right|_{X_{dg}}^{X} - \frac{e}{\varepsilon} N_A\left(X - X_{dg}\right) \tag{47a}$$

Substituting equation 45 in equation 47a, we get

$$-E(x) + 0 = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left[1 + \operatorname{erf}\left(\frac{X-R_p}{\sqrt{2\pi}\sigma}\right) - 1 - \operatorname{erf}\left(\frac{x_{dg}-R_p}{\sqrt{2\pi}\sigma}\right)\right] - \frac{e}{\varepsilon} N_A\left(X - X_{dg}\right) \tag{47b}$$

Rearranging and solving equation 47b, we get

$$E(x) = \frac{qQ}{2\epsilon}\left[\operatorname{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2}\sigma}\right) - \operatorname{erf}\left(\frac{X-R_p}{\sqrt{2}\sigma}\right)\right] + \frac{qN_a}{\epsilon}\left(X - X_{dg}\right) \tag{48}$$

The rule for error function's integration can be shown in equation (49)

$$\int \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{(X-R_P)^2}{2\sigma^2}\right) dx = \frac{1}{2\sigma}\left[1 + \text{erf}\left(\frac{X-R_p}{\sigma\sqrt{2}}\right)\right] \quad (49)$$

3.2 Threshold voltage

The Threshold voltage of depletion mode MESFET can be considered that when gate voltage is equal or smaller than threshold voltage, then the channel is completely depleted. And threshold voltage is a negative value for depletion mode MESFET device. In order to determine Vt, one should determine potential equation first.

The potential equation can be determined by integrated electric field equation and can be shown in equation 50. The corresponding device structure and potential position can be shown in Figure 3.4

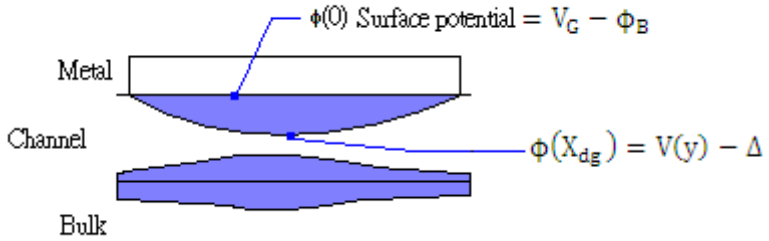


Figure 3.4 Potential boundary conditions were marked above.

$$\int_{X_{dg}}^{\phi(X)} d\phi(X) = \int_{X_{dg}}^{X} -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left[\text{erf}\left(\frac{X-R_p}{\sqrt{2\pi}\sigma}\right) - \text{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right)\right] dX + \int_{X_{dg}}^{X} \frac{e}{\varepsilon} N_A (X - X_{dg}) dx \quad (50)$$

Solving integration on both sides of equation 50, we obtain

$$\phi(X) - \phi(X_{dg}) = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(-\text{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right)\right)(X - X_{dg}) + \text{Solve} + \frac{e}{\varepsilon} N_A \left|\frac{X^2}{2} - X_{dg} X\right|_{X_{dg}}^{X} \quad (50a)$$

Substituting equation 46 in equation 50a, we obtain

$$\phi(X) - V(y) + \Delta = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(-\text{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right)\right)(X - X_{dg}) + \text{Solve} + \frac{e}{\varepsilon} N_A \left(\frac{X^2}{2} - X_{dg} X - \frac{{X_{dg}}^2}{2} + {X_{dg}}^2\right)$$

(50b)

Solving equation 50b, we obtain

$$\phi(X) - V(y) + \Delta = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(\text{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right)\right)(X - X_{dg}) + \text{Solve} + \frac{e}{\varepsilon}N_A\frac{1}{2}(X_{dg} - X)^2 \quad (50d)$$

Where the Solve term can be determined from equation(51)

$$\text{Solve} = \int_{X_{dg}}^{X} -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(\text{erf}\left(\frac{X-R_p}{\sigma\sqrt{2}}\right)\right)dX \quad (51)$$

$$\text{If} \quad u = \frac{X}{\sigma\sqrt{2}} - \frac{R_P}{\sigma\sqrt{2}} \quad => \quad du = \frac{dx}{\sigma\sqrt{2}} - 0 \quad (51a)$$

$$\sigma\sqrt{2}du = dX \quad (51b)$$

$$\int_{X_{dg}}^{X} -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}[\text{erf}(u)]\sigma\sqrt{2}du = -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}\sigma\sqrt{2}\left|u\,\text{erf}(u) + \frac{1}{\sqrt{\pi}}\exp(-u^2)\right|_{X_{dg}}^{X} \quad (51c)$$

Substituting value of u in LHS of equation 51c, we get

$$= -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}\sigma\sqrt{2}\left|\frac{X-R_p}{\sigma\sqrt{2}}\text{erf}\left(\frac{X-R_P}{\sigma\sqrt{2}}\right) + \frac{1}{\sqrt{\pi}}\exp\left(-\frac{(X-R_P)^2}{2\sigma^2}\right)\right|_{X_{dg}}^{X} \quad (51d)$$

Applying the limits and solving equation 51d

$$= -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}\sigma\sqrt{2}\left[\frac{X-R_p}{\sigma\sqrt{2}}\text{erf}\left(\frac{X-R_P}{\sigma\sqrt{2}}\right) + \frac{1}{\sqrt{\pi}}\exp\left(-\frac{(X-R_P)^2}{2\sigma^2}\right) - \frac{X_{dg}-R_p}{\sigma\sqrt{2}}\text{erf}\left(\frac{X-R_P}{\sigma\sqrt{2}}\right) - \frac{1}{\sqrt{\pi}}\exp\left(-\frac{(X_{dg}-R_P)^2}{2\sigma^2}\right)\right] \quad (51e)$$

Further solving equation 51e, we obtain

$$= -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}(X - R_p)\,\text{erf}\left(\frac{X-R_P}{\sigma\sqrt{2}}\right) - \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\frac{\sigma\sqrt{2}}{\sqrt{\pi}}\exp\left(-\frac{(X-R_P)^2}{2\sigma^2}\right) + \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(X_{dg} - R_p)\,\text{erf}\left(\frac{X_{dg}-R_P}{\sigma\sqrt{2}}\right) + \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\frac{\sigma\sqrt{2}}{\sqrt{\pi}}\exp\left(-\frac{(X_{dg}-R_P)^2}{2\sigma^2}\right) \quad (51f)$$

Bring Solve term equation 51f into potential equation 50d, and the interface of metal and channel potential equation can be shown in equation 52

$$\phi(X) - V(y) + \Delta =$$

$$\frac{eQ}{\varepsilon}\frac{1}{2\sigma}\text{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right)(X - X_{dg}) + \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\text{erf}\left(\frac{X_{dg}-R_P}{\sigma\sqrt{2}}\right)(X_{dg} - R_p) - \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(X - R_p)\,\text{erf}\left(\frac{X-R_P}{\sigma\sqrt{2}}\right) + \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\frac{\sigma\sqrt{2}}{\sqrt{\pi}}\exp\left(-\frac{(X_{dg}-R_P)^2}{2\sigma^2}\right) - \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\frac{\sigma\sqrt{2}}{\sqrt{\pi}}\exp\left(-\frac{(X-R_P)^2}{2\sigma^2}\right) + \frac{e}{\varepsilon}N_A\frac{1}{2}(X_{dg} - X)^2 \quad (52)$$

Further solving equation 52, we obtain

$$\phi(X) - V(y) + \Delta = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(X - R_p\right)\left[\operatorname{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) - \operatorname{erf}\left(\frac{X - R_P}{\sigma\sqrt{2}}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{\left(X_{dg} - R_P\right)^2}{2\sigma^2}\right) - \exp\left(-\frac{(X - R_P)^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}\left(X_{dg} - X\right)^2 \quad (52a)$$

The electric potential can be obtained in equation (53)

$$\phi(X) = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(X - R_p\right)\left[\operatorname{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) - \operatorname{erf}\left(\frac{X - R_P}{\sigma\sqrt{2}}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{\left(X_{dg} - R_P\right)^2}{2\sigma^2}\right) - \exp\left(-\frac{(X - R_P)^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}\left(X_{dg} - X\right)^2 + V(y) - \Delta \quad (53)$$

According to this potential equation, one can get the surface potential equations by bring the surface potential boundary conditions equation 54 into equation 53. And the result can be shown in equation 56a

$$\phi(0) = V_G - \phi_B \quad (54)$$

$$\phi\left(X_{dg}\right) = V(y) - \Delta \quad (55)$$

Then

$$\phi(0) = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(R_p\right)\left[\operatorname{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) - \operatorname{erf}\left(\frac{0 - R_P}{\sigma\sqrt{2}}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{\left(X_{dg} - R_P\right)^2}{2\sigma^2}\right) - \exp\left(-\frac{(0 - R_P)^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}\left(X_{dg} - 0\right)^2 + V(y) - \Delta \quad (56)$$

Solving equation 56, we obtain

$$V_G - \phi_B = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}\left(-R_p\right)\left[\operatorname{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) + \operatorname{erf}\left(\frac{R_P}{\sigma\sqrt{2}}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{\left(X_{dg} - R_P\right)^2}{2\sigma^2}\right) - \exp\left(-\frac{{R_P}^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}{X_{dg}}^2 + V(y) - \Delta \quad (56a)$$

Where the error function can be changed by rule $\operatorname{erf}(-u) = -\operatorname{erf}(u)$.

After getting surface potential equation, one can determine the threshold voltage equation by bringing threshold boundary conditions equation 57, equation 58 and equation 59 into surface potential equation 54a.

$$V_G = V_T \tag{57}$$

$$V(y) = 0 = V_P \rightarrow \phi(0) = V_T - \phi_B \tag{58}$$

$$X_{dg} = X_{ds} = X_P \tag{59}$$

Then threshold voltage can be shown in equation 59

$$V_T = -\frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_P - R_p}{\sqrt{2\pi}\sigma}\right) + \mathrm{erf}\left(\frac{R_P}{\sigma\sqrt{2}}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{(X_P - R_P)^2}{2\sigma^2}\right) - \exp\left(-\frac{{R_P}^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}{X_P}^2 + V(y) - \Delta + \phi_B \tag{60}$$

3.3 Approximation derivation process

Where one encounter term of $\exp\left[-\frac{(X-R_p)}{\sqrt{2}\sigma}\right]$. In order to solve this term, the approximation equations are needed and can be determined by using doping profile equation 42. This approximation is basic on reason that doping profile equal to zero in the depletion region between channel and bulk, and the illustration can be shown in Figure 3.5

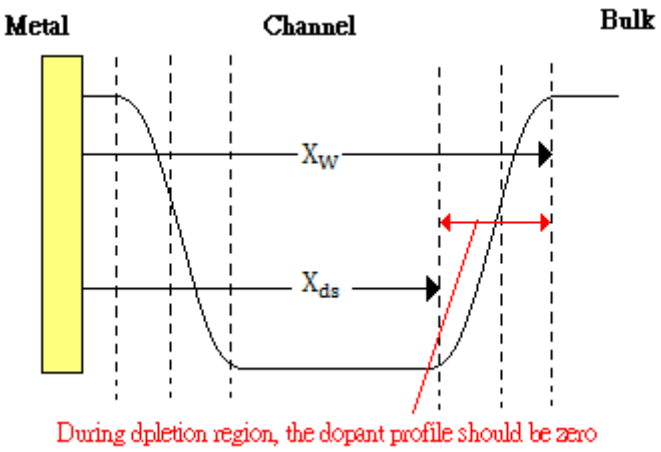


Figure 3.5 Illustration of approximation between channel and bulk.

$$\int_{X_{ds}}^{X_W} N(x)\,dx = 0 \tag{61}$$

Where bring doping equation 42 into equation 61. Then determine equation(X)

$$\int_{X_{ds}}^{X_W} \frac{Q}{\sqrt{2}\sigma} \exp\left[-\frac{(X-R_p)}{\sqrt{2}\sigma}\right]^2 - Na\,dx = 0 \tag{62}$$

$$\frac{Q}{2\sigma}\left|1 + \text{erf}\left(\frac{X-R_P}{\sqrt{2}\sigma}\right)\right|_{X_{ds}}^{X_W} - N_A(X_w - X_{ds}) = 0 \tag{62a}$$

Applying limits and solving equation 62a, we obtain

$$\frac{Q}{2\sigma}\left[\text{erf}\left(\frac{X_W-R_P}{\sqrt{2}\sigma}\right) - \text{erf}\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right)\right] = N_A(X_w - X_{ds}) \tag{62b}$$

where

$$X_w - X_{ds} = \sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}\left(V_{bi} - V_{BS} + V(y)\right)} \tag{63}$$

Where build voltage can be shown in equation 63a

$$V_{bi} = \frac{KT}{q}\ln\frac{N_A N_D}{{n_i}^2} \tag{63a}$$

$$X_W - R_P \gg \sigma \rightarrow \text{erf}\left(\frac{X_W-R_P}{\sqrt{2}\sigma}\right) \cong 1 \tag{64}$$

The approximation result of equation 64 can be determine by Matlab and shown in Figure 3.6

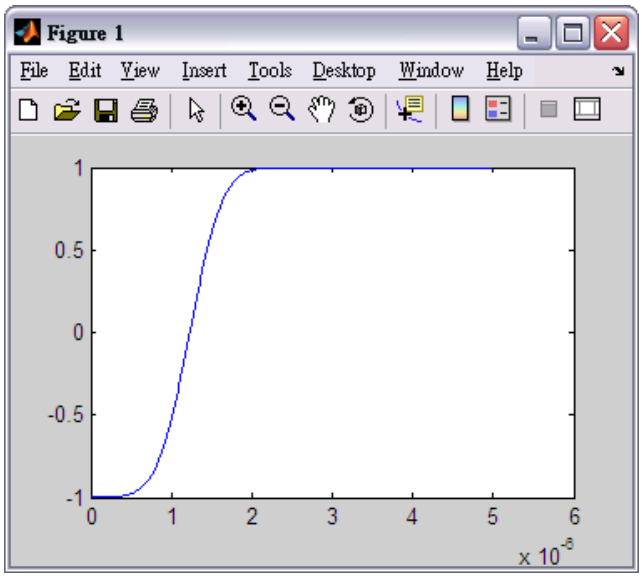


Figure 3.6 $X_W - R_P$ further larger than straggle parameter. The error function will approach to 1.

Bring approximation equations(equation 63 equation 64) into equation 62b, then one can obtain the approximation equations of error function shown in equation 65a

$$\frac{Q}{2\sigma}\left[1 - \text{erf}\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right)\right] = N_A\sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}\left(V_{bi} - V_{BS} + V(y)\right)} \tag{65}$$

Rearranging equation 65, we obtain

$$\mathrm{erf}\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right)=1-\frac{2N_A}{Q}\sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}\left(V_{bi}-V_{BS}+V(y)\right)} \tag{65a}$$

When equation 65a is applied at drain and under pinch off condition and this equation can be rewrite to equation 66. Then one could obtain the solution of $\mathrm{erf}\left(\frac{X_P-R_P}{\sqrt{2}\sigma}\right)$ term.

$$\mathrm{erf}\left(\frac{X_P-R_P}{\sqrt{2}\sigma}\right)=1-\frac{2N_A}{Q}\sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}\left(V_{bi}-V_{BS}+V_P\right)} \tag{66}$$

Another useful approximation is deal with term of $\exp\left(-\frac{(X-X_P)^2}{2\sigma^2}\right)$. For this term, there is a approximation shown in equation 67

$$\exp\left(-\frac{(X-X_P)^2}{2\sigma^2}\right)\cong 1-\mathrm{erf}^2\left(\frac{X-R_P}{\sqrt{2}\sigma}\right) \tag{67}$$

Equation 67 can be prove by using Matlab and the result is shown in Figure 3.7

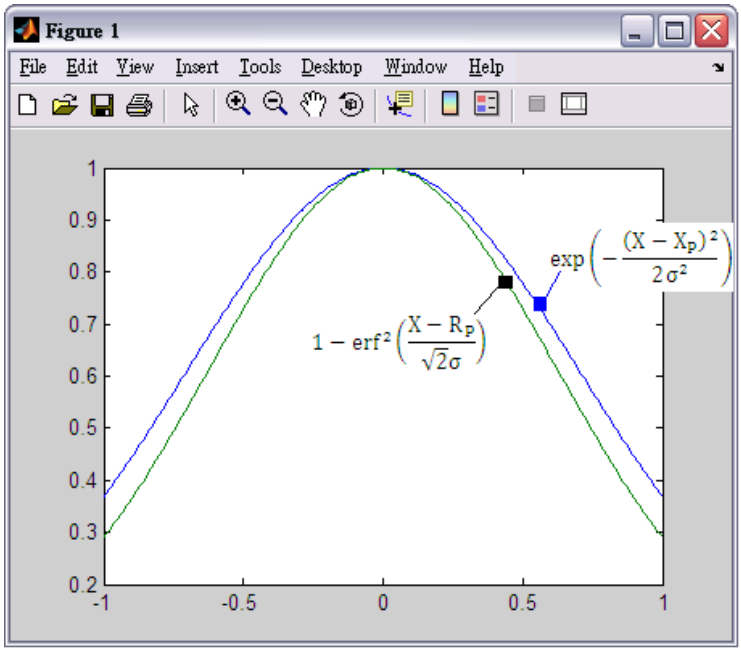


Figure 3.7 Approximation proof of term $\exp\left(-\frac{(X-X_P)^2}{2\sigma^2}\right)$

After getting two useful approximation equations, one can bring equation 66 and equation 67 into threshold voltage equation 60. In equation 60, it is consider term $\exp\left(-\frac{(X_P-R_P)^2}{2\sigma^2}\right)$, one can rewrite equation 60 into equation 69.

$$\exp\left(-\frac{(X_P-R_P)^2}{2\sigma^2}\right)=1-\mathrm{erf}^2\left(\frac{R_P}{\sqrt{2}\sigma}\right) \tag{68}$$

Substituting values in equation 68

$$=1-\left[1-4\frac{N_A}{Q}\sqrt{\frac{2\epsilon}{qN_A}(V_{bi}-V_{BS})}+\frac{4{N_A}^2}{Q^2}\left(\frac{2\epsilon}{qN_A}(V_{bi}-V_{BS})\right)\right] \tag{68a}$$

$$=4\frac{N_A}{Q}\sqrt{\frac{2\epsilon}{qN_A}(V_{bi}-V_{BS})}-\frac{8N_A}{Q^2}\frac{\epsilon}{q}(V_{bi}-V_{BS}) \tag{68b}$$

Then bring equation 66 and equation 68b into equation 60 and one can obtain threshold voltage V_T equation.

$$\begin{aligned}V_T=&-\frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[1-\frac{2N_A}{Q}\sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}(V_{bi}-V_{BS})}+\mathrm{erf}\left(\frac{R_P}{\sigma\sqrt{2}}\right)\right]\\&-\frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{{R_P}^2}{2\sigma^2}\right)-4\frac{N_A}{Q}\sqrt{\frac{2\epsilon}{qN_A}(V_{bi}-V_{BS})}-\frac{8N_A}{Q^2}\frac{\epsilon}{q}(V_{bi}-V_{BS})\right]\\&+\frac{e}{\varepsilon}N_A\frac{1}{2}{X_P}^2+V(y)-\Delta+\phi_B\end{aligned} \tag{69}$$

3.4 I-V Characteristics

The idea for determine drain current is to integrate total free charge in the un-depleted section of the channel. The basic equation can be shown in equation 70

$$I_{DS}=q\mu\frac{Z}{L}\int_0^{V_{ds}}Q_n(V)dv \tag{70}$$

Where Q_n term means that total free charge in the un-depleted channel region.

For determine Q_n, need to integrate implanted doping profile under channel from X_{dg} to X_{ds} and the energy band diagram for integration area can be shown in blue area in Figure 3.8. The Q_n derivation can be shown in equation 71.

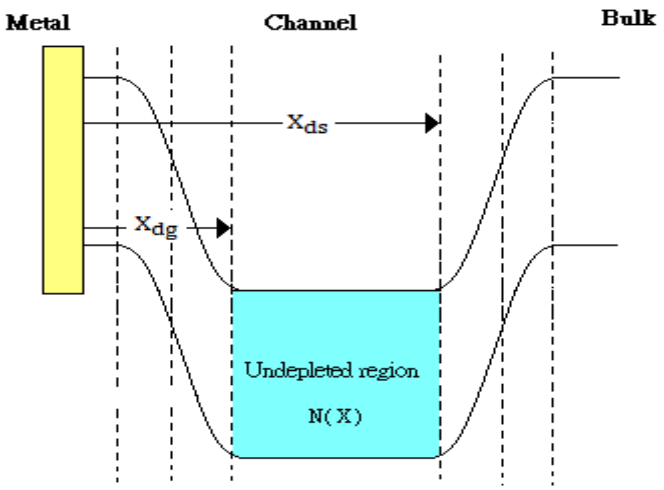


Figure 3.8 Energy band diagram for showing un-depleted channel region.

$$Q_n = \int_{X_{ds}}^{X_{dg}} N(x)dx \tag{71}$$

Substituting value of N(x), we get

$$Q_n = \int_{X_{dg}}^{X_{ds}} \frac{Q}{\sqrt{2}\sigma} \exp\left[-\frac{(X-R_p)}{\sqrt{2}\sigma}\right]^2 - Na\, dx \tag{71a}$$

Solving integration

$$Q_n = \frac{Q}{2\sigma}\left|1 + erf\left(\frac{X-R_P}{\sqrt{2}\sigma}\right)\right|_{X_{dg}}^{X_{ds}} - N_A(X_{dg} - X_{ds}) \tag{71b}$$

Applying limits value, we obtain

$$Q_n = \frac{Q}{2\sigma}\left[1 + erf\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right) - 1 - erf\left(\frac{X_{dg}-R_P}{\sqrt{2}\sigma}\right)\right] - N_A(X_{dg} - X_{ds}) \tag{71c}$$

In equation 71c, ignore background minority concentration (acceptor) in implanted region. Because N_A is much smaller than N_D. And equation 71c can be rewrite to equation 72

$$Q_n = \frac{Q}{2\sigma}\left[erf\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right) - erf\left(\frac{X_{dg}-R_P}{\sqrt{2}\sigma}\right)\right] \tag{72}$$

For determine Q_n, one need approximation for solve term $erf\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right)$ and $erf\left(\frac{X_{dg}-R_P}{\sqrt{2}\sigma}\right)$. First error function can be obtained from equation 65a, and the second error function can be determined by subtracting equation 76 from equation 74.

For finding term $\mathrm{erf}\left(\frac{X_{ds}-R_P}{\sqrt{2}\sigma}\right)$, surface potential boundary condition $\phi(0)$ will be applied into potential equation 53 and get the first relative equation 73.

$$\phi(0) = V_G - \phi_B = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(-R_p)\left[\mathrm{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right) + \mathrm{erf}\left(\frac{R_P}{\sigma\sqrt{2}}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{(X_{dg}-R_P)^2}{2\sigma^2}\right) - \exp\left(-\frac{{R_P}^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}{X_{dg}}^2 + V(y) - \Delta \quad (73)$$

Rearranging equation 73

$$V = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right) + \mathrm{erf}\left(\frac{R_P}{\sigma\sqrt{2}}\right)\right] - \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{(X_{dg}-R_P)^2}{2\sigma^2}\right) - \exp\left(-\frac{{R_P}^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}{X_{dg}}^2 + \Delta + V_G - \phi_B \quad (74)$$

For finding second relative equation the pinch off boundary condition will be considered and shown in equation 75 and equation 76

$$V = V_P = V_{GS} - V_T \quad (75)$$

$$X_{dg} = X_{ds} = X_P \quad (76)$$

Substituting values for second relative equation

$$V_P = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_P - R_p}{\sqrt{2\pi}\sigma}\right) + \mathrm{erf}\left(\frac{R_P}{\sigma\sqrt{2}}\right)\right] - \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{(X_P - R_P)^2}{2\sigma^2}\right) - \exp\left(-\frac{{R_P}^2}{2\sigma^2}\right)\right] + \frac{e}{\varepsilon}N_A\frac{1}{2}{X_P}^2 + \Delta + V_G - \phi_B \quad (77)$$

After getting two relative equation, use equation 74 subtract equation 77 and the new equation can be shown in eq78.

$$V - V_P = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_{dg}-R_p}{\sqrt{2\pi}\sigma}\right) - \mathrm{erf}\left(\frac{X_P-R_p}{\sqrt{2\pi}\sigma}\right)\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[\exp\left(-\frac{(X_P-R_P)^2}{2\sigma^2}\right) - \exp\left(-\frac{(X_{dg}-R_P)^2}{2\sigma^2}\right)\right] - N_A\frac{Q}{\epsilon}\frac{1}{2}\left({X_{dg}}^2 - {X_P}^2\right) \quad (78)$$

Let reduce previous equation 78 by substitute term

$\mathrm{erf}\left(\frac{X_P - R_p}{\sqrt{2\pi}\sigma}\right) = 1 - \frac{2N_A}{Q}\sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}(V_{bi} - V_{BS} + V_P)}$, and set $a_P = \frac{2N_A}{Q}\sqrt{\frac{2\epsilon}{q}\frac{1}{N_A}(V_{bi} - V_{BS} + V_P)}$

and bring it into equation 78.

And the result can be shown in equation 78a

$$V - V_P =$$

$$\frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) - 1 + a_P\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[1 - \mathrm{erf}^2\left(\frac{X_P - R_P}{\sqrt{2}\sigma}\right) - \exp\left(-\frac{(X_{dg} - R_P)^2}{2\sigma^2}\right)\right] \quad (78a)$$

Where $N_A\frac{Q}{\epsilon}\frac{1}{2}\left({X_{dg}}^2 - {X_P}^2\right)$ is ignored because N_A is very small in the implanted region.

$$V - V_P = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) - 1 + a_P\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[1 - (1 - a_P)^2 - 1 + \mathrm{erf}^2\left(\frac{X_{dg} - R_P}{\sigma\sqrt{2}}\right)\right] \quad (78b)$$

After organize equation 78b, Then $V - V_P$ can be shown in equation 78c

$$V - V_P = \frac{eQ}{\varepsilon}\frac{1}{2\sigma}(R_p)\left[\mathrm{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) - 1 + a_P\right] + \frac{eQ}{\varepsilon}\frac{1}{\sqrt{2\pi}}\left[+\mathrm{erf}^2\left(\frac{X_{dg} - R_P}{\sigma\sqrt{2}}\right) - (1 - a_P)^2\right] \quad (78c)$$

Set term $\mathrm{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right)$ equal to X, $P_1 = \frac{R_P}{2\sigma}\frac{qQ}{\epsilon}$ and $P_2 = \frac{qQ}{\epsilon}\frac{1}{\sqrt{2\pi}}$, rewrite into equation 79.

$$V - V_P = P_1[X - 1 + a_P] + P_2[X^2 - 1 + 2a_P - {a_P}^2] \quad (79)$$

$$V - V_P = P_1X - P_1 + P_1a_P + P_2X^2 - P_2 + 2P_2a_P - P_2{a_P}^2 \quad (79a)$$

$$V - V_P = P_2X^2 + P_1X + P_1(a_P - 1) + P_2(1 - 2a_P + {a_P}^2) \quad (79b)$$

$$P_2X^2 + P_1X + P_1(a_P - 1) + P_2(1 - a_P)^2 - V + V_P = 0 \quad (79c)$$

Then get this solution of quadratic by using $\mathrm{solve} = \frac{-b \mp \sqrt{b^2 - 4ac}}{2a}$ and the solution of term

$\mathrm{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right)$ can be shown in equation 80b.

$$\mathrm{erf}\left(\frac{X_{dg} - R_p}{\sqrt{2\pi}\sigma}\right) = \frac{-P_1}{2P_2}\sqrt{\frac{{P_1}^2}{4{P_2}^2} - \frac{P_1}{P_2}(a_P - 1) - (1 - a_P)^2 - \frac{1}{P_2}(V - V_P)} \quad (80a)$$

$$= -\frac{R_P}{2\sigma}\sqrt{\frac{\pi}{2}} + \sqrt{\frac{{R_P}^2\pi}{8\sigma^2} + \frac{R_P}{\sigma}\sqrt{\frac{\pi}{2}}(a_p - 1) + (a_P - 1)^2 + \frac{\epsilon\sqrt{2\pi}}{qQ}(V - V_P)} \quad (80b)$$

Bring equation 80a and equation 65a into equation 72 and one can get free charge in un-depleted region Q_n and Q_n can be organized into equation 81.

$$Q_n = \frac{Q}{2}\left\{(1+\alpha) - \sqrt{{a_P}^2 + \frac{V-V_P}{V_1}} - \sqrt{(\alpha + 1 - {a_P}^2) + \frac{V-V_P}{V_2}}\right\} \quad (81)$$

The final step, bring equation 81 into equation 82 for determine the I-V characteristic and the current equation can be shown in equation 83

$$I_{DS} = q\mu\frac{Z}{L}\int_0^{V_{DS}} Q_n\,dv \quad (82)$$

Substitute value of Q_n from equation 81 into equation 82, we obtain

$$I_{DS} = q\mu\frac{Z}{L}\frac{Q}{2}\int_0^{V_{DS}} (1+\alpha) - \sqrt{{a_P}^2 + \frac{V-V_P}{V_1}} - \sqrt{(\alpha + 1 - {a_P}^2) + \frac{V-V_P}{V_2}}\,dv \quad (83)$$

For solving integration, equation 83 can be rewrite to equation 84

$$I_{DS} = q\mu\frac{Z}{L}\frac{Q}{2}[(1+\alpha)V_{DS} - (Solve1) - (Solve2)] \quad (84)$$

Where term Solve1 and Solve2 can be shown in equation 85 and equation 86

$$Solve1 = \int_0^{V_{DS}} \sqrt{{a_P}^2 + \frac{V-V_P}{V_1}}\,dV \quad (85)$$

$$Solve2 = \int_0^{V_{DS}} \sqrt{(\alpha + 1 - {a_P}^2) + \frac{V-V_P}{V_2}}\,dV \quad (86)$$

For determine Solve1, set $u = {a_P}^2 + \frac{V}{V_1} - \frac{V_P}{V_1}$

➔ $\frac{du}{dV} = 0 + \frac{1}{V_1} - 0$ (87a)

➔ $V_1\,du = dV$ (87b)

Bring equation 87 into equation 85 and one can get equation 88

$$Solve1 = V_1\int_0^{V_{DS}} [u]^{\frac{1}{2}}\,du \quad (88)$$

$$= V_1 \left|\frac{2}{3} u^{\frac{3}{2}}\right|_0^{V_{DS}} \quad (88a)$$

Bring term $u = {a_P}^2 + \frac{V}{V_1} - \frac{V_P}{V_1}$ back to equation 88 and one get equation 89

$$\text{Solve1} = V_1 \frac{2}{3}\left[\left({a_P}^2 + \frac{V_{DS} - V_P}{V_1}\right)^{\frac{3}{2}} - \left({a_P}^2 + \frac{V_P}{V_1}\right)^{\frac{3}{2}}\right] \quad (89)$$

For Solve2, set $u = (\alpha + 1 - {a_P}^2) + \frac{V - V_P}{V_2}$

➔ $\frac{du}{dV} = 0 + \frac{1}{V_2} - 0$ (90)

➔ $V_2 du = dV$ (91)

Bring equation 91 into equation 88a and one can get equation 93

$$\text{Solve2} = V_1 \int_0^{V_{DS}} [u]^{\frac{1}{2}} du \quad (92)$$

$$= V_2 \left|\frac{2}{3} u^{\frac{3}{2}}\right|_0^{V_{DS}} \quad (93)$$

Bring term $u = (\alpha + 1 - {a_P}^2) + \frac{V - V_P}{V_2}$ back to equation 93 and one get equation 94

$$\text{Solve2} = V_2 \frac{2}{3}\left[\left[(\alpha + 1 - {a_P}^2) + \frac{V_{DS} - V_P}{V_2}\right]^{\frac{3}{2}} - \left[(\alpha + 1 - {a_P}^2) + \frac{V_P}{V_2}\right]^{\frac{3}{2}}\right] \quad (94)$$

After getting Solve1 and Solve2, bring equation 89 and equation 94 back into drain current equation 84 Finally, I-V characteristic equation can be shown in equation 95

$$I_{DS} = q\mu \frac{Z}{L}\frac{Q}{2}\left\{(1 + \alpha)V_{DS} - V_1 \frac{2}{3}\left[\left({a_P}^2 + \frac{V_{DS} - V_P}{V_1}\right)^{\frac{3}{2}} - \left({a_P}^2 + \frac{V_P}{V_1}\right)^{\frac{3}{2}}\right] - V_2 \frac{2}{3}\left[\left[(\alpha + 1 - {a_P}^2) + \frac{V_{DS} - V_P}{V_2}\right]^{\frac{3}{2}} - \left[(\alpha + 1 - {a_P}^2) + \frac{V_P}{V_2}\right]^{\frac{3}{2}}\right]\right\} \quad (95)$$

3.5 Gate to source capacitance

Gate to source capacitance, C_{gs} is a typical parameter for showing device input capacitance. Due to the miller effect, Gate to drain capacitance will also increase the input capacitance although to a much lesser degree. Since C_{gs} is found in the standard way by integrating the total free charge in the channel and then differentiating this quantity with respect to the gate voltage. The equation for C_{gs} can be shown in equation 96[105].

$$C_{gs} = \frac{qQZL}{2}\left\{\frac{M}{2\sqrt{MR+A_1}} + \frac{\sqrt{N}}{2\left(\sqrt{N}-\sqrt{R}\right)^2}\left[\frac{\sqrt{MN+A_1}}{\sqrt{R}} - \frac{M\left(\sqrt{N}-\sqrt{R}\right)}{\sqrt{MR+A_1}} - \frac{\sqrt{MR+A_1}}{\sqrt{R}} - \frac{1}{Q}\sqrt{\frac{2N_B\epsilon}{q}}\left\{\frac{2\left(\sqrt{N}-\sqrt{R}\right)}{\sqrt{R}}\frac{V_{DS}}{\sqrt{RN}}\right\}\right]\right\} \quad (96)$$

Where

$$N = V_{bi} - V_{GS} - V_{DS} \quad (96a)$$

$$R = V_{bi} - V_{GS} \quad (96b)$$

$$M = \frac{4\alpha\epsilon}{qQR_p} \quad (96c)$$

$$A_1 = \alpha^2 + A_3 \quad (96d)$$

$$\alpha = \frac{R_P}{2\sigma}\sqrt{\frac{\pi}{2}} \quad (96e)$$

$$A_2 = \mathrm{erf}\left(\frac{R_p}{2\sigma}\right) - \alpha \quad (96f)$$

$$A_3 = 1 - \exp\left[-\left(\frac{R_P}{\sqrt{2}\sigma}\right)^2\right] - 2\alpha\mathrm{erf}\left[\frac{R_P}{\sqrt{2}\sigma}\right] \quad (96g)$$

3.6 Breakdown voltage consideration

For drain voltages beyond Vdsat, the drain current is assumed to remain essentially the same as the saturation current. As the drain voltage increase further, breakdown occurs where the current rises sharply with the drain bias. This breakdown occurs at the gate edge toward the drain side where the field is the highest. Analysis of the breakdown condition in an FET is inherently more complicated than in a bipolar transistor because it is a two-dimensional

situation as opposed to one-dimensional.

The fundamental mechanism responsible for breakdown is impact ionization. Since impact ionization is a strong function of the electric field, the maximum field is often regarded as the first-order criterion for breakdown. Using a simple one-dimensional analysis in the x-direction, and treating the gate-drain structure as a reverse-biased diode, the drain breakdown voltage V_{db} is similar to that of the gate-junction breakdown and is linearly dependent on the relative voltage of the drain to the gate;

$$V_{db} = V_b - V_{gb} \tag{97}$$

Where, V_b is the gate break-down voltage.

Unlike a MOSFET where the heavily doped source and drain overlap the gate at the gate edges, the JFETs and MESFET have a gap between the gate and the source/drain contacts (or heavily doped regions under the contacts). For breakdown consideration, this gate-drain distance is critical. In this gap the doping level is the same as the channel. If surface traps are present in this gate-drain spacing, they can deplete part of the channel doping and affect the field distribution. In certain cased they can improve the breakdown voltage. Without surface traps, the field is highest at the gate edge where breakdown occurs. Using a one-dimensional analysis, the field at the gate edge can be shown in equation 98

$$E(L) = \frac{qN_d}{\epsilon_s}\sqrt{\frac{2\epsilon_s}{qN_d}(\psi_{bi} + v_D - v_G) - \frac{N`_{st}}{N_d}L_{GD}{}^2} \tag{98}$$

$N`_{st}$ is the density of surface trap. This equation implies that Lgd is larger than the depletion width so that $N`_{st} = 0$, $E(L)$and V_{db} are dependent of Lgd. the break-down in MESFET are less controllable and have different breakdown behavior compared to Si JFETs. One factor for a reduced breakdown voltage in MESFET is due to tunneling current associated with the Schottly-barrier gate contact. At high fields, this tunneling currents from thermionic-field emission which has temperature dependence. The gate current can initiate avalanche multiplication and induces lower drain breakdown voltage. With higher channel

current, the internal node is at a higher temperature which triggers an earlier gate-current-initiated avalanche breakdown. This can be responsible for lower V_{db} at higher Vg. The higher channel current can initiate avalanche at a lower voltage, or produce the temperature effects which trigger earlier breakdown as discussed. The breakdown voltage can be improved by extending the region between the gate and the drain. Furthermore, to maximize its function, the field distribution should be made as uniform as possible. One technique is to introduce a doping gradient in the lateral direction. Another, called RESURF (reduced surface field), is to have a p-layer underneath such that at high drain bias, this n-layer is fully depleted [105].

3.7 Transconductance (gm)

The transconductance of the silicon MESFET is obtained by differentiating I_{DS} with respect to V_{GS}, the equation can be shown in equation 99.

$$gm = \frac{q\mu ZQ}{4L}\left[\frac{8N_A\epsilon}{qQ^2a_P} + \frac{\sqrt{2\pi\epsilon}}{qQ\sigma(\alpha+1-a_P)}\right](V_{GS} - V_T) \quad (99)$$

$$\text{Where } a_P = \frac{2N_A}{Q}\sqrt{\frac{2\epsilon}{qN_A}\left(V_{bi} - V_{BS} + V_p\right)}$$

3.8 Cut off frequency calculation

The cut off frequency calculation of MESFET is determined by the transconductance and gate to source capacitance C_{gs}, and the equation can be shown in equation 100

$$f_T = \frac{gm}{2\pi C_{gs}} \quad (100)$$

CHAPTER 4

Process simulation using TCAD sentaurus tool

4.1 Introduction

Sentaurus Process is an advanced 1D, 2D and 3D process simulator for developing and optimizing silicon semiconductor process technologies. It is a new-generation process simulator for addressing the challenges found in current and future process technologies. Equipped with a set of advanced process models, which include default parameters calibrated with data from equipment vendors, Sentaurus Process provides a predictive framework for simulating a broad range of technologies from nanoscale CMOS to large-scale high-voltage power devices. Sentaurus Process is part of a comprehensive suite of core TCAD products for multi-dimensional process, device, and system simulations, embedded into a powerful user interface [107].

Sentaurus Process is a complete and highly flexible, multidimensional, process modeling environment. With its modern software architecture and extensive breadth of capabilities, Sentaurus Process is a state-of-the-art process simulation tool. Calibrated to a wide range of the latest experimental data using proven calibration methodology, Sentaurus Process offers unique predictive capabilities for modern silicon and non-silicon technologies [108].

Sentaurus Process accepts as input a sequence of commands that is either entered from standard input (that is, at the command prompt) or composed in a command file. A process flow is simulated by issuing a sequence of commands that corresponds to the individual process steps. Parameter settings should be in a separate file, which is sourced at the beginning of input files using the source command [108]. Several commands allow you to select physical models and parameters, grid strategies, and graphical output preferences if required. In addition, a special language (Alagator) allows to describe and implement unique models and diffusion equations [108].

4.2 Benefits to use S-Process

- Fast prototyping, development, and optimization of a broad range of technologies with comprehensive physics-based process modeling capabilities.
- Enhance device performance by optimization of thermal and mechanical stress in process structures with stress history.
- Provides insights into advanced physical phenomena through self-consistent multi-dimensional modeling capabilities [108].

4.3 Starting Sentaurus Process

Sentaurus Process can be run in either the interactive mode or batch mode. In the interactive mode, a whole process flow can be simulated by entering commands line-by-line as standard input. To start Sentaurus Process in the interactive mode, enter the following on the command line:

> sprocess

Sentaurus Process displays version and host information, followed by the Sentaurus Process command prompt. Now to enter Sentaurus Process commands at the prompt:

sprocess>

This is a flexible way of working with Sentaurus Process to test individual process steps or short sequences, but it is inconvenient for long process flows. It is more useful to compile the command sequence in a command file, which can be run in batch mode or inside Sentaurus Workbench [108].

To run Sentaurus Process in batch mode, load a command file when starting Sentaurus Process, for example:

> sprocess input.cmd

4.3.1 Defining Initial Grid

The initial 1D grid is defined with the line command:

```
line y loc=3.0 spa=0.2 tag=left
line y loc=6.0 spa=0.2 tag=right
line x loc=1 spa=0.25 tag=top
line x loc=5 tag=bottom
```

The first argument of the line specifies the direction of the grid. For 1D, this is always x. The grid spacing is defined by pairs of the location and spacing keywords. The keyword spacing defines the spacing between two grid lines at the specified location. Sentaurus Process expands or compresses the grid spacing linearly in between two locations defined in the line command.

4.3.2 Defining Initial Simulation Domain

The initial simulation domain is defined with the region command:

```
# Silicon substrate definition
region Silicon xlo=top xhi=bottom ylo=left yhi=right
```

The keyword silicon specifies the material of the region. The keywords xlo and xhi take tags as arguments, which are defined in the line command.

4.3.3 Initializing the Simulation

The simulation is initialized with the init command:

```
init concentration= 1e19 field= $Boron    wafer.orient=100    slice.angle=[CutLine2D 0 0 1.0 0]
```

Here, the initial boron concentration in the silicon wafer (as defined in the previous region command) is set to 10^{19} cm^{-3}.

4.3.4 Setting up a Meshing Strategy

The initial grid is valid until the first command that changes the geometry, such as oxidation, deposition, and etching. For these steps, a remeshing strategy must be defined. Sentaurus Process can use Sentaurus Mesh or MGOALS as remeshing engines. MGOALS also performs etching and deposition. Sentaurus Mesh is the default.

To define a remeshing strategy, use:

mgoals on normal.growth.ratio=1.1 min.normal.size= 3<nm> max.lateral.size=0.2<um>

where:

- The keyword min.normal.size determines the grid spacing of the first layer starting from the interface.
- The keyword max.lateral.size limits not only the lateral grid spacing for 2D simulations, but also the maximum grid spacing anywhere.
- The keyword normal.growth.ratio determines how fast the grid spacing can increase from one layer to another.

4.3.5 Depositing Oxide Layer

A faster alternative to the simulation of the oxide growth is to deposit an oxide layer and to simulate afterwards a thermal cycle to account for the thermal budget during the oxidation. This is an efficient way to emulate the creation of the oxide if oxidation-enhanced diffusion (OED) and the silicon consumption during the oxidation are not important.

To deposit a layer of oxide, use:

deposit material = Oxide type = isotropic rate = {1.0} time=0.3

mask name=mask_1_2 segments = {-0.1 1.5 4.5 6.1 } negative

photo mask=mask_1_2 thickness=1

etch material = Oxide type= anisotropic rate= {10.0} time= 0.027

strip Photoresist

4.3.6 Channel Ion-Implantation

To implant arsenic with an energy of 35 keV, a dose of 10^{14} cm^{-2}, an implant tilt of 7°, and a wafer rotation -90°, use:

```
refinebox min= { -0.1 0.5 } max= { 0.7 1.5 } xrefine= 0.04 yrefine= 0.05
refinebox min= { -0.1 4.5 } max= { 0.7 5.5 } xrefine= 0.04 yrefine= 0.05
grid remesh

#During Channel ion-implantation step, the Arsenic is to be used for channel dopant.
implant $Phosphorus dose= @channel_dose@ energy= 35 tilt=7 rot=-90
temp_ramp name=tempramp_1_2 time=0.01 temp=800
diffuse temp_ramp=tempramp_1_2
```

4.3.7 Implanting Source/Drain

The source and drain regions are created using:

```
#Deposit another Nitride layer for source and drain ion-implantation window.
deposit material= Oxide type= isotropic rate= {1.0} time=1
mask name=mask_1_3 segments = {-0.1 0.75 1.45 4.55 5.25 6.1 } negative
photo mask=mask_1_3 thickness=1

#Etch the Nitride for forming the ion implantation window of source and drain.
etch material= Oxide type= anisotropic rate = {10.0} time=1.1
strip Photoresist
deposit material= Oxide type = isotropic rate= {1.0} time=0.02

#Do ion-plantation with Arsenic for forming source and drain well.
```

implant $D2 dose= 1e14 energy= 55 tilt=0 rot=0

temp_ramp name=tempramp_1_3 time=0.01 temp=800

diffuse temp_ramp=tempramp_1_3

To ensure a low resistivity of the source and drain regions, this implant step uses a very high dose of 10^{14} cm^{-2}. A tilt of 0° is used to reduce channeling and a rotation of 0° ensures that the plane of incident is parallel to the gate stack, such that the 0° tilt angle does not lead to asymmetry between the source and drain.

4.3.8 Deposit Aluminum to split SD_CONTACTS

To deposit a layer of Aluminum, use:

etch material= Oxide type=anisotropic rate = {0.5} time=1

deposit Aluminum isotropic thickness= 0.55 selective.materials= { Silicon }

mask name=mask_1_4 segments = {-0.1 2.25 3.75 6.1 } negative

photo mask=mask_1_4 thickness=1

etch material = Oxide type=anisotropic rate = {10.0} time=1.1

strip Photoresist

4.3.9 Defining Titanium Gate

The Titanium gate is created using:

#Titanium is deposited on the surface of MESFET for schottky contact

deposit material= {Titanium} type = isotropic rate = {1.0} time=0.25

etch material= {Titanium} type= cmp coord= -0.25

strip Photoresist

4.3.10 Remeshing for Device Simulation

In the following commands, the internal technique is used to produce a structure and mesh appropriate for device simulation.

```
# Remeshing for the device simulation
# clear the process simulation mesh
refinebox clear
refinebox !keep.lines
line clear
# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error       1e37
pdbSet Grid AdaptiveField Refine.Rel.Error       1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0
pdbSet Grid Adaptive 1
pdbSet Grid SnMesh DelaunayType boxmethod

refinebox name= Substrate \
   refine.fields= { NetActive } def.max.asinhdiff= 1 \
   adaptive silicon add

refinebox name= Channel_Interface \
   min= "-0.1 3.0" \
   max= "0.7 5.5" \
   min.normal.size= 2e-3 normal.growth.ratio= 1.5 \
   interface.materials= {Silicon } all add
```

grid remesh

transform reflect left

contact name= source point x= -0.2 y= 1.0

contact name= drain point x= -0.2 y= 5.0

contact name= substrate bottom

contact name= gate point x= -0.1 y= 3.0

struct smesh= n@node@

After finish the structure, next step is going to simulate this device by using S-Device software. By editing the input command file, one could execute this text file with S-Device and after that S-Device would generate two files of the results, one of them is .tdr file, another one is .plt. Both two files contain all the electrical properties and the designer could open it through software Tecplot 360, or Inspect.

CHAPTER 5
Device simulation using TCAD sentaurus tool

5.1 Introduction

Sentaurus Device simulates numerically the electrical behavior of a single semiconductor device in isolation or several physical devices combined in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and conduction mechanisms. A real semiconductor device, such as a transistor, is represented in the simulator as a 'virtual' device whose physical properties are discretized onto a nonuniform 'grid' (or 'mesh') of nodes. Therefore, a virtual device is an approximation of a real device. Continuous properties such as doping profiles are represented on a sparse mesh and, therefore, are only defined at a finite number of discrete points in space. The doping at any point between nodes (or any physical quantity calculated by Sentaurus Device) can be obtained by interpolation[109]. Each virtual device structure is described in the Synopsys TCAD tool suite by a TDR file containing the following information:

1. The grid (or geometry) of the device contains a description of the various regions, that is, boundaries, material types, and the locations of any electrical contacts. It also contains the locations of all the discrete nodes and their connectivity.
2. The data fields contain the properties of the device, such as the doping profiles, in the form of data associated with the discrete nodes. The doping profile of a MESFET structure discretized by a mixed-element grid. By default, a device simulated in 2D is assumed to have a 'thickness' in the third dimension of 1μm.

The features of Sentaurus Device are many and varied. They can be summarized as:

1. An extensive set of models for device physics and effects in semiconductor devices (drift diffusion, thermodynamic, and hydrodynamic models).
2. General support for different device geometries (1D, 2D, 3D, and 2D cylindrical).

3. Mixed-mode support of electrothermal net lists with mesh-based device models.

5.2 Meshing device structure

Device structures can be created in various ways, including 1D, 2D, or 3D process simulation (Sentaurus Process), 2D or 3D process emulation (Sentaurus Structure Editor), and 2D or 3D structure editors (Sentaurus Structure Editor). Regardless of the means used to generate a virtual device structure, it is recommended that the structure be remeshed using Sentaurus Structure Editor (2D and 3D meshing with an interactive graphical user interface (GUI)) or Sentaurus Mesh (1D, 2D, and 3D meshing without a GUI) to optimize the grid for efficiency and robustness [109].

For maximum efficiency of a simulation, a mesh must be created with a minimum number of vertices to achieve the required level of accuracy. For any given device structure, the optimal mesh varies depending on the type of simulation. It is recommended that to create the most suitable mesh, the mesh must be densest in those regions of the device where the following are expected:

1. High current density (MESFET channels, bipolar base regions)
2. High electric fields.
3. High charge generation (single event upset (SEU) alpha particle, optical beam)

For example, accurate drain current modeling in a MOSFET requires very fine, vertical, mesh spacing in the channel at the oxide interface (of the order) when using advanced mobility models. For reliable simulation of breakdown at a drain junction, the mesh must be more concentrated inside the junction depletion region for good resolution of avalanche multiplication. Generally, a total node count of 2000 to 4000 is reasonable for most 2D simulations. Large power devices and 3D structures require a considerably larger number of elements [109].

5.3 Tool Flow

In a typical device tool flow, the creation of a device structure by process simulation (Sentaurus Process) is followed by re-meshing using Sentaurus Structure Editor or Sentaurus Mesh. In this scheme, control of mesh refinement is handled automatically through the file _dvs.cmd. Sentaurus Device is used to simulate the electrical characteristics of the device. Finally, Tecplot SV is used to visualize the output from the simulation in 2D and 3D, and Inspect is used to plot the electrical characteristics.

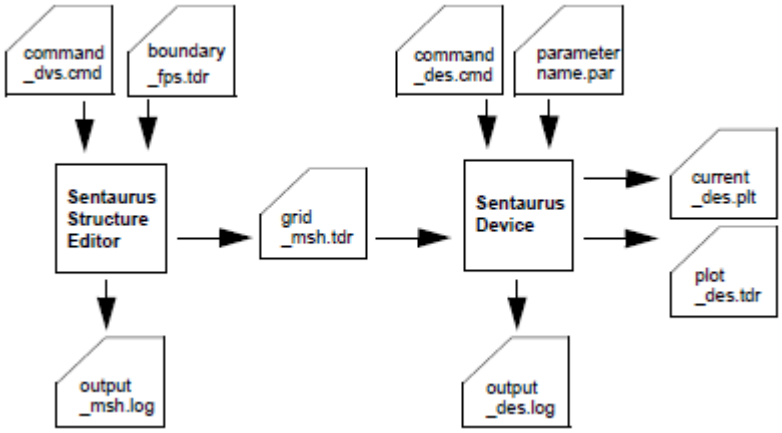


Figure 5.1

5.4 Starting Sentaurus Device

There are two ways to start Sentaurus Device: from the command line or Sentaurus Workbench.

From Command line

Sentaurus Device is driven by a command file and run by the command:

sdevice <command_filename>

From Sentaurus Workbench

Sentaurus Device is launched automatically through the Scheduler when working inside Sentaurus Workbench.

Sentaurus Workbench interprets # as a special marker for conditional statements. When Sentaurus Device starts, the command file is checked for correct syntax, and the commands are executed in sequence.

5.5 Sentaurus Device Command file

The Sentaurus Device command file is organized in command or statement sections that can be in any order (except in mixed-mode simulations). Sentaurus Device keywords are not case sensitive and most can be abbreviated. Each command file contain number of sections of statements. Basically it is divided into 6 sections.

1. File Section
2. Electrode Section
3. Physics Section
4. Plot Section
5. Math Section
6. Solve Section

5.5.1 File Section

First, the input files that define the device structure and the output files for the simulation results must be specified.

The device is defined by the file nmes_msh.tdr:

```
File {
* input files:
Grid = "nmes_msh.tdr"
* output files:
Plot = "n1_des.tdr"
Current = "n1_des.plt"
```

Output = "n1_des.log"

}

The File section specifies the input and output files necessary to perform the simulation.

* input files:

This is a comment line.

Grid = "nmes_msh.tdr"

This essential input file defines the mesh and various regions of the device structure, including contacts. Sentaurus Device automatically determines the dimensionality of the problem from this file. It also contains the doping profiles data for the device structure.

* output files:

This is a comment line.

Plot = "n1_des.tdr"

This is the file name for the final spatial solution variables on the structure mesh.

Current = "n1_des.plt"

This is the file name for electrical output data (such as currents, voltages, charges at electrodes). Its standard extension is _des.plt.

Output = "n1_des.log"

This is an alternate file name for the output log or protocol file that is automatically created whenever Sentaurus Device is run. This file contains the redirected standard output, which is generated by Sentaurus Device as it runs.

The device in this example is two-dimensional. By default, Sentaurus Device assumes a ‘thickness’ of 1μm. This effective width is adjusted by specifying an Area Factor in the Physics section, or an AreaFactor for each electrode individually. An Area Factor is a multiplier for the electrode currents and charges.

5.5.2 Electrode Section

Having loaded the device structure into Sentaurus Device, it is necessary to specify which of the contacts are to be treated as electrodes. Electrodes in Sentaurus Device are defined by electrical boundary conditions and contain no mesh. The Electrode section defines all the electrodes to be used in the Sentaurus Device simulation, with their respective boundary conditions and initial biases. Any contacts that are not defined as electrodes are ignored by Sentaurus Device. The polysilicon gate of a MOS

transistor can be treated in two ways:

1. As a metal, in which case, it is simply an electrode.

2. As a region of doped polysilicon, in which case, the gate electrode must be a contact on top of the polysilicon region.

```
Electrode{
{ Name="source" Voltage=0}
{ Name="drain" Voltage=0}
{ Name="gate" Voltage=0 workfunction=@phig_n@ schottky }
{ Name="substrate" Voltage=0 }
}
```

Each electrode is specified by a case-sensitive name that must match exactly an existing contact name in the structure file. Only those contacts that are named in the Electrode section are included in the simulation. Voltage=0, defines a voltage boundary condition with an initial value. One or more boundary conditions must be defined for each electrode, and any value given to a boundary condition applies in the initial solution. In this example, the simulation commences with a 100mV bias on the drain. As this is a NMESFET device the workfunction is related to Schottky contact.

5.5.3 Physics Section

The Physics section allows a selection of the physical models to be applied in the device simulation. In this example, it is sufficient to include basic mobility models and a definition of the band gap and, therefore, the intrinsic carrier concentration.

```
Physics {
    DefaultParametersFromFile
    Fermi
    Recombination (SRH Auger)
    Mobility(Phumob Enormal HighFieldSaturation)
    EffectiveIntrinsicDensity(BandgapNarrowing(delAlamo))
    eBarrierTunneling "NLM_gate"
    hBarrierTunneling "NLM_gate"
}
```

Mobility models including high-field saturation (velocity saturation), transverse field dependence are specified for this simulation. EffectiveIntrinsicDensity is the silicon bandgap narrowing model that determines the intrinsic carrier concentration.

5.5.4 Plot Section

The Plot section specifies all of the solution variables that are saved in the output plot files (.tdr). Only data that Sentaurus Device is able to compute, based on the selected physics models, is saved to a plot file.

```
Plot {
    eDensity hDensity
    eCurrent hCurrent Current
    ElectricField
```

```
    eQuasiFermi hQuasiFermi
    Potential Doping SpaceCharge
    SRH Auger Avalanche
    eMobility hMobility

    eBarrierTunneling
    hBarrierTunneling
    NonLocal
}
```

5.5.5 Math Section

Sentaurus Device solves the device equations (which are essentially a set of partial differential equations) self-consistently, on the discrete mesh, in an iterative fashion. For each iteration, an error is calculated and Sentaurus Device attempts to converge on a solution that has an acceptably small error. For this example, it is only necessary to define a few settings for the numeric solver.

```
Math{
    CNormPrint
    Iterations=20
    DirectCurrent
    ExitOnFailure
    -CheckUndefinedModels

    # nonlocal meshes for barrier tunneling:
    Nonlocal "NLM_gate" (Electrode="gate" Length=10e-7)
```

}

5.5.6 Solve Section

The Solve section defines a sequence of solutions to be obtained by the solver. The drain has a fixed initial bias of 100mV, and the source and substrate are at 0 V. To simulate the IdVg characteristic, it is necessary to ramp the gate bias from 0V to 2V, and obtain solutions at a number of points in-between. By default, the size of the step between solution points is determined by Sentaurus Device internally. As the simulation proceeds, output data for each of the electrodes (currents, voltages, and charges) is saved to the current file n1_des.plt after each step and, therefore, the electrical characteristic is obtained. This can be plotted using Inspect.

```
Solve {
  NewCurrentPrefix= "temp_"
  Coupled(iterations=1000) { Poisson }
  Quasistationary (
    doZero
    InitialStep= 0.1   MaxStep= 0.1 Minstep= 1e-4
    Goal { name="drain" Value= @Vd@ }
  ) {
    Coupled(Iterations= 20) {
      Poisson
      electron
      hole
    }
  }
  System("rm -f temp_*")
```

```
  NewCurrentPrefix="IdVg_"
  Quasistationary (
    doZero
    InitialStep= 0.05   MaxStep= 0.05 Minstep= 1e-4
    Goal { name="gate" Value= @Vgfinal@ }
  ) {
    Coupled(Iterations= 20) {
      Poisson
      electron
      hole
    }
  }
}
```

Poisson specifies that the initial solution is of the nonlinear Poisson equation only. Electrodes have initial electrical bias conditions as defined in the Electrode section. Coupled introduces the continuity equation for electrons, with the initial bias conditions applied. In this case, the electron current continuity equation is solved fully coupled to the Poisson equation, taking the solution from the previous step as the initial guess. The fully coupled or 'Newton' method is fast and converges in most cases. It is rarely necessary to use a 'Plugin' approach. The Quasistationary statement specifies that quasistatic or steady state 'equilibrium' solutions are to be obtained. A set of Goals for one or more electrodes is defined in parentheses. In this case, a sequence of solutions is obtained for increasing gate bias up to and including the goal of 2V. A fully coupled (Newton) method for the self-consistent solution of the Poisson and electron continuity equations is specified in braces. Each bias step is solved by taking the solution from the previous step as its initial guess.

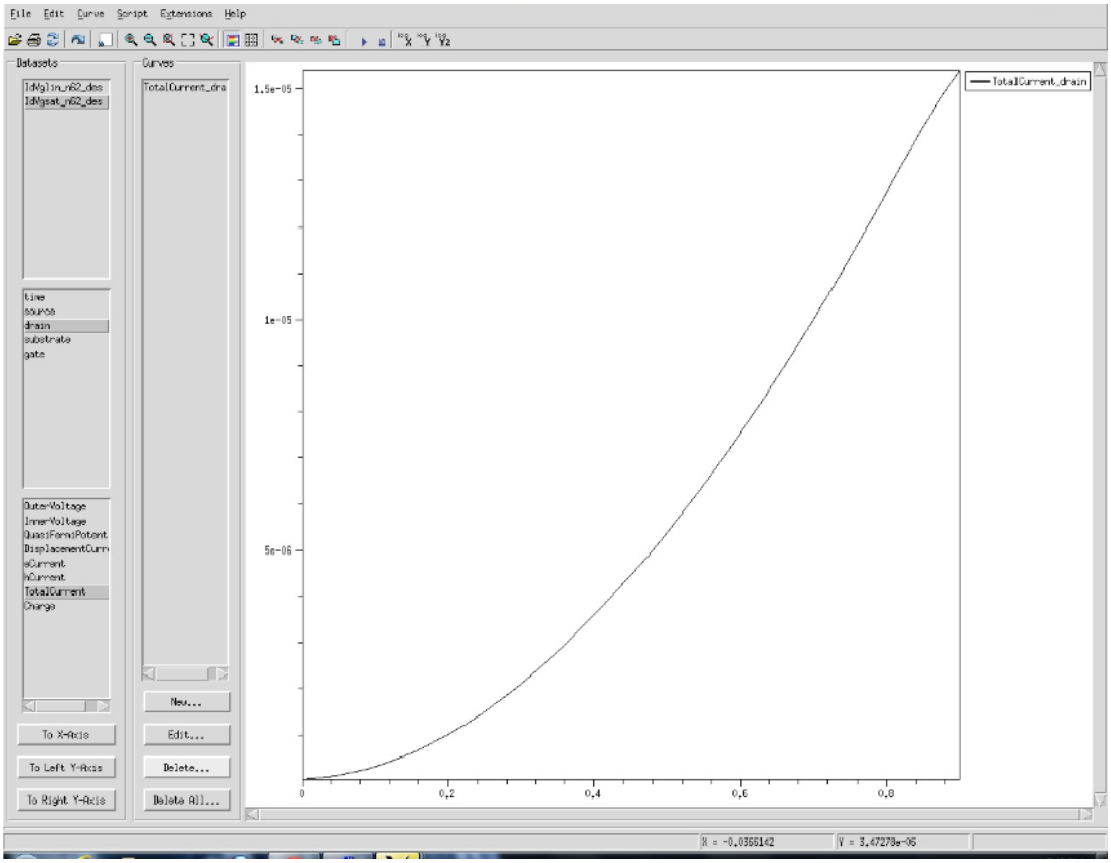


Figure 5.2 I_d-V_{gs} characteristic of 1µm n-channel MESFET

5.6 Mixed-mode simulation

The mixed-mode capability of Sentaurus Device allows for the simulation of a circuit that combines any number of Sentaurus Device devices of arbitrary dimensionality (1D, 2D, or 3D) with other devices based on compact models. In this paper, I presented a transient mixed-mode simulation with two 2D physical devices; an n-channel and a p-channel MESFET, combined with a voltage source to form CMES inverter circuit. Sentaurus Mesh is used to create 2D grids for the NMESFET and PMESFET devices. Sentaurus Device computes the transient response of the inverter to a voltage signal. The simulation results are plotted automatically using Inspect, driven by the command file, which is created by Sentaurus Workbench from the root command file.

CHAPTER 6

Numerical calculations, results and discussion

The result of the 2D-CMES device structure from sentauraus process simulator and the electrical properties of complementary MESFET from Sdevice simulator are compiled in this chapter. In Tecplot 360 tool from TCAD for observing initial doping concentration, channel implantation, n-well, p-well, source, drain and gate formation. In Inspect one can see I-V characteristics such as I_D-V_D and I_D-V_G graphs.

6.1 Doping profile

In S-process software, designer has two major doping methods like real clean room. One is the ion-implantation, another one is diffusion. In this paper, ion-implantation method has been used for forming channel, source and drain region. The full structure doping profile is shown in Figure 6.1. The source and drain as well as the active channel region are defined by ion implantation with ion dose of $1 \times 10^{14}\text{cm}^{-2}$ and dose of $1.4\times 10^{12}\text{cm}^{-2}$ respectively. The channel doping profile has been presented in Figure 6.1, and the doping profile of source and drain has been exhibited in Figure 6.1.

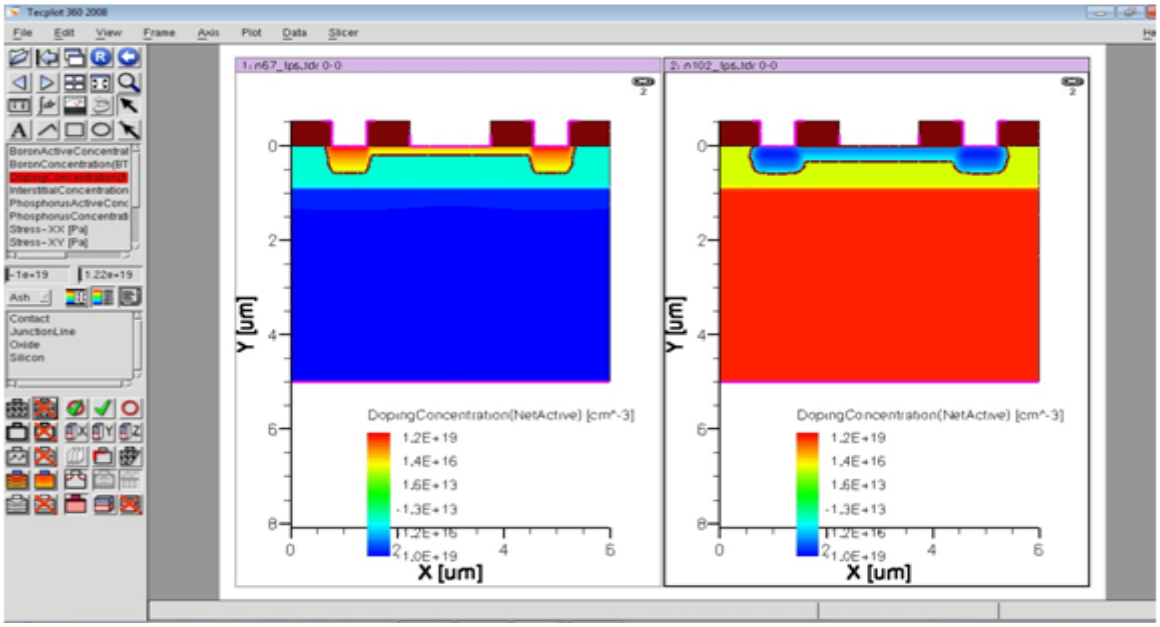


Figure 6.1 The doping profile for 1.5µm n-MESFET(left) and 1.5µm p-MESFET(right)

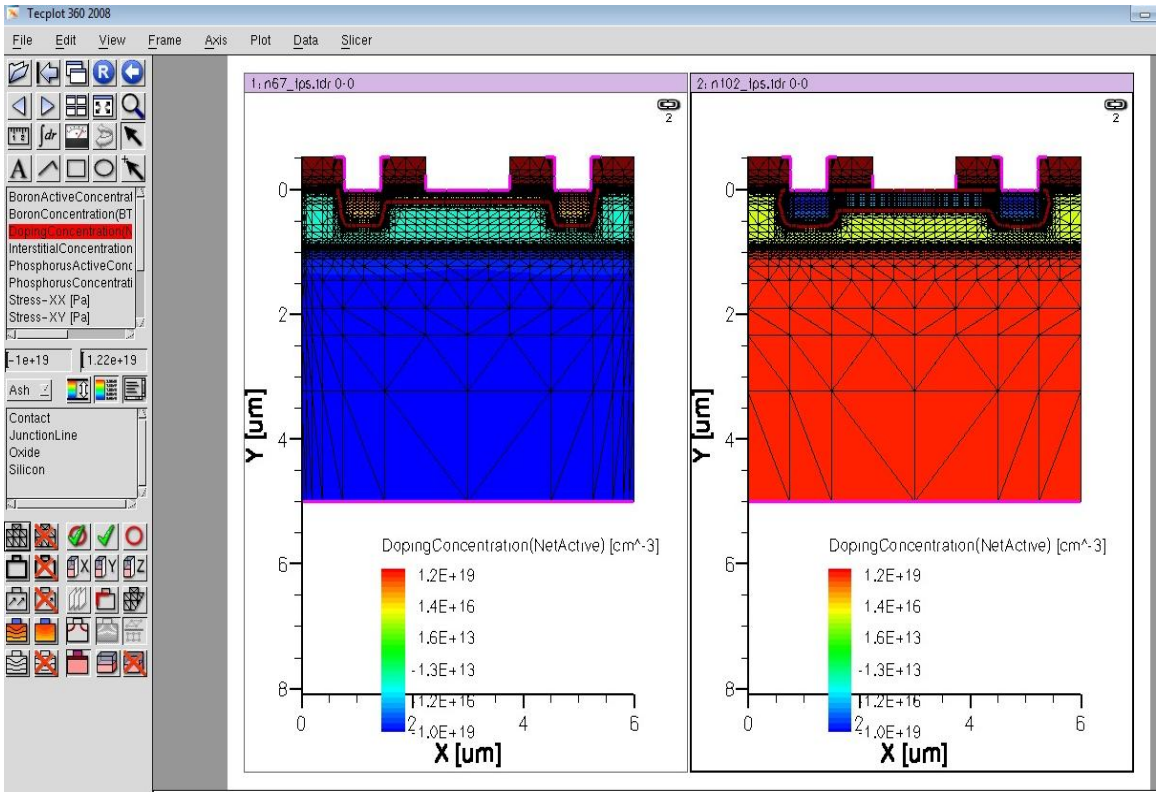


Figure 6.2 Meshing for 1.5µm n-MESFET(left) and 1.5µm p-MESFET(right)

Active area simulation:

Total number of nodes in active area = 43000

Total number of nodes outside active area = 2000

Initial doping concentration = 1×10^{19} cm^{-3}

Active doping concentration = $1.4\times 10^{12} cm^{-3}$

Source and Drain doping concentration = $1.0 \times 10^{14} cm^{-3}$

Run Time for Sprocess = 45 minutes

Tool Used: Sentaurus Sprocess, Tecplot 360

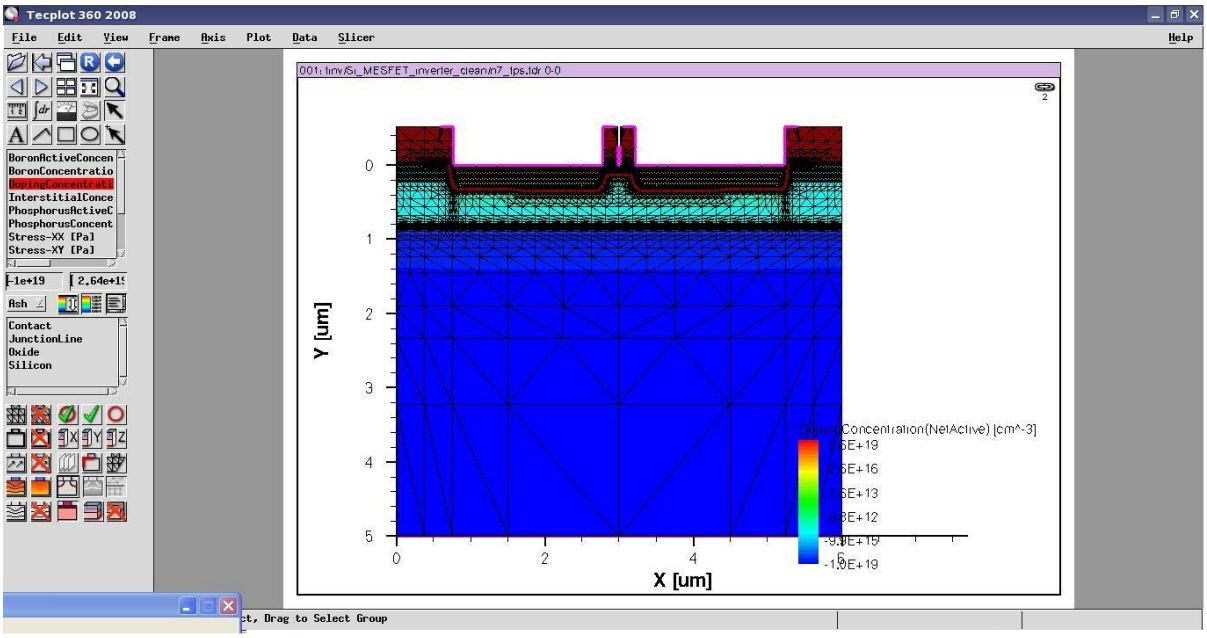


Figure 6.3 The doping profile for 30nm nMES

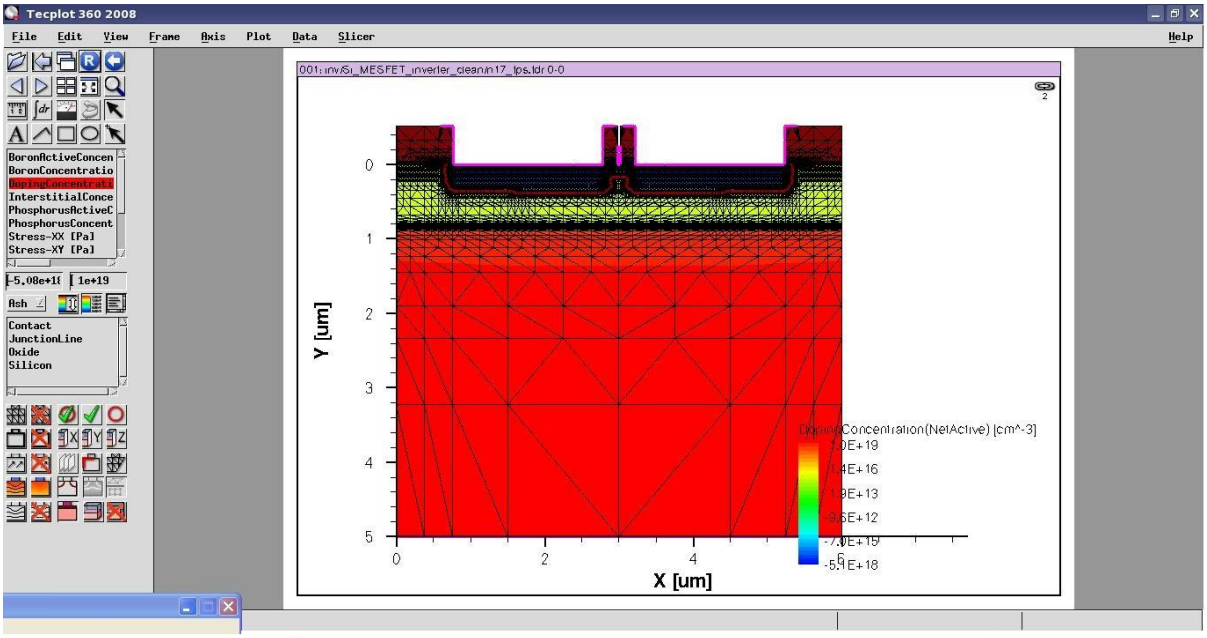


Figure 6.4 The doping profile for 30nm pMES

Active area simulation:

Total number of nodes in active area = 44500

Total number of nodes outside active area = 2000

Initial doping concentration = 1×10^{19} cm^{-3}

Active doping concentration = $1.0\times 10^{17} cm^{-3}$

Source and Drain doping concentration = $1.0 \times 10^{14} cm^{-3}$

Run Time for Sprocess = 50 minutes

Tool Used: Sentaurus Sprocess, Tecplot 360

In both devices with 1.5x10-4 cm and 30 nm gate length, all recombination effect such as Auger recombination, SRH recombination, non-ionized impurity effects, etc. has been incorporated in the simulation. The characteristics of drain current (I_D) versus gate voltage (V_G) and drain current versus drain voltage (V_{DS}) have been determined by the Synopsys Sentaurus TCAD and the results have been described in the next section.

6.2 Simulated Result of I_D-V_G Characteristics of NMES and PMES in CMES

I-V characteristic of CMES has been determined by using the SDevice software tool. In figure 6.5 and figure 6.6 shows the simulated plot of I_D-V_G graph of 1.5µm nMES and 30nm nMES respectively.

1. Simulated Result of I_D-V_G for nMES

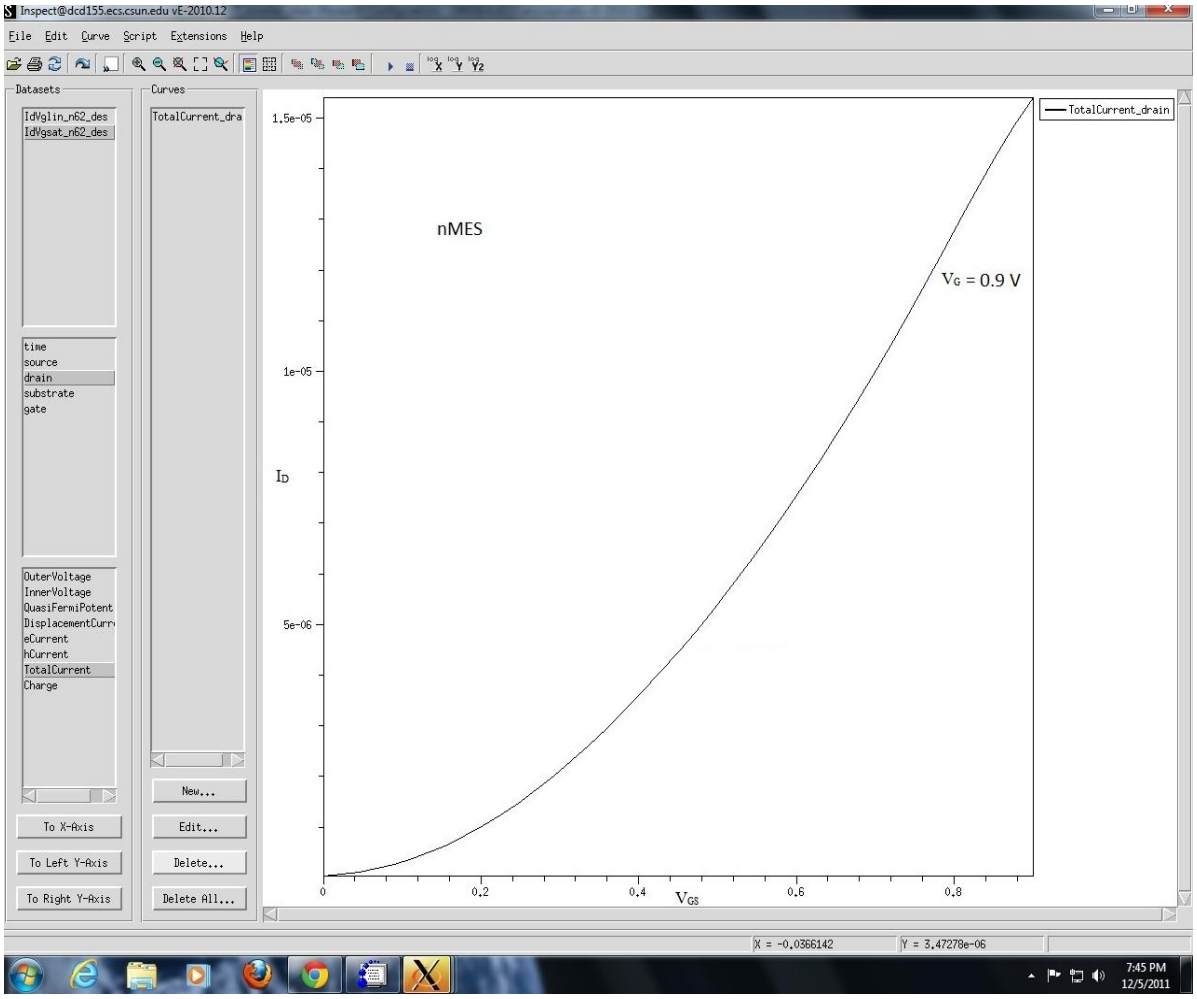


Figure 6.5 I_D (Y-axis) vs V_{GS} (X-axis) curve for 1.5µm nMES

The Figure 6.5 shows a simulated plot of drain current and gate voltage for the gate length of $1.5x10^{-4}$cm and the rest incorporated parameters have been described above. The transfer characteristics of drain current versus gate voltage show the increment of drain current with the increase of gate voltage. At low gate voltage in the range of 0 – 0.6V, the drain current exponentially increases with increment of gate voltage and this property shows clearly the indication of sub-threshold voltage. The threshold voltage obtained from the transfer

characteristics plot is approximately in the order of o.3V and the value has been found at the intersection of the plot with V_{GS} axis at drain current $I_{DS} = 0$

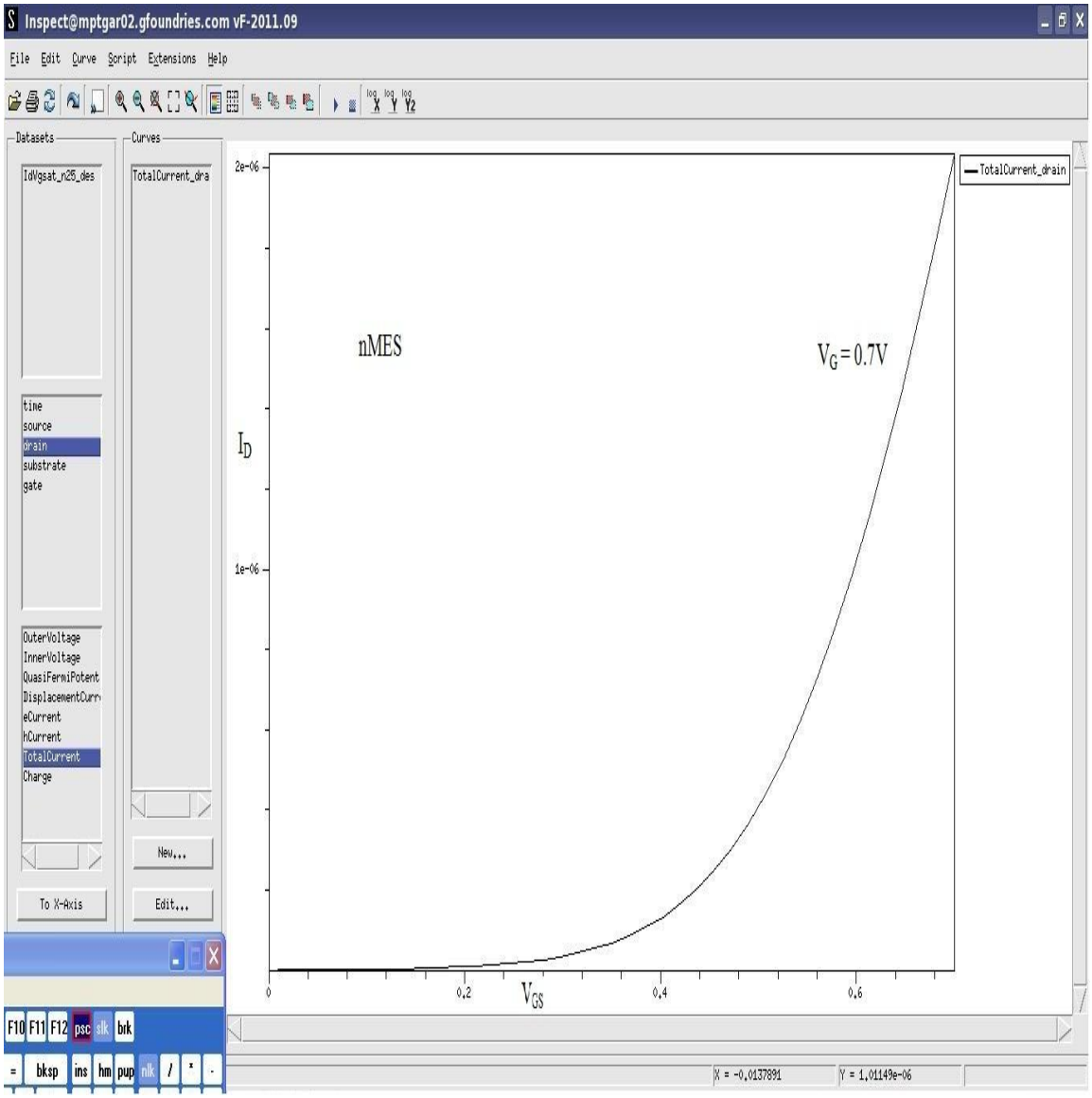


Figure 6.6 I_D (Y-axis) vs V_{GS} (X-axis) curve for 30nm nMES

The Figure 6.6 presents a simulated plot of drain current and gate voltage for the gate length of 30 nm. The transfer characteristics of drain current versus gate voltage show the increment of drain current with the increase of gate voltage. At low gate voltage in the range of 0 – 0.55V, the drain current exponentially increases with increment of gate voltage and this property shows clearly the indication of sub-threshold voltage. The nature of sub-threshold shows a extremely large exponential curve due to large amount of minority carriers. The threshold voltage obtained from the transfer characteristics plot is approximately in the order of 0.55V.

2. Simulated Result of I_D-V_G for pMES

I-V characteristic of CMES has been determined by using the SDevice software tool. The figure 6.7 and figure 6.8 shows the simulated plot of I_D-V_G graph of 1.5µm pMES and 30nm pMES respectively.

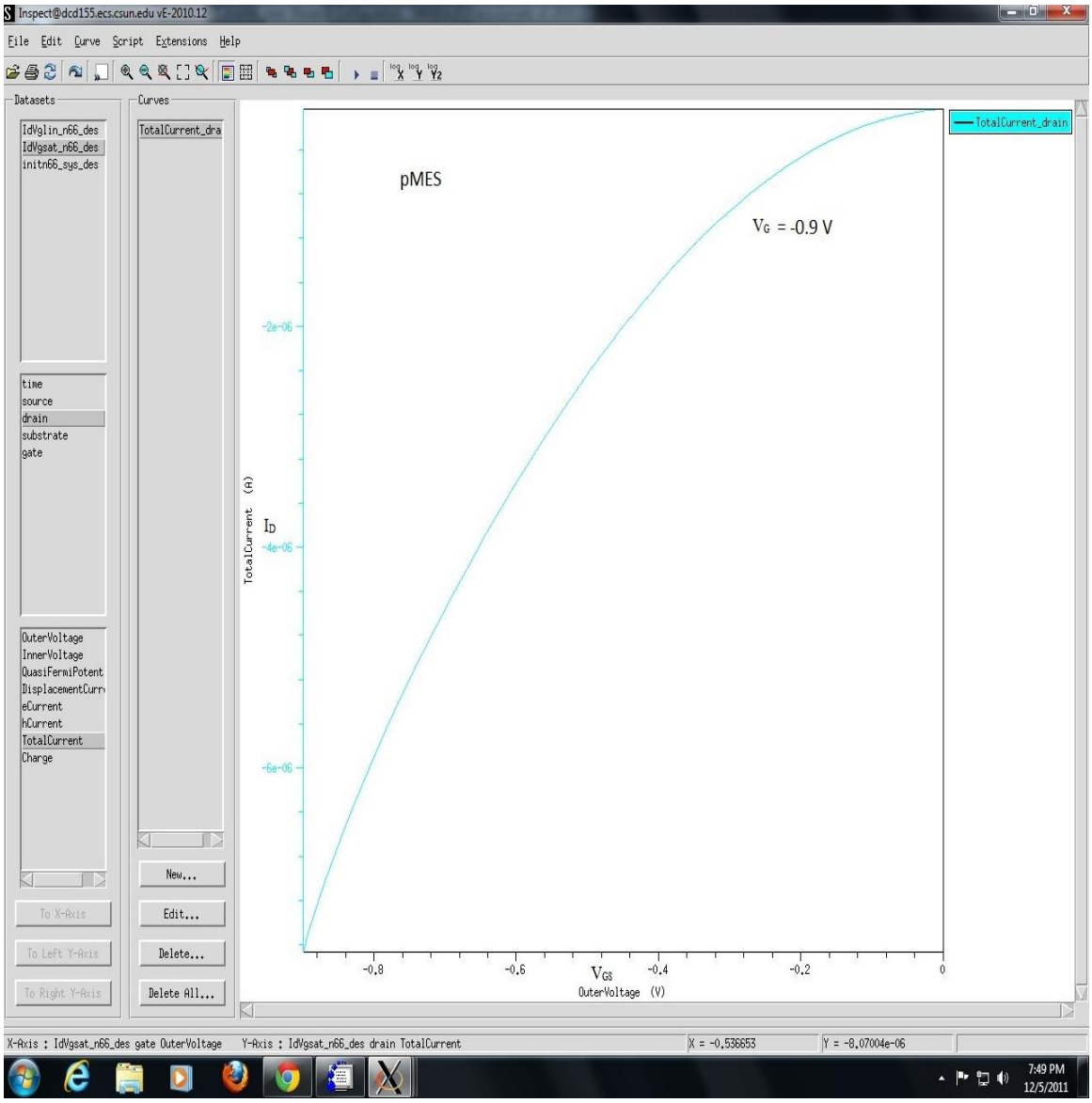


Figure 6.7 I_D (Y-axis) vs V_{GS} (X-axis) curve for 1.5µm pMES

The figure 6.7 shows the I-V characteristics of PMES with a gate length of $1.5x10^{-4}$ cm. The figure exhibits a plot of drain current I_D versus drain-source voltage for single gate-source voltage V_{GS} = 0.9V. The curve of the plot clearly shows the linear and non-linearity properties and the saturation current is found to be $1x10^{-6}$A.

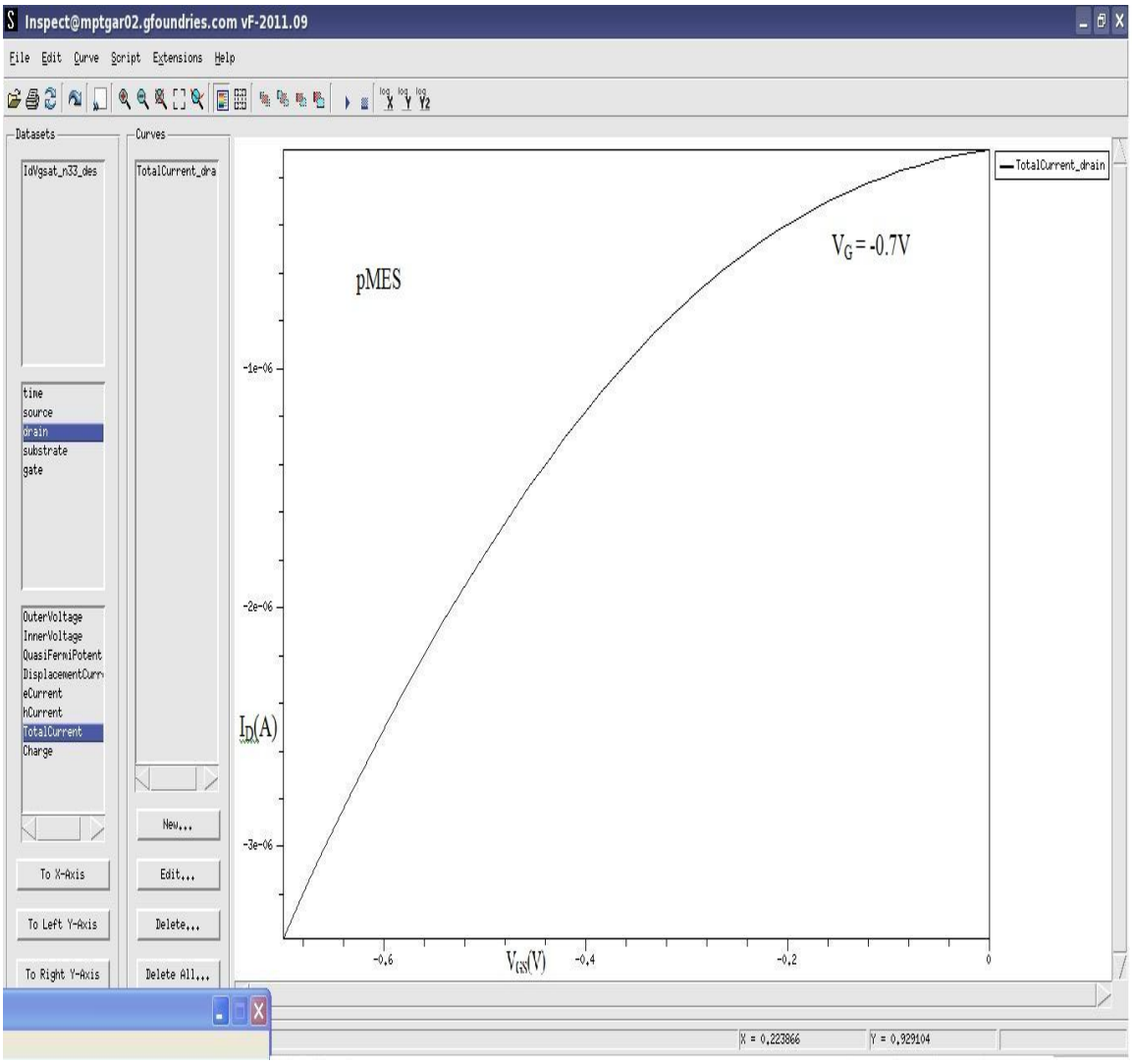


Figure 6.8 I_D (Y-axis) vs V_{GS} (X-axis) curve for 30nm pMES

The figure 6.8 demonstrates the I-V characteristics of PMES with a gate length of $1.5x10^{-4}$ nm. The figure exhibits a plot of drain current I_D versus drain-source voltage for single gate-source voltage V_{GS} = 0.9V. The curve of the plot clearly shows the linear and non-linearity properties and the current becomes saturated at the $I_D = 2x10^{-6}$A. The saturation current for the gate length of 30nm is almost doubles compared to gate length of $1.5x10^{-4}$cm because of the ratio device width and gate length. The plot of I-V characteristics of 30 nm gate length show same nature of I-V characteristics of large channel ($1.5x10^{-4}$cm) and no punch-through effect is observed because of artifact in the software program and improper device scaling.

6.3 Simulated Result of I_D-V_D Characteristics of NMES in CMES Device

1. Simulated Result of I_D-V_D for nMES

I-V characteristic of CMES has been determined by using the SDevice software tool. In figure 6.9 and figure 6.10 shows the simulated plot of I_D-V_D graph of 1.5µm nMES and 30nm nMES respectively.

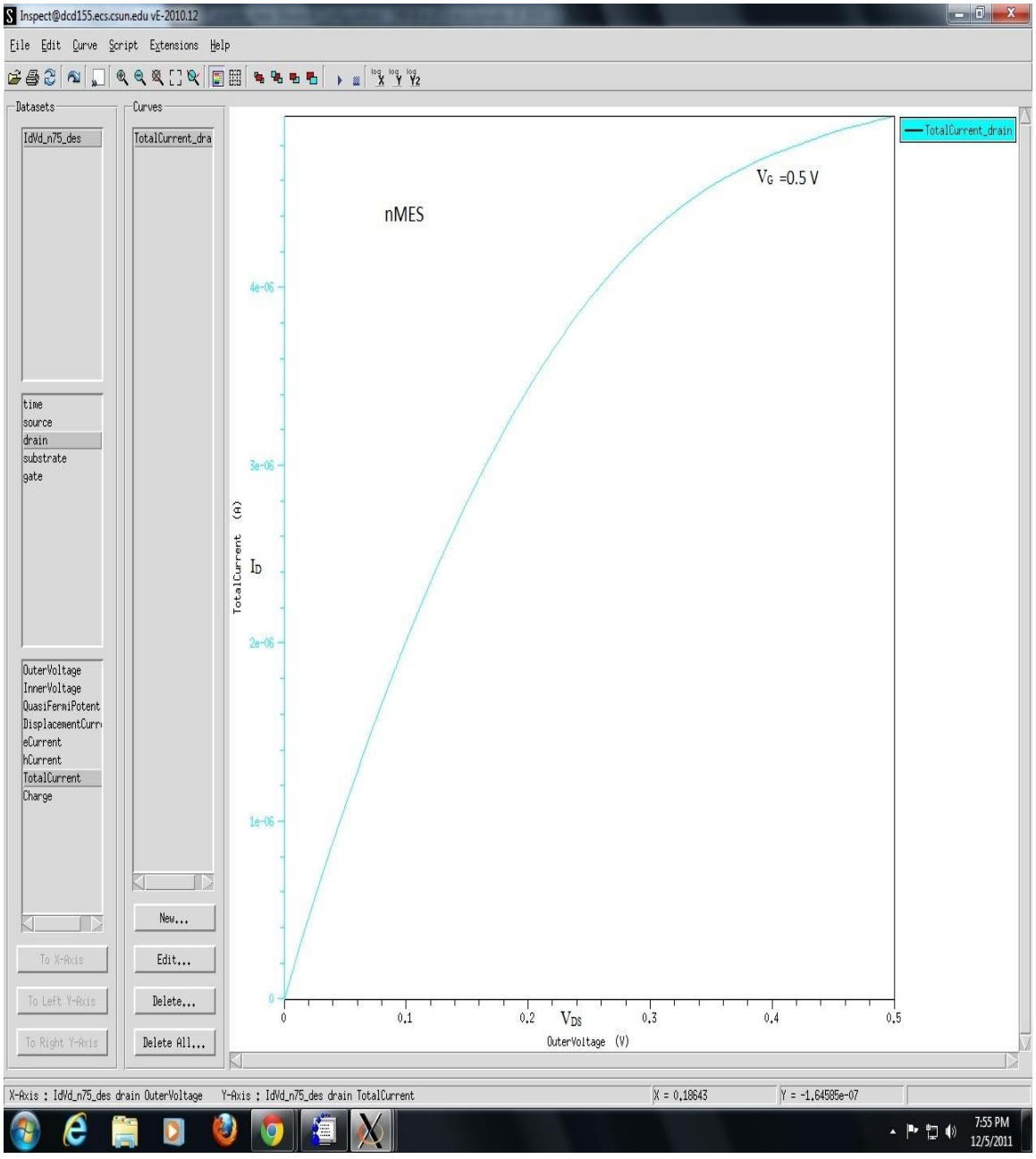


Figure 6.9 I_D (y-axis)-V_D (x-axis) curve for 1.5µm nMES

The figure 6.9 shows the I-V characteristics of NMES with a gate length of $1.5x10^{-4}$ cm. The figure exhibits a plot of drain current I_D versus drain-source voltage for single gate-source

voltage V_{GS} = 0.9V. The curve of the plot clearly shows the linear and non-linearity properties and the saturation current is obtained in order of $1x10^{-5}$A.

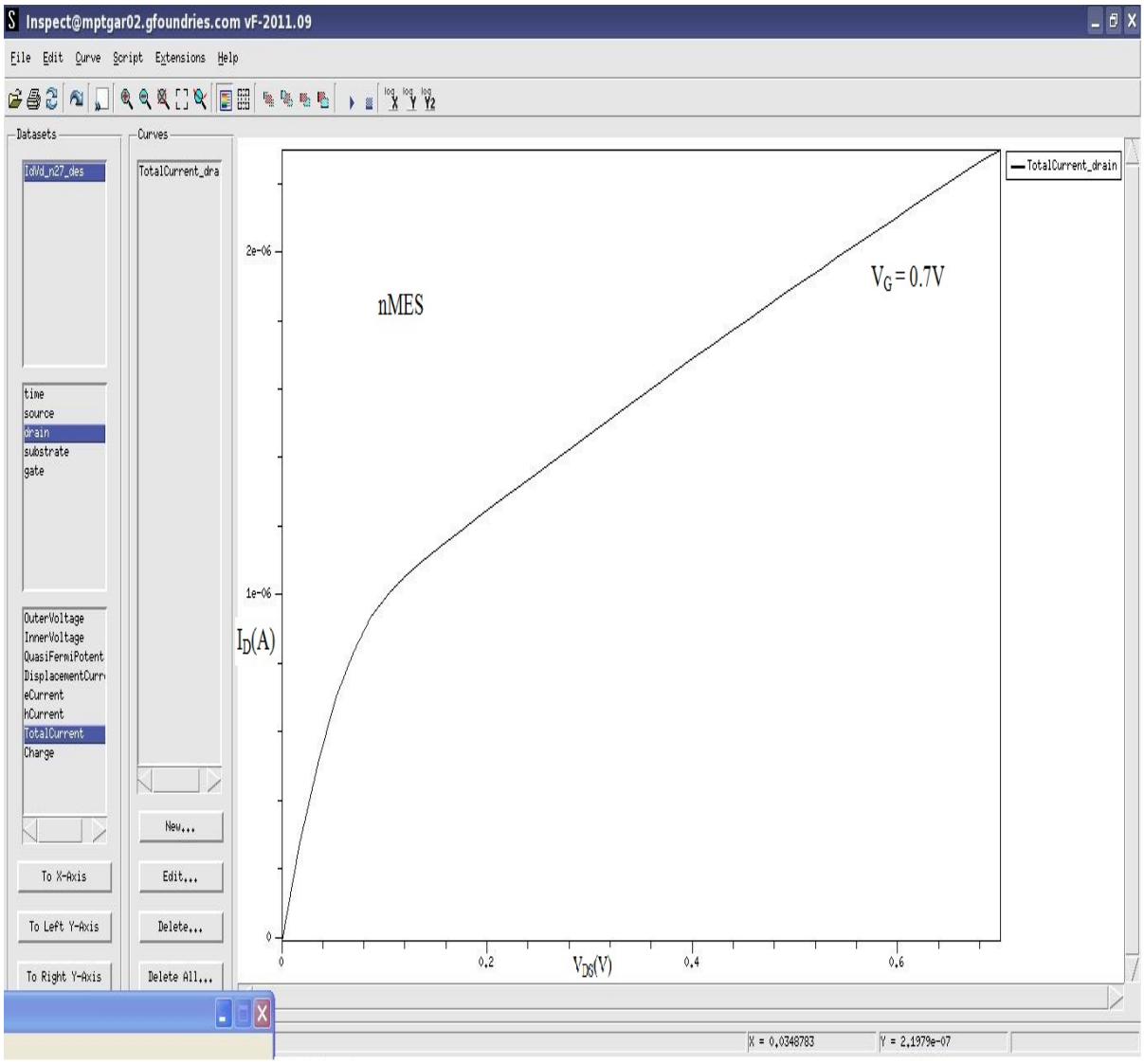


Figure 6.10 I_D (y-axis)-V_D (x-axis) curve for 30nm nMES

The figure 6.10 demonstrates the I-V characteristics of NMES with a gate length of 30 nm. The figure exhibits a plot of drain current I_D versus drain-source voltage for single gate-source voltage V_{GS} = 0.7V. The curve of the plot clearly shows the linear and non-linearity properties and the current becomes saturated at the I_D = $2.0x10^{-6}$A. The saturation current for the gate length of 30nm is almost doubles compared to gate length of $1.5x10^{-4}$cm because of the ratio device width and gate length. The plot of I-V characteristics of 30 nm gate length show the

saturation current in the order of $2.0x10^{-6}$A and the increment of drain current up to $2.2x10^{-6}$A shows an indication of punch-through effect on short-channel MOS which shows a similar plot obtained from punch-through characteristics of typical of short channel MOS devices [110].

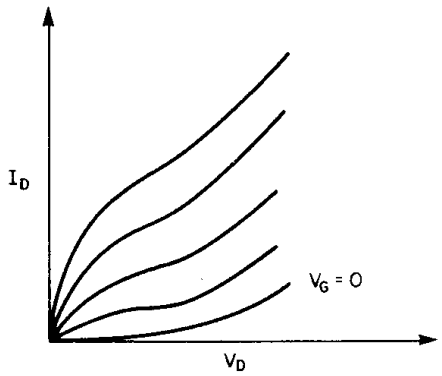


Figure 6.11 punch-through characteristics of typical of short channel MOS devices

The figure 6.11 shows the plot obtained from punch-through characteristics of typical of short channel MOS devices.

2. Simulated Result of I_D-V_D for pMES

I-V characteristic of CMES has been determined by using the SDevice software tool. In figure 6.12 and figure 6.13 shows the simulated plot of I_D-V_D graph of 1.5µm pMES and 30nm pMES respectively.

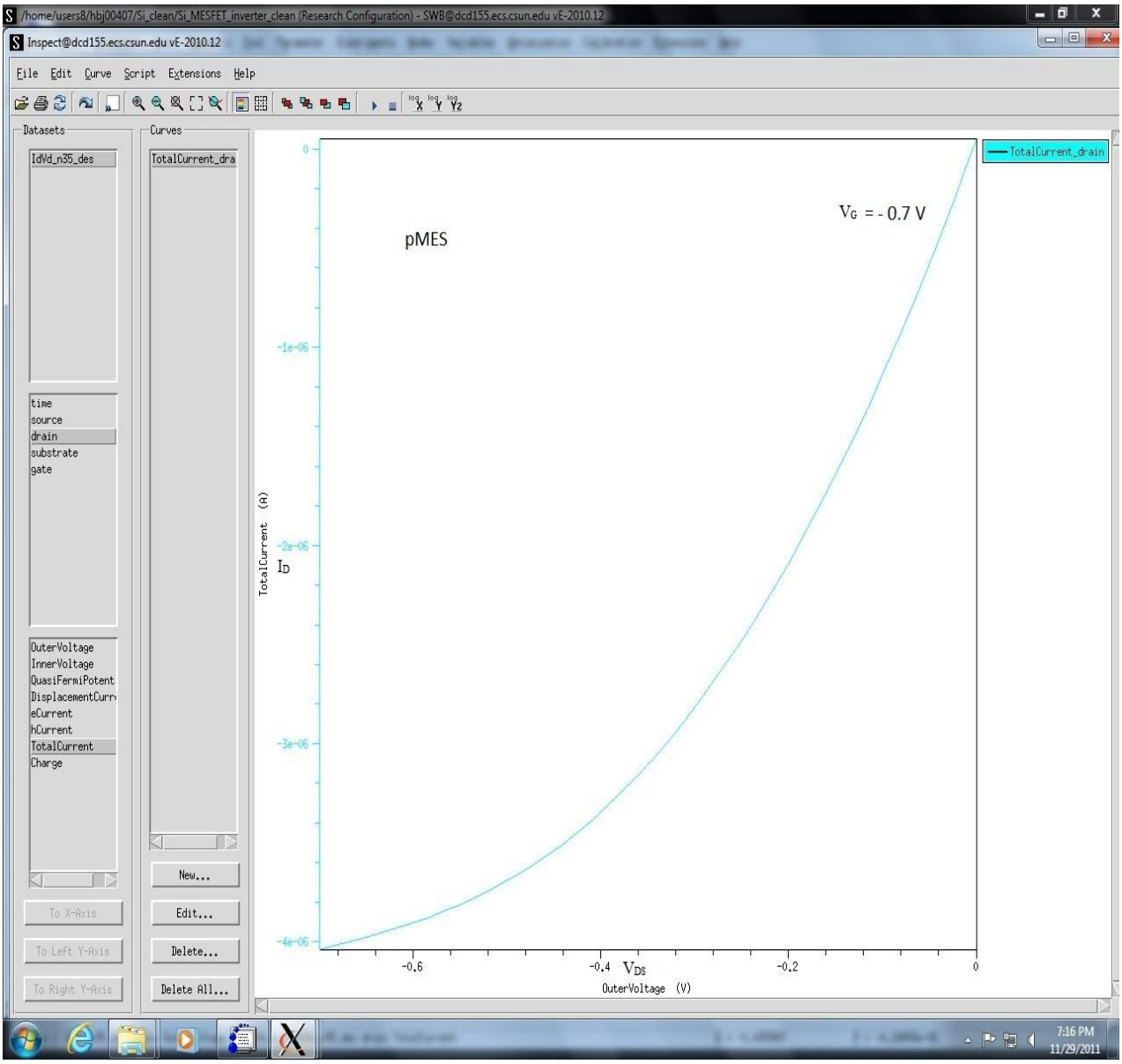


Figure 6.12 I_D (y-axis)-V_D (x-axis) curve for 1.5µm pMES

The figure 6.12 shows the I-V characteristics of PMES with a gate length of $1.5x10^{-4}$ cm. The figure exhibits a plot of drain current I_D versus drain-source voltage for single gate-source voltage V_{GS} = 0.7V. The curve of the plot clearly shows the linear and non-linearity properties and the saturation current is obtained in order of $-4x10^{-6}$A.

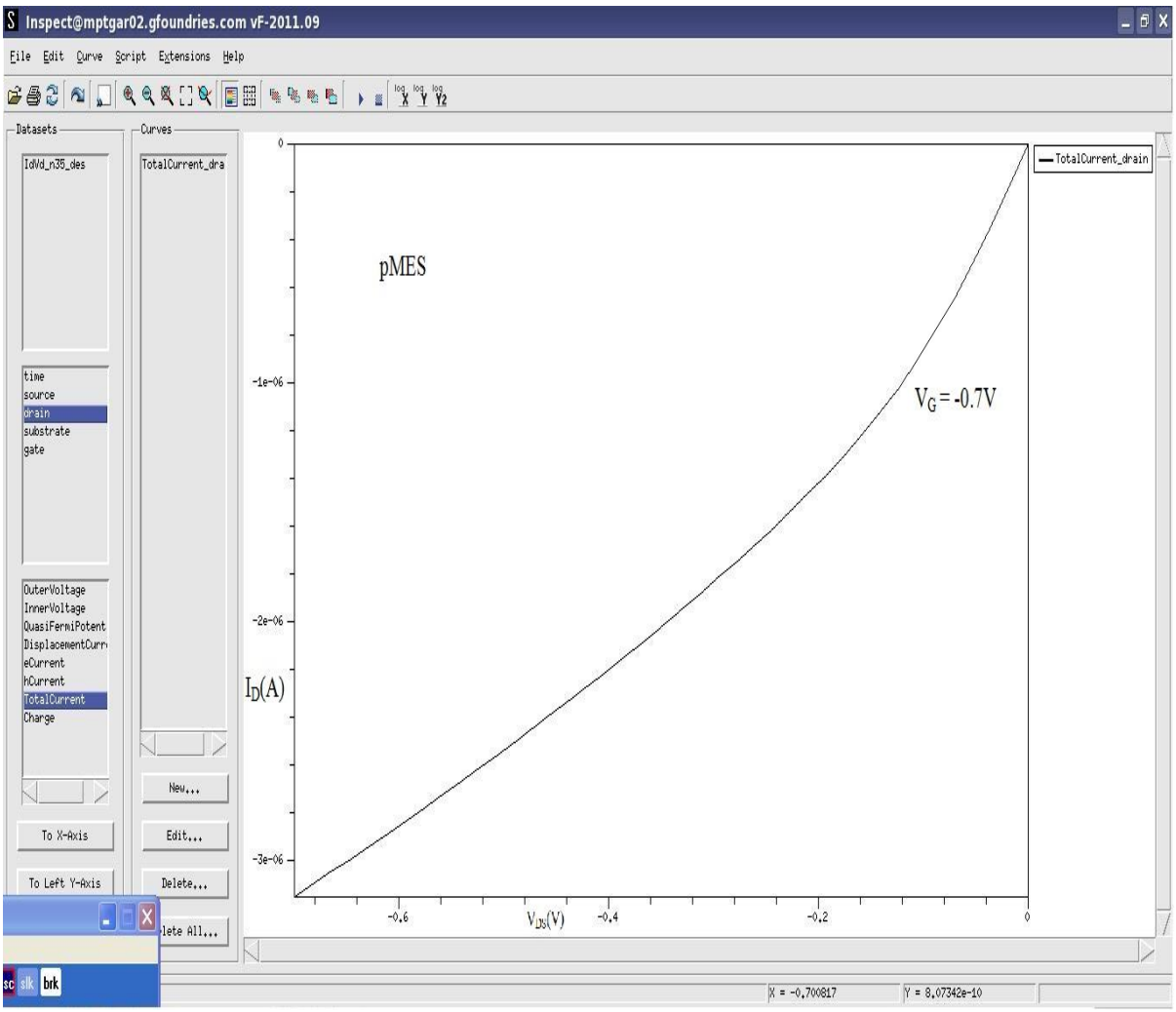


Figure 6.13 I_D (y-axis)-V_D (x-axis) curve for 30nm pMES

The figure 6.13 demonstrates the I-V characteristics of PMES with a gate length of 30 nm. The figure exhibits a plot of drain current I_D versus drain-source voltage for single gate-source voltage V_{GS} = 0.7V. The curve of the plot clearly shows the linear and non-linearity properties and the current becomes saturated at the I_D = -2.0x10^{-6}A. The saturation current for the gate length of 30nm is almost doubles compared to gate length of 1.5x10^{-4}cm because of the ratio device width and gate length. The plot of I-V characteristics of 30 nm gate length show the saturation current in the order of -2.0x10^{-6}A and the increment of drain current up to3.2x10^{-6}A shows an indication of punch-through effect on short-channel MOS which shows a similar plot obtained from punch-through characteristics of typical of short channel MOS devices.

6.4 Transient response

Transient response of CMES has been determined by using the SDevice software tool. In figure 6.14 and figure 6.15 shows the simulated plot of transient response of 1.5µm CMES and 30nm CMES respectively.

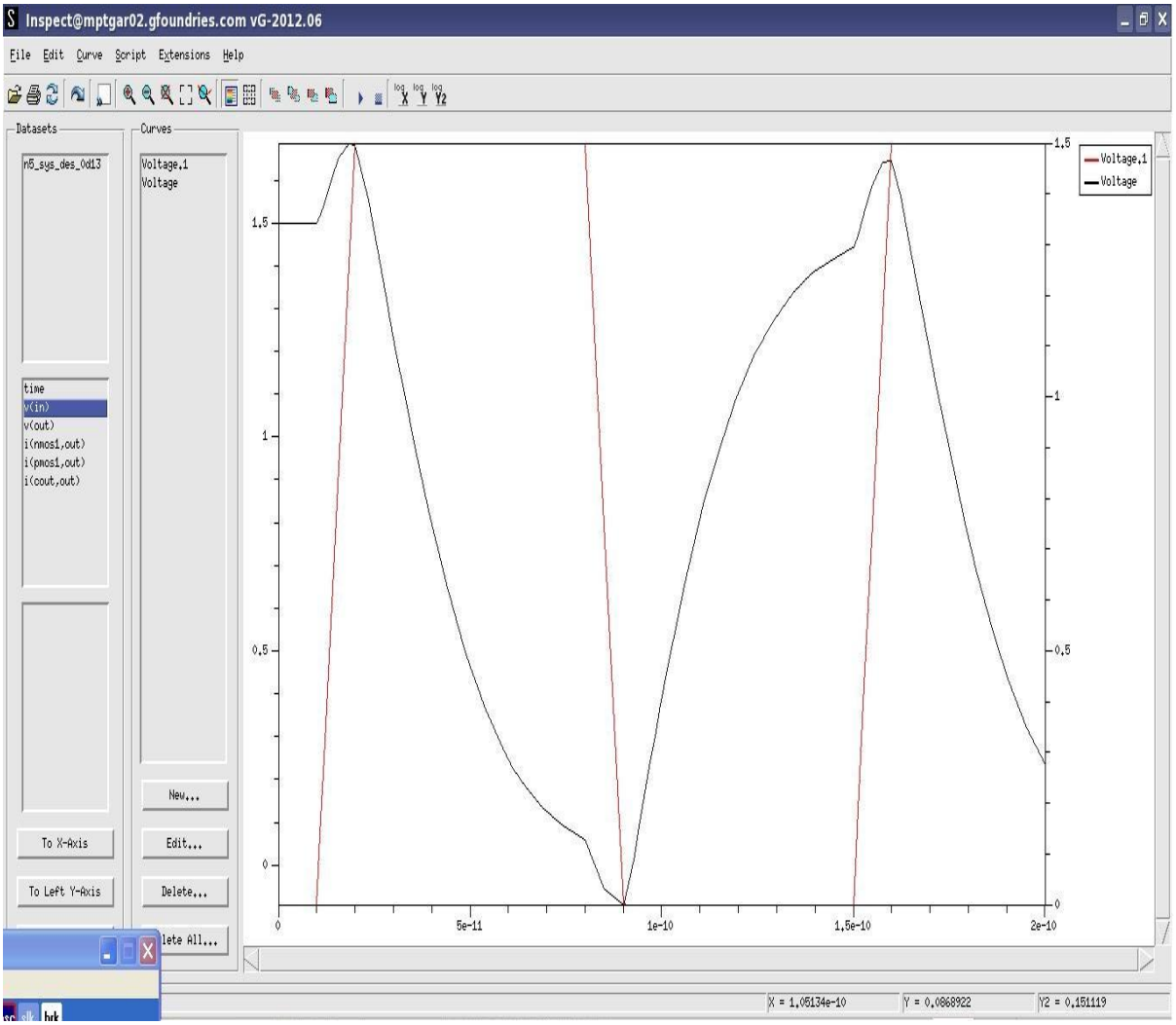


Figure 6.14 Transient Response for 1.5µm CMES

Figure 6.14 shows a transient response for 1.5µm gate lengths of NMOS and PMOS integrated in CMES device. The transient response shows the rise time in the order of 70ps and fall time in the order of 70ps.

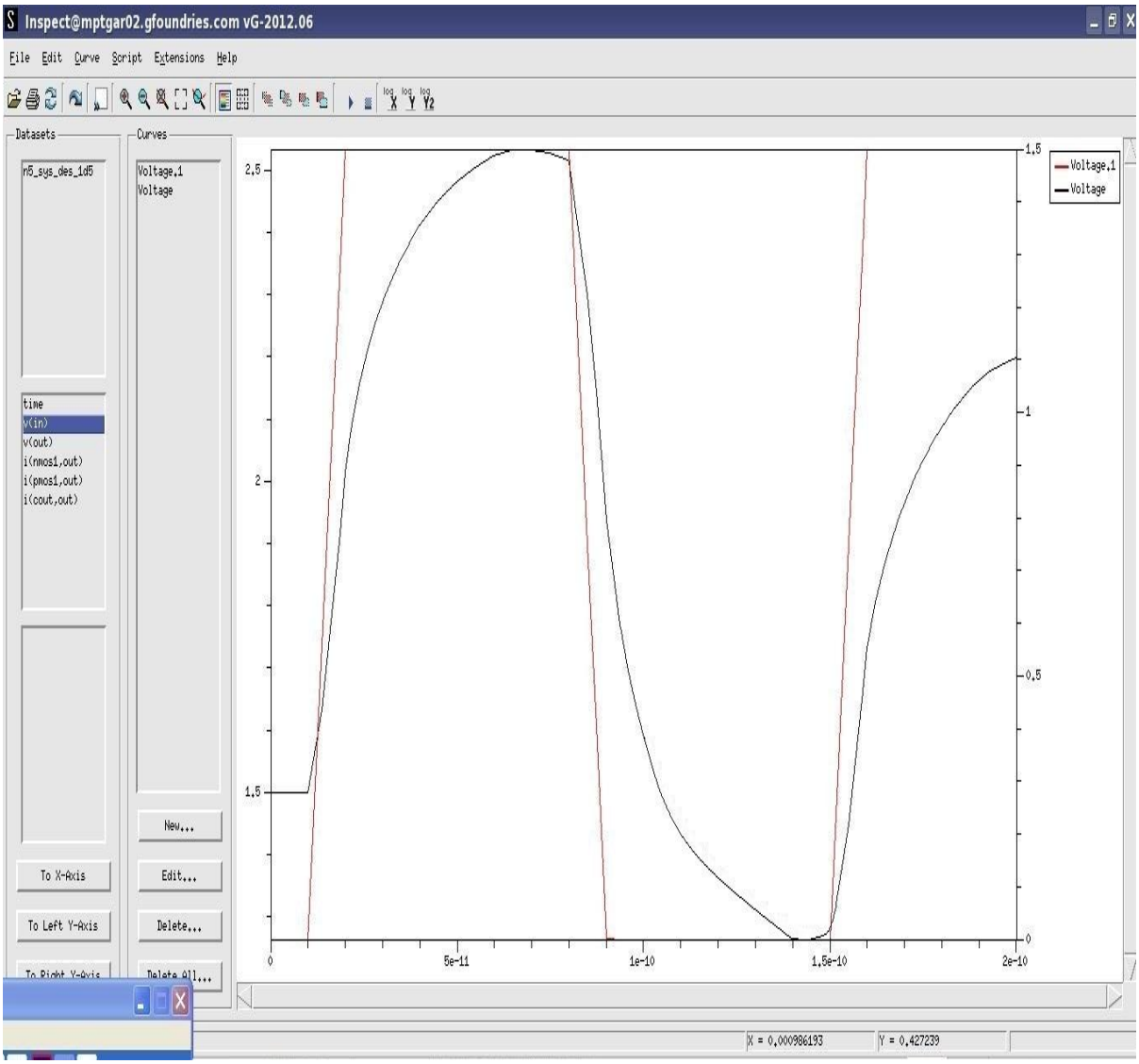


Figure 6.15 Transient response for 30nm CMES

Figure 6.15 shows a transient response for 30nm gate lengths of NMOS and PMOS integrated in CMES device. The transient response of 30nm CMES shows the rise time in the order of 60ps and fall time in the order of 60ps.The rise time and fall time can be achieved for shorter value. However, Figure 6.8 shows the I-V characteristics of 30nm pMES, where, the punch-through was not observed due to the artifact of the software or lack of proper device scaling. An attempt is going on to investigate the error.

CHAPTER 7

Conclusion

The development of complete complementary silicon MESFET has been presented. To reduce parasitic resistances, sidewall spacers are utilized. TCAD Sentaurus process simulator was extensively used for device structure development. The simulation of CMES device was accomplished through TCAD Sdevice simulator to extract the device physical and fabrication parameters and circuit parameters to achieve the best device performance. TCAD tool basically matches the physics phenomena in the device. Also, TCAD tools show an excellent ability for device structure to design in 3D. TCAD tools allow users to view the structure and electrical properties in free angle, which means that designer can modify the structure of device. Result shows better potential application of the CMES device compared to CMOS devices in terms the device speed obtained from the transient response for 1.5µm and 30nm gate length. In order to obtain the transient of physical dimension from 1.5µm and 30nm gate length, the CMES device was properly scaled down. The I-V characteristics of 30nm gate length shows an indication of the punch through effect due to the extremely low space separation between the source and drain region. The performance of CMES begins to look better device performance compared to other digital devices and hence this research claims a great prospect of future device revolutions.

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APPENDIX A

Notation and Symbols Used

K Bolzmann constant

T Absolute temperature at 300K

q Electronic charge. It is 1.6×10^{-19}

Z Device width.

L Channel length

N_A Substrate doping concentration.

N_D Channel doping concentration.

X_{dg} Distance from surface to edge of gate depletion region in the channel

X_{ds} Distance from surface to edge of gate depletion region in the channel.

X_P Distance from surface to channel potential minimum.

X_{PM} Maximum value of X_P above threshold.

X_w Distance from surface to edge of substrate depletion region in the bulk.

Q Ion implant dose.

R_P Ion implant range, it is a function of ion energy.

σ Ion implant straggle parameter in R_P idrection, it is a sub range paraper repest to R_P.

μ Carrier mobility in silicon carbide

ϵ Permittivity of Silicon Carbide

ϕ Electron potential in X direction.

ϕ_B Metal semiconductor work function difference.

Δ Depth of Fermi level below the conduction band in theundepleted channel.

V_{BS} Substrate to source voltage..

V_{DS} Drain to source voltage.

V_{GS} Gate to source voltage.

V_T Threshold voltage. When zero V_{DS} and gate voltage equal to V_T or smaller,

channel would depleted.

V_P Pinch off voltage. When zero V_{GS} and V_{DS} increase and large enough to deplete the channle.

V_{Dsat} saturation drain voltage.

V_{bi} Build in potential between channel and N epi layer.

V(y) Voltage of channel in y direction(Horizon direction, x means vertical direction).

C_{gs} Gate to source capacitance.

h Plank's contact.

m^* Effective mass of carrier.

gm Transconductance of MESFET.

APPENDIX B

Command File for Sentaurus Process Simulation

```
fset Type @Type@
math numThreads= 4
if { $Type== "nMES" } {
fset D1 Boron
fset D2 Phosphorus
} else {
fset D2 Boron
fset D1 Phosphorus
}
line y loc=3.0 spa=0.2 tag=left
line y loc=6.0 spa=0.2 tag=right
line x loc=1 spa=0.25 tag=top
line x loc=5 tag=bottom
# -- Silicon substrate definition
region Silicon xlo=top xhi=bottom ylo=left yhi=right
init concentration= 1e19 field= $D1   wafer.orient=100   slice.angle=[CutLine2D 0 0 1.0 0]
mgoals on normal.growth.ratio=1.1 min.normal.size= 3<nm> max.lateral.size=0.2<um>
if { $Type== "nMES" } {
deposit Silicon thickness= 1 fields= { Boron } values= { 1e15 }
} else {
deposit Silicon thickness= 1 fields= { Phosphorus } values= { 1e15 }
}
#Deposite Oxide Layer
deposit material = Oxide type = isotropic rate = {1.0} time=0.3
```

```
mask name=mask_1_2 segments = {-0.1 1.5 4.5 6.1 } negative
photo mask=mask_1_2 thickness=1
etch material = Oxide type= anisotropic rate= {10.0} time= 0.027
strip Photoresist
#split CH_IMPLANT
refinebox min= { -0.1 0.5 } max= { 0.7 1.5 } xrefine= 0.04 yrefine= 0.05
refinebox min= { -0.1 4.5 } max= { 0.7 5.5 } xrefine= 0.04 yrefine= 0.05
grid remesh
#Channel ion-implantation step
implant $D2 dose= @channel_dose@ energy= 35 tilt=7 rot=-90
temp_ramp name=tempramp_1_2 time=0.01 temp=800
diffuse temp_ramp=tempramp_1_2
etch material= Oxide type=anisotropic rate = {10.0} time=1.1
#Deposit another Oxide layer for source and drain ion-implantation window
deposit material= Oxide type= isotropic rate= {1.0} time=1
mask name=mask_1_3 segments = {-0.1 0.75 1.45 4.55 5.25 6.1 } negative
photo mask=mask_1_3 thickness=1
#Etch the Oxide for forming the ion implantation window of source and drain
etch material= Oxide type= anisotropic rate = {10.0} time=1.1
strip Photoresist
deposit material= Oxide type = isotropic rate= {1.0} time=0.02
#Do ion-plantation for forming source and drain well
implant $D2 dose= 1e14 energy= 55 tilt=0 rot=0
temp_ramp name=tempramp_1_3 time=0.01 temp=800
diffuse temp_ramp=tempramp_1_3
#split SD_CONTACTS
```

```
etch material= Oxide type=anisotropic rate = {0.5} time=1
deposit Aluminum isotropic thickness= 0.55 selective.materials= { Silicon }
mask name=mask_1_4 segments = {-0.1 2.25 3.75 6.1 } negative
photo mask=mask_1_4 thickness=1
etch material = Oxide type=anisotropic rate = {10.0} time=1.1
strip Photoresist
#Titanium is deposited on the surface of MESFET for schottky contact
deposit material= {Titanium} type = isotropic rate = {1.0} time=0.25
etch material= {Titanium} type= cmp coord= -0.25
strip Photoresist
# Remeshing for the device simulation
# clear the process simulation mesh
refinebox clear
refinebox !keep.lines
line clear
# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error       1e37
pdbSet Grid AdaptiveField Refine.Rel.Error       1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0
pdbSet Grid Adaptive 1
pdbSet Grid SnMesh DelaunayType boxmethod
refinebox name= Substrate \
refine.fields= { NetActive } def.max.asinhdiff= 1 \
   adaptive silicon add
refinebox name= Channel_Interface \
   min= "-0.1 3.0" \
```

```
    max= "0.7 5.5" \
    min.normal.size= 2e-3 normal.growth.ratio= 1.5 \
    interface.materials= {Silicon } all add
grid remesh
transform reflect left
contact name= source point x= -0.2 y= 1.0
contact name= drain point x= -0.2 y= 5.0
contact name= substrate bottom
contact name= gate point x= -0.1 y= 3.0
struct smesh= n@node@
```

APPENDIX C

Command File for Sentaurus Device Simulation

```
Electrode {
   { name="source" voltage=0 }
   { name="drain"   voltage=0 }
   { name="substrate"   voltage=0 }
   { name="gate"    voltage=0 workfunction=@phig@ schottky}
}
File {
  grid       = "n@node|sprocess@_fps.tdr"
  plot       = "@tdrdat@"
  output     = "@log@"
  current    = "@plot@"
  parameter = "@parameter@"
}
Physics {
    DefaultParametersFromFile
    Fermi
    Recombination (SRH Auger)
    Mobility(Phumob Enormal HighFieldSaturation)
    EffectiveIntrinsicDensity(BandgapNarrowing(delAlamo))
    eBarrierTunneling "NLM_gate"
    hBarrierTunneling "NLM_gate"
}
#include "traps_des.cmd"
Plot {
```

```
    eDensity hDensity
    eCurrent hCurrent Current
    ElectricField
    eQuasiFermi hQuasiFermi
    Potential Doping SpaceCharge
    SRH Auger Avalanche
    eMobility hMobility
    eBarrierTunneling
    hBarrierTunneling
    NonLocal
}
Math{
  CNormPrint
  Iterations=20
  DirectCurrent
  ExitOnFailure
  -CheckUndefinedModels
  # nonlocal meshes for barrier tunneling:
  Nonlocal "NLM_gate" (Electrode="gate" Length=10e-7)
}
```