Physics based analytical Modeling of Gallium Arsenide MESFET for Evaluation

Of Junction Capacitance with new modeling conception

A graduate project submitted in partial fulfillment of the requirements
for the degree of Masters of Science
in Electrical Engineering.

By

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ABSTRACT

Physics Based Analytical modeling of GaAs MESFET for evaluation

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In this project, an analytical modeling of Gallium Arsenide MESFET has been reported. The model has been developed to obtain the drain current versus drain-source voltage for different gate-source voltages and the response of I-V characteristics has been determined from intrinsic parameters such as gate capacitances including both of the gate-source capacitances and gate-drain capacitances with respect to various gate-source voltages and gate drain-voltages with a new modeling conception. The new conception provides increased accuracy over a wide range of silicon and gallium arsenide devices for microwave circuit design applications. In order to understand the device performance the device parameters such as the drain current and the variation of gate-source capacitance and gate drain capacitance for gate-source and source-drain biasing were studied and the result is obtained by using the MATLAB software.

CHAPTER 1

Introduction

In recent years, the GaAs MESFET has increasingly been adopted in large-signal microwave applications such as power amplifiers and oscillators. As is well known, an essential prerequisite for computer-aided design software to obtain a reliable design depends critically on an accurate large signal model for GaAs MESFET, especially its nonlinear behavior. Therefore, much work has been undertaken and varieties of analytical models have been developed to describe the operation characteristics of a GaAs MESFET. Among the field-effect transistor nonlinear characteristics, the most important ones are the drain–source performance and the nonlinear gate charge with respect to drain–source and gate–source voltages. It is worth noting that the accuracy of the charge model affects the simulation results for frequency-dependent characteristics such as - parameters, as well as nonlinear properties including distortion, harmonic analysis, and third-order inter modulation product, and adjacent channel power ratio. Therefore, there is a need for an accurate GaAs MESFET charge model for the design of microwave nonlinear circuits, especially power amplifiers [1].

In order to design, develop, and produce high-yield low-cost microwave circuits, adequate models of all components are required. One of the first models used for nonlinear GaAs MESFET's was proposed by Curt-ice. The capacitance–voltage relations were, to a first degree of approximation, assumed to be independent of the current–voltage relation, and were modeled by a simple diffusion capacitance. Later, Statz proposed modified equations resulting in a more accurate prediction of measured S-parameters, valid in a broader area of MESFET operation. These equations also conserve charge at the device terminals. Even now, a lot of work is still done on nonlinear capacitance MESFET modeling. Performing accurate circuit simulations not only requires accurate device models, but also accurate extraction of all model parameters [2].

The surface of the device has been recognized as a major source of many detrimental effects on the performance of GaAs MESFET. Various theoretical studies over the years have led to the conclusion that the surface played a significant role in the device characteristics particular, the breakdown voltage and instability in the current voltage family of curves are two surface related parameters that directly affect the power performance of a device. In recent years, the surface of the device in the vicinity of the gate has been indirectly addressed by the advent of the low-temperature gown passive and overlapping-gate technology .Devices which utilized this technology have demonstrated dramatic improvement in the gate-drain breakdown voltage, which in turn drastically enhanced the power output by the devices [3].

Gallium arsenide devices have been widely used since the late 1960s for microwave applications, and they are still dominating this field. The use of GaAs for digital circuit applications began in the early 1970s, and it has developed over the years into a well-established LSI technology, with an increasing number of VLSI applications in recent years. Two examples of this are the GaAs supercomputer CRAY-3 under development at Cray Research [4]. Manufacturers of existing, silicon-based computer architectures are also starting to replace critical ICs like cache memories and disc controllers with plug-in compatible GaAs circuits in order to increase performance.

Silicon technology is still 2 - 4 times more Cheaper than GaAs technology, depending on the complexity of the process in consideration, but its usage is tested in applications that require very high speed and low power consumption. With the increasing volume of portable electronic equipment, from phones to computers, the GaAs logic families are becoming attractive for system designers because their low power dissipation property.

The accurate models for the device active and passive circuit elements are required for the design of the high speed gallium arsenide digital integrated circuits. The modeling area has increased considerably with the use of gallium arsenide integrated circuits, but the models using gallium arsenide still have a long difference to cover to reach the accuracy of the existing silicon mosfet models. The lack of inadequate and non proprietary models used for circuit simulation is restricting the use of gallium arsenide technology.

In recent years, however, a large number of GaAs MESFET models have been proposed, and some have been implemented in SPICE with far better results than the old, inadequate models. As the model complexity increases, however, it gets more difficult to extract the model parameters from measurement data, and it becomes necessary to resort to nonlinear optimization techniques. A lot of work has been undertaken and varieties of analytical models have been developed to describe the operation characteristics of a GaAs MESFET. Among the field-effect transistor FET's nonlinear characteristics, the most important ones are the drain–source performance and the nonlinear gate charge with respect to drain–source and gate–source voltages. It is worth noting that the accuracy of the charge model affects the simulation results for frequency-dependent characteristics such as -parameters, as well as nonlinear properties including distortion, harmonic analysis, and third-order inter modulation product, and adjacent channel power ratio [5].

There are different ways of modeling MESFET gate charge capacitances such as physical models [6-8], table-based models [9, 10], and empirical models. Among these three, the empirical model is the most commonly used approach in GaAs MESFET nonlinear modeling, which uses analytical functions to describe bias dependence of the capacitances. The existing empirical MESFET charge models can be classified into two groups. In the first group, analytical equations are found to fit and separately while the terminal charge conservation is not considered. These models may be difficult to implement in circuit simulators whose capacitance is always the derivative of an internal state variable. In addition, the simulation may have convergence problems as charge conservation is not maintained. In the second group, analytical equations are proposed for terminal charge, and the capacitor values are derived from the partial derivatives of charge with respect to the appropriate voltages. These models are capable of accurately describing capacitance performance in some device operation regions. However, normally the inaccuracy is still most significant in the linear region, saturation knee region, and sub threshold region [11].

Simulation of nonlinear microwave circuits utilizing GaAs MESFET devices reveals the circuit simulation accuracy from an ac point of view to be quite sensitive to the precision by which the gate-source and gate-drain capacitances of the device are modeled as a

function of voltage [12] has been discussed with emphasis on the Statz approach. Inaccuracies from this viewpoint restrict the bias area over which the accuracy of the overall model remains high from a microwave point of view.

The MESFET is a three terminal device just like any other transistor as shown in figure 1. The terminals are named as source, gate and drain. Charge carriers flow from the source to the drain via a channel. The channel is defined by doping the epitaxial layer grown on semiconductor and offers good conduction. The flow of charge carriers in the channel is controlled by a Schottky barrier gate. The main advantages of a MESFET compared to its counter parts are high electron velocity inside the channel; smaller transit time leading to faster response and fabrication of active layer on semi-insulating GaAs substrates to decrease the parasitic capacitances[13].
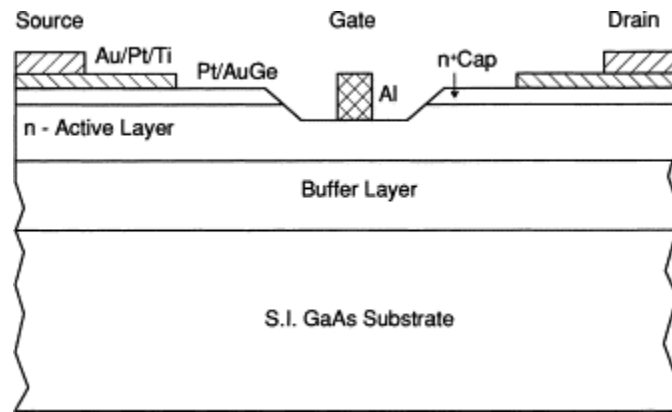
Figure 1 Schematic cross-section diagram of the GaAs MESFET.

A number of different GaAs FET models exist, and each of them can be classified among several different categories. When models are classified according to how they are derived, they can be grouped into physically based model, empirical model and experimental model. When FET models are classified according to the type of performance predicted by them, they can be grouped into small-signal model, large signal model [14].

When designing high-performance digital and analog circuits with modern technologies such as GaAs D- and E/DMESFET technology, it is of utmost importance to get reliable simulation data of the circuits in question. Today, the device models or the input

parameters used for these models often do not meet these requirements. Most of the GaAs MESFET models currently in use for circuit simulation are more or less nonphysical curve fitting models, which complicates the task of extracting simulation parameters from the measurement data.

The empirical model can be easily implemented into circuit simulators. Thus, they are most widely used by circuit designers and in device libraries. Both small-signal and large-signal models are important for nonlinear MESFET modeling. As mentioned earlier, power amplifiers are the main applications of GaAs MESFETs. MESFET devices exhibit nonlinear behavior in power amplifiers. Thus, accurate large signal MESFET models are particularly critical for the performance prediction of nonlinear microwave circuits. Although much work has been done in large signal modeling of GaAs MESFET, accurate linear and nonlinear models are still in great demand [15].

CHAPTER 2

Chemistry of Gallium Arsenide Material and devices

2.1 Nature and Properties of gallium arsenide material

Gallium arsenide (GaAs) is a compound of the elements gallium and arsenic. It is grey, cubic crystals with a melting-point of 1238 °C, density: 5.3176 g/cm3. It is insoluble in water slightly soluble in 0.1 M phosphate buffer at pH 7. Gallium arsenide decomposes with evolution of arsenic vapor at temperatures above 480 °C and reacts with strong acid reducing agents to produce arsine gas [16]. GaAs is a III–V compound semiconductor composed of the element gallium (Ga) from column III and the element arsenic (As) from column V of the periodic table of the Elements. GaAs was first created by Goldschmidt and reported in 1929, but the first reported electronic properties of III–V compounds as semiconductors did not appear until 1952 [17]. The GaAs crystal is composed of two sub lattices, each face centered cubic (FCC) and offset with respect to each other by half the diagonal of the fcc cube. This crystal configuration is known as cubic or zinc blended. Figure 2 shows a unit cube for GaAs and Table-1 provides a listing of some of the general material characteristics and properties.
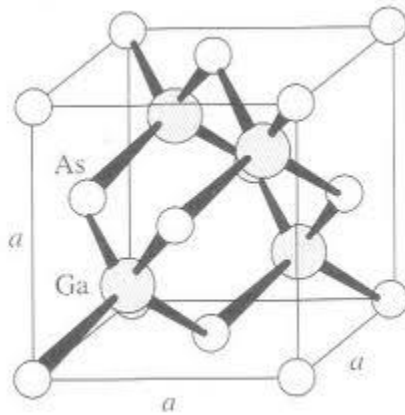

Figure 2 Gallium Arsenide Crystal Lattice

Property	Parameter
Crystal structure	Zinc blende
Lattice constant	5.65 Å
Density	5.32 g/cm^3
Atomic density	4.5×10^{22} atoms/cm^3
Molecular weight	144.64
Bulk modulus	7.55×10^{11} dyn/cm^2
Sheer modulus	3.26×10^{11} dyn/cm^2
Coefficient of thermal expansion	5.8×10^{-6} K^{-1}
Specific heat	0.327 J/g-K
Lattice thermal conductivity	0.55 W/cm-°C
Dielectric constant	12.85
Band gap	1.42 eV
Threshold field	3.3 kV/cm
Peak drift velocity	2.1×10^7 cm/s
Electron mobility (undoped)	8500 cm^2/V-s
Hole mobility (undoped)	400 cm^2/V-s
Melting point	1238°C

Table-1 Room temperature properties of GaAs.

2.2 Structural properties

One of the important characteristics that are attributed to GaAs is its superior electron mobility brought about as the result of its energy band structure as shown in the figure 3 below. Gallium Arsenide (GaAs) is a direct gap material with a maximum valence band and a minimum conduction band and is supposed to coincide in k-space at the Brillion zone centers. In the graph shown below, we can see that the some valleys in the band structure are narrow and some are sharply curved. These curves and narrows differ corresponding to the electrons with low effective mass state, while valleys that are wide with gentle curvature are characterized by larger effective masses. The curvature that is seen in the figure 3 of the energy versus electron momentum profile clearly shows the

effective mass of electrons travelling through the crystal. The minimum point of gallium arsenide's conduction band is near the zero point of crystal-lattice momentum, as opposed to silicon, where conduction band minimum occurs at high momentum. Now, mobility, μ, depends upon Concentration of impurity N, Temperature T, and is also inversely related to the electron effective mass, m [18].

Energy band structure of silicon and gallium arsenide
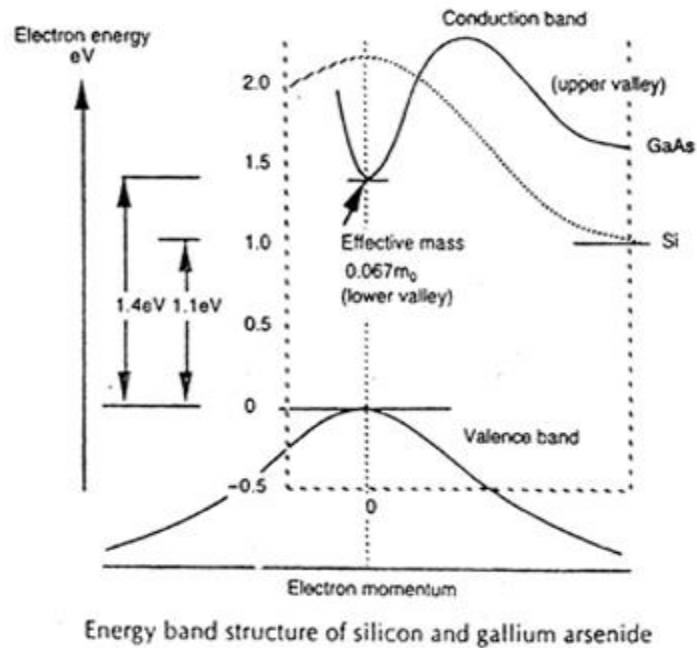
Figure 3 Energy band diagrams of gallium Arsenide and Silicon

GaAs is a direct band gap semiconductor, which means that the minimum of the conduction band is directly over the maximum of the valance band. Transitions between the valance band and the conduction band require only a change in energy, and no change in momentum, unlike indirect band-gap semiconductors such as silicon (Si). This property makes GaAs a very useful material for the manufacture of light emitting diodes and semiconductor lasers, since a photon is emitted when an electron changes energy levels from the conduction band to the valance band. Alternatively, an incident photon can excite an electron from the valence band to the conduction band, allowing GaAs to be used in photo detectors [19].

2.3   Mobility and drift velocity

GaAs has several advantages over silicon for operation in the microwave region-primarily, higher mobility and saturated drift velocity and the capability to produce devices on a semi-insulating substrate. In a semiconductor, when a carrier (an electron) is subjected to an electric field, it will experience a force (F = −qE) and will be accelerated along the field. During the time between collisions with other carrier ions and the semiconductor lattice, the carrier will achieve a velocity that is a function of the electric field strength. This velocity is defined as the drift velocity (v).   The variations for different semiconductors is shown in figure 4
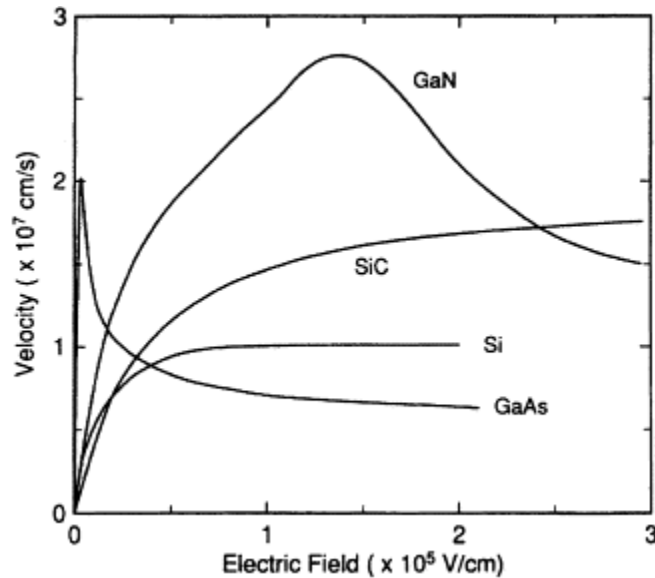
Figure 4 Drift velocity of electrons in GaAs, Si, SiC and GaN as a function of electric field

From the conservation of momentum, it can be shown that the drift velocity (*v*) is proportional to the applied electric field Figure 4 and can be expressed as

$$V = \frac{-(q\tau)E}{m*} \qquad (1)$$

The proportionality factor depends on the mean free time between collisions (t*c*) and the electron effective mass (m*). The proportionality factor is called the electron mobility (m) in units of cm2/V-s.

Mobility is an important parameter for carrier transport because it describes how strongly the motion of an electron is influenced by an applied electric field. From the equation above, it is evident that mobility is related directly to the mean free time between collisions, which in turn is determined primarily by lattice scattering and impurity scattering. The lattice scattering increases with temperature and becomes dominant at high temperatures and lattice scattering is a result of thermal vibrations of the lattice. Therefore, the mobility decreases with increasing temperature. Impurity scattering on the other hand, which is a result of the movement of a carrier past an ionized dopant impurity, becomes less significant at higher temperatures [20].

Although the peak mobility of GaAs in the linear region can be as much as six times greater than that of silicon (Si) at typical field strengths, the advantage of GaAs may be only as much as a factor of two[21]. This still translates to the fact that GaAs devices can work at significantly higher frequencies than Si. The exact increase in the speed of operation depends on factors such as the circuit capacitance and the electric field regime in which the device operates.

2.4 Crystal Defects
No semiconductor crystalline material is perfect, and GaAs crystals, in spite of the efforts to control crystal growth, contain a number of crystal defects, dislocations, and impurities. These defects can have either desirable or undesirable effects on the electronic properties of GaAs. The natures of these defects and the observed effects are determined by the method of their incorporation into the material and the general growth conditions.

2.5 Point Defects
Localized defects of atomic dimensions, called point defects, can occur in an otherwise perfect crystal lattice. These point defects can include vacancies, interstitials, misplaced atoms, intentionally introduced dopant impurities, and impurities introduced inadvertently during the material growth process. The study of point defects is important because of the effect these defects have on the electronic properties of the material and the strong relationship between diffusion and the number and type of defects in the crystalline material. The electrical properties of a semiconductor can be manipulated by

the deliberate insertion of chemical defects (impurities) into the material during the growth and processing steps. However, intrinsic defects present in the material also play an important role in the electronic behavior of GaAs.

Many intrinsic defects are observed in GaAs. The concentration and effect of these defects are determined by the manner in which the material is grown. Intrinsic defects in GaAs include arsenic and gallium vacancies, their concentration being determined by the overpressure of arsenic during processing. The effect of these vacancy defects has been observed to be neutral [22], deep donor-like, and deep acceptor-like [23]. EL2, an important defect in GaAs, is present in material grown from an arsenic rich melt. This defect is donor-like in character and is located at the middle of the energy gap [24]. It is thermally very stable and can withstand processing temperatures up to 900°C, and acts as an electron trap. The importance of this defect lies in its ability to convert p-type GaAs to semi-insulating material, and its thermal stability.

2.6 Impurities in GaAs

Chemical point defects (doping impurities) can be introduced to the crystalline material either deliberately or inadvertently as contamination during processing. In general, substitution impurities are electronically active, whereas many contaminants are interstitial in nature and are electronically inactive. Dopants are classified as either donors or acceptors. A donor has one more electron than the atom it is replacing in the crystal. This extra electron is easily removed or donated to the conduction current. An acceptor, on the other hand, has one less electron than the atom it is replacing. Thus, an acceptor can easily capture an electron and prevent it from adding to the conduction current. Regardless of the type or character of the impurity, the electrical properties of the semiconductor are altered.
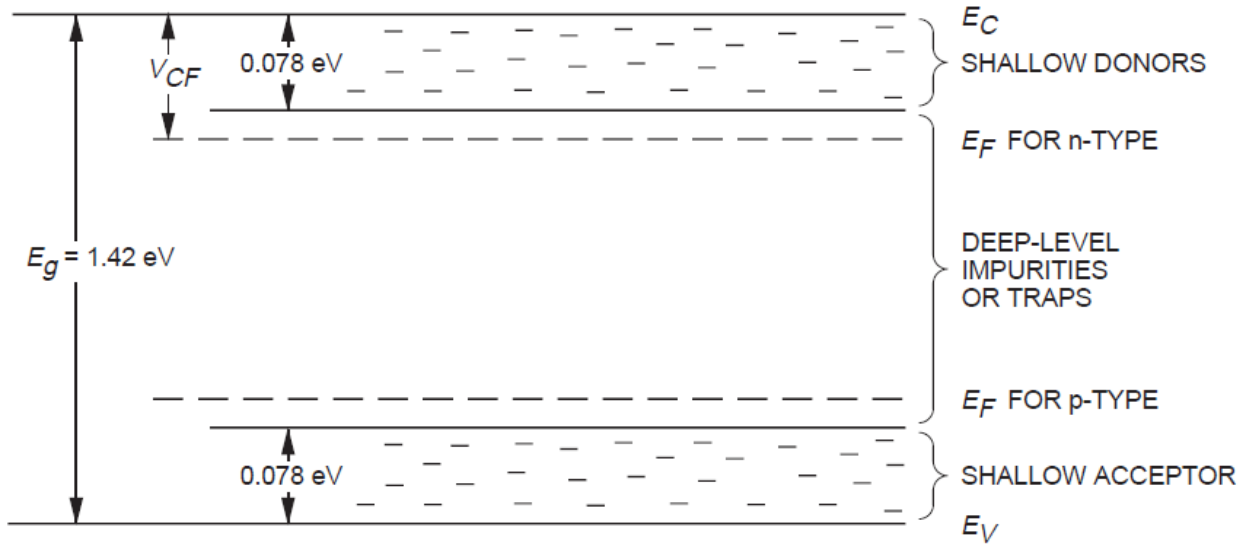
Figure 5 Energy band diagrams of GaAs with impurities.

Figure 5 shows the energy band diagram of GaAs with the addition of impurities. Shallow donor or acceptor impurities have energy levels within $3kT$ of the conduction and valance band, respectively. Since the energy required for an electron to transition from these impurity energy levels to the nearest band edge is very small, they are typically fully ionized at room temperature. The Fermi level shifts from the band center towards the impurity levels to reflect this. In other words, for donor impurities, the Fermi level shifts towards the conduction band and decreases as the donor doping concentration increases. A similar description can be made of acceptor impurities. It is these shallow impurities that are used for doping purposes. Impurities with energies in the center of the band gap are called deep impurities. Deep impurities generally degrade device performance by reducing the carrier lifetime.

Both impurity types, deep and shallow, are present in GaAs in the form of complexes with gallium or arsenic. One of the most common is silicon. This group IV element can be used to give either p-type GaAs by incorporating it at low temperatures, or n-type GaAs by processing it at high temperatures. Another group IV element, carbon, is also used extensively to provide p-type GaAs. Chromium (Cr) behaves as an acceptor, with an

impurity level close to the center of the energy gap. This property makes it very useful for counter doping n-type GaAs to make it semi-insulating. Other elements such as copper, oxygen, selenium, and tin are also used in GaAs processing to provide the desired n- or p-like behavior [25].

2.7 Technical products and impurities

Purity requirements for the raw materials used to produce gallium arsenide are stringent. For optoelectronic devices such as light-emitting diodes (LEDs), laser diodes, photo detectors, solar cells), the gallium and arsenic must be at least 99.9999% pure; for integrated circuits, a purity of 99.99999% is required. These purity levels are referred to by several names: 99.9999%-pure gallium is often called 6-nines, 6N or optoelectronic grade, while 99.99999%-pure gallium is called 7-nines, 7N, semi-insulating (SI) or integrated circuit (IC) grade.

For 7N gallium, the total of the impurities must be < 100 µg/kg. In addition to the challenge of consistently producing material with such high purity, there are difficulties in detecting the small quantity of impurities. Certain impurities cause more problems than others during gallium arsenide production. Those of most concern are calcium, carbon, copper, iron, magnesium, manganese, nickel, selenium, silicon, sulfur, tellurium and tin. Generally, these elements should be present in concentrations < 1 µg/kg in both the gallium and the arsenic. Lead, mercury and zinc should be present in concentrations < 5 µg/kg. Although aluminum, chlorine and sodium are often present, the concentrations of each should be < 10 µg/kg . Some companies have even more stringent requirements [26]

2.8 Occurrence

Gallium arsenide does not occur naturally. Gallium is present in the earth's crust at 5–15 mg/kg and is recovered as a by-product of the extraction of aluminum and zinc from their ore [27]. Arsenic concentration in the earth's crust is generally less than 2 mg/kg, but may be elevated in zones of active or extinct volcanic activity [28].

2.9 Exposure

Exposure to gallium arsenide occurs predominantly in the microelectronics industry where workers are involved in the production of gallium arsenide crystals, ingots and wafers, in grinding and sawing operations, in device fabrication, and in sandblasting and clean-up activities [29]. The National Institute for Occupational Safety and Health (NIOSH) estimated that in 1981 the microelectronics industry with over 500 plants manufacturing semiconductors [30].

2.10 Production

Gallium occurs in very small concentrations in many rocks and ores of other metals. Most gallium is produced as a by-product of processing bauxite, and the remainder is produced from zinc-processing residues. Only part of the gallium present in bauxite and zinc ores is recoverable, and the factors controlling the recovery are proprietary. Therefore, an estimate of current reserves cannot be made. The world bauxite reserve base is so large that much of it will not be mined for many decades; hence, most of the gallium in the bauxite reserve base cannot be considered to be available in the short term [31].

Demand for gallium in the USA in 2003 was satisfied by imports, mainly low-purity material from China, Kazakhstan and the Russian Federation and smaller amounts of high-purity material from France. In addition, in 2002, the USA imported an estimated 120 tons of doped and un- doped gallium arsenide wafers, mainly from Finland, Germany, Italy and Japan. Consumption of high-purity gallium in Japan in 2002 was estimated to be 108 tones, including domestic production of 8 tones, imports of 55 tones and scrap recycling of 45 tones [32]

Gallium arsenide can be obtained by direct combination of the elements at high temperature and pressure; it can also be prepared, mainly as a thin film, by numerous exchange reactions in the vapor phase. Gallium arsenide single crystals are more difficult to fabricate than those of silicon, with silicon, only one component needs to be

controlled, whereas with gallium arsenide, a 1:1 ratio of gallium atoms to arsenic atoms must be maintained. At the same time, arsenic volatilizes at the temperatures needed to grow crystals. To prevent loss of arsenic, which would result in the formation of an undesirable gallium-rich crystal, gallium arsenide single-crystal ingots are grown in an enclosed environment. Two basic methods are used to fabricate gallium arsenide ingots: the boat-growth, horizontal Bridgeman or gradient freeze technique and the liquid-encapsulated Czochralski technique. Ingots produced by the horizontal Bridgeman method are D-shaped and have a typical cross-sectional area of about 4insq .In contrast, single-crystal ingots grown by the liquid-encapsulated Czochralski method are round and are generally 3 in diameter, with a cross-sectional area of about 7insq [33,34]. Ingots grown by the horizontal Bridgeman method are cleaned in chemical baths of aqua regia and isopropyl alcohol, and sandblasted using an abrasive material such as silicon carbide.

The crystalline orientation of the gallium arsenide ingot is checked by X-ray diffraction and the ends are cut off with a diamond blade saw. The ingots are shaped by grinding the edges and then sliced into wafers along the proper crystalline axis. Wafers pass through several stages of surface preparation, polishing and testing before they are ready for device manufacture or epitaxial growth. Epitaxy is a method for growing single crystals in which chemical reactions produce thin layers of materials whose lattice structures are identical to that of the substrate on which they are deposited. Pure gallium arsenide is semi-insulating and, in order to conduct electricity, a small number of atoms of another element must be incorporated into the crystal structure; this is called doping. Doping is accomplished by either ion implantation or epitaxial growth [35,36]

2.12 Applications

Gallium arsenide has light-emitting properties, high electron mobility, electromagnetic properties and photovoltaic properties. As a semiconductor, it has several unique material properties which can be utilized in high speed semi-conductor devices, high power microwave and millimeter-wave devices, and optoelectronic devices including fiber optic sources and detectors. Its advantages as a material for high speed devices are high electron mobility and saturation velocity, and relatively easy growth of semi-insulating substrates which render low parasitic and good device isolation. Other useful properties

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are controllable band gap by alloying, desirable ionization and optical absorption properties. Gallium arsenide has certain advantages over other semiconductor materials: faster operation with lower power consumption, better resistance to radiation and, most importantly, it may be used to convert electrical into optical signals [37].

Gallium arsenide wafer manufacturers and some electrical companies produce gallium arsenide epitaxial-growth wafers and LED drips. Vapor-phase epitaxial or liquid-phase epitaxy is used to grow gallium arsenide layers for most LEDs. The super-bright red LEDs are manufactured using liquid-phase epitaxial to grow aluminum–gallium–arsenide on gallium arsenide substrates. Epitaxial growth based on metal–organic chemical vapor deposition (MOCVD) technology is used in manufacturing some types of infrared LEDs used in optocouplers. MOCVD is also used to grow a gallium arsenide layer (buffer layer) on gallium arsenide substrates for low-cost optic fibres dedicated to local area computer networks. Gallium arsenide-based laser diodes are manufactured using liquid-phase epitaxial, MOCVD and molecular beam epitaxial technologies [38].

For analogue ICs, the requirements for epitaxial grow at the same rate as frequencies increase. An epitaxial gallium arsenide layer is also required for most microwave devices with frequencies over 20 GHz. Photovoltaic applications require gallium arsenide wafers and epitaxial layers. Night-vision system devices use an epitaxial layer of gallium arsenide applied to one end of a photomultiplier to enhance infrared images. Gallium arsenide epitaxial-growth wafers are is also used in optical ICs and magneto electric transducers [39].

CHAPTER 3

MESFET device principle and operation

3.1 Basic operation

The overall electrical characteristics of the GaAs MESFET are mainly determined by the electrical property of the semiconductor material and the nature of the physical contact to the material. Knowledge of the device physical structure and properties is helpful for both device modeling and circuit design. In the second part of this chapter, a brief description of MESFET operation is presented. It covers the basic construction of the device, the major operating regions, the small signal equivalent circuit, important nonlinear properties, and some second order effects [40].

A variety of models have been proposed for the GaAs MESFET. For small signal models, the difference of various models lies in the equivalent circuit topology selection and the way the equivalent circuit parameters are extracted. For nonlinear models, according to how these models are derived, they can be classified into physical model, empirical model, experimental model and the more recently developed black-box model, various MESFET models have been used by both device and circuit designers. Different applications and designs place different requirements on the model. Therefore, an understanding of the features of various modeling approaches is helpful for choosing the right model, and constructing new models for different application. The second part of this chapter gives an overview of GaAs MESFET models, including the nonlinear and the small signal models [41].

3.2 Device Description and operation

A cross-section view of a MESFET is shown in Figure 6, which illustrates its basic structure. Three metal electrode contacts are shown to be formed onto a thin semiconductor active channel layer. Source and drain are ohmic contacts, while gate is a Schottky contact. The gate metal forms a Schottky barrier diode, which gives a depletion region between the source and the drain. The gate depletion region and the semi-insulating substrate form the boundary of the conducting channel. A potential applied to

the drain causes electrons to flow from the source to the drain. Any potential applied on the gate causes a change in the shape of depletion region, and a subsequent change in current flow.
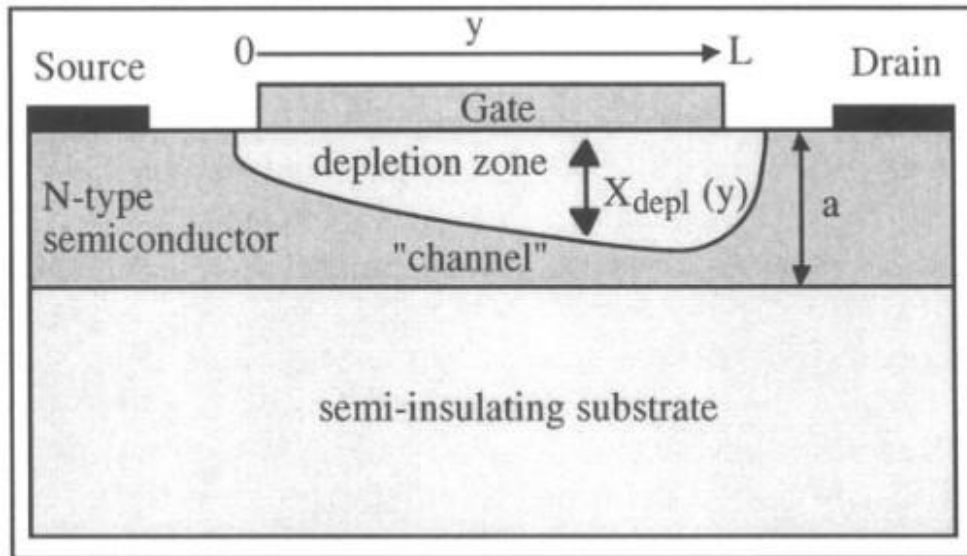

Figure 6 Cross-sectional view of GaAs MESFET

The most critical dimension is the "length" of the gate along the carrier path for microwave operations. The shorter the gate length, the higher becomes the signal frequency. If the FET is to handle a large amount of signal current, the gate width must be increased appropriately [42].

The MESFET is a form of semiconductor technology which is very similar to a junction FET or JFET. As the name of the MESFET indicates, it has a metal contact directly onto the silicon, and this forms a Schottky barrier diode junction. The material that is used in this form of semiconductor technology is GaAs (gallium arsenide). The substrate for the semiconductor device is semi-insulating for low parasitic capacitance, and then the active layer is deposited epitaxial. The resulting channel is typically less than 0.2 microns thick.

The doping profile is normally non-uniform in a direction perpendicular to the gate. This makes for a device which has good linearity and low noise. Most devices are required for

high speed operation, and therefore an n-channel is used because electrons have a much greater mobility than holes that would be present in a p-channel [43].

The gate contacts can be made from a variety of materials including Aluminum, a Titanium-Platinum-Gold layered structure, Platinum itself, or Tungsten. These provide a high barrier height and this in turn reduces the leakage current. This is particularly important for enhancement mode devices which require a forward biased junction.

The gate length to depth ratio is an important as this determines a number of the performance parameters. Typically it is kept at around four as there is a trade-off between parasitic, speed, and short channel effects [44].

The source and drain regions are formed by ion-implantation. The drain contacts for GaAs MESFETs are normally AuGe - a Gold-Germanium alloy.

There are two main structures that are used for MESFETs as shown in Figure 7 and Figure 8

1. **Non-self-aligned source and drain:**

    For this form of MESFET, the gate is placed on a section of the channel. The gate contact does not cover the whole of the length of the channel. This arises because the source and drain contacts are normally formed before the gate.
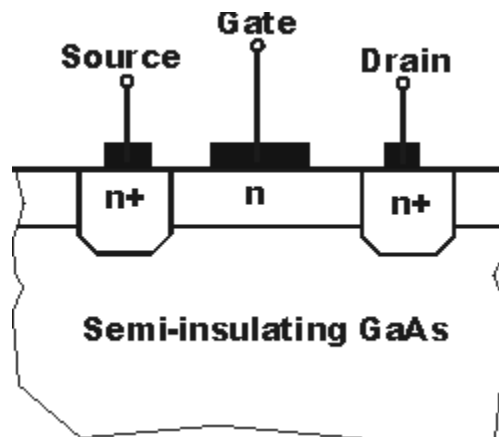

Figure 7 Non-self-aligned MESFET structure

2. **Self-aligned source and drain:**

This form of structure reduces the length of the channel and the gate contact covers the whole length. This can be done because the gate is formed first, but in order that the annealing process required after the formation of the source and drain areas by ion implantation, the gate contact must be able to withstand the high temperatures and this results in the use of a limited number of materials being suitable.
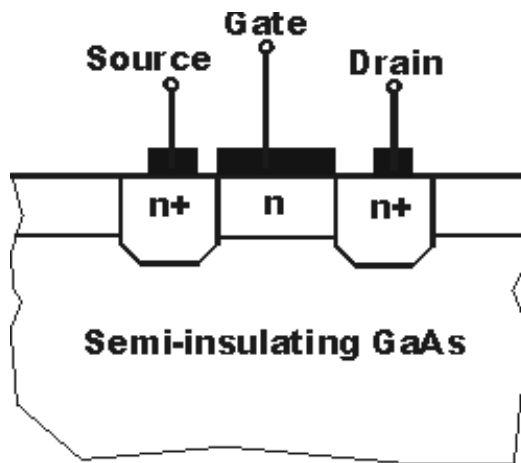
Figure 8 Self aligned MESFET structure

3.3 Current Voltage Characteristics

The current-voltage relationships of a MESFET are illustrated in Figure 8. The channel current is plotted as a function of applied drain-source potential for different gate-source voltage levels. Three regions of operation can be identified from the figure. They are the linear region, the saturation region and the breakdown region. In the linear region, current flow is approximately linear with drain voltage. As drain potential increases, the depletion region at the drain end of the gate becomes larger than at the source end. Since the device is taking constant current through the channel region, the electrical field

increases as the channel region narrows, and therefore a related increase in electron velocity occur [45].

However, if the gate reverse bias is increased while the drain bias is held constant, the depletion region widens and the conductive channel becomes narrower, reducing the current. When Vgs=V_p, the pinch-off voltage, the channel is fully depleted and the drain current is zero, regardless of the value of Vds. Thus, both V_{gs} and V_{ds} can be used to control the drain current. When the MESFET is operated under such bias voltages, where both V_{gs} and V_{ds} have a strong effect on the drain current, it is said to be in its linear or voltage controlled resistor region channel near the drain becomes narrower, the electrons must move faster.

However, the electron velocity cannot, increase indefinitely; the average velocity of the electrons in GaAs cannot exceed a velocity called the saturated drift velocity, approximately 1.3x107 cm/s. If V_{ds} is increased beyond the value that causes velocity saturation (usually only a few tenths of a volt), the electron concentration rather than velocity must increase in order to maintain current continuity. Accordingly, a region of electron accumulation forms near the end of the gate. Conversely, after the electrons transit the channel and move at saturated velocity into the wide area between the gate and drain, an electron depletion region is formed [46].

The depletion region is positively charged because of the positive donor ions remaining in the crystal. As V_{ds} is increased further, as shown in figure 9, progressively more of the voltage increase is dropped across this region to enforce the electrons to cross it and less is dropped across the unsaturated part of the channel. This region is called a dipole layer or charge domain. Eventually, a point is reached where further increase in V_{ds} is dropped entirely across the charge domain and does not substantially increase the drain current. At this point, the electrons move at saturated drift velocity over a large part of the channel length. When the MESFET is operated in this manner, which is the normal mode of operation for small-signal devices, it is said to be in its saturated region [47].
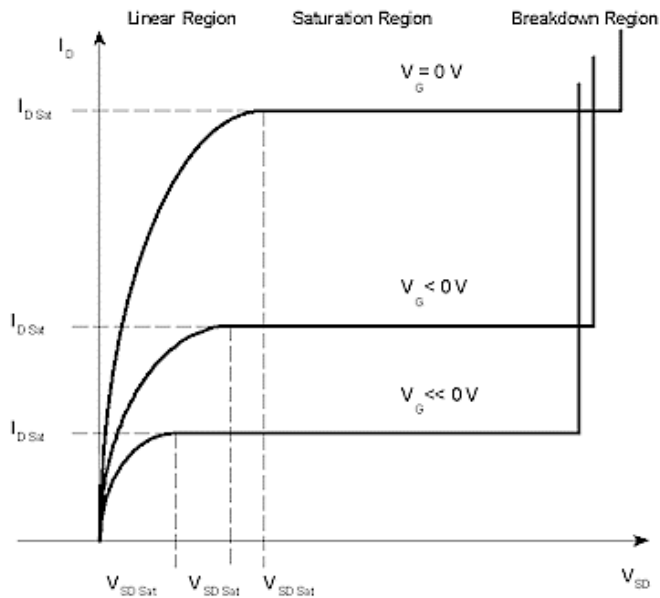
Figure 9 Current-Voltage characteristics of MESFET

3.4 Transconductance and output resistance

The output conductance of the device is an important characteristic in analog applications. It plays a significant role in determining the maximum voltage gain attainable from the device and is extremely important for determining optimum output matching properties. In general, for a device to have a low value output conductance is desirable, or, equivalently, an extremely high output resistance. Figure 10 shows measured microwave output resistance for a MESFET device. As expected from Figure 10, the output resistance is low at low drain-source bias levels and increases dramatically as the device reaches saturation. This is true for all the curves except for a gate bias level of −1V. At this bias level, the active channel is nearly pinched-off by the depletion region. Device dimensions and channel material properties both affect output resistance of the MESFET. As in the case of channel current, the magnitude of the device output conductance (the inverse of the resistance) is directly proportional to device gate width.
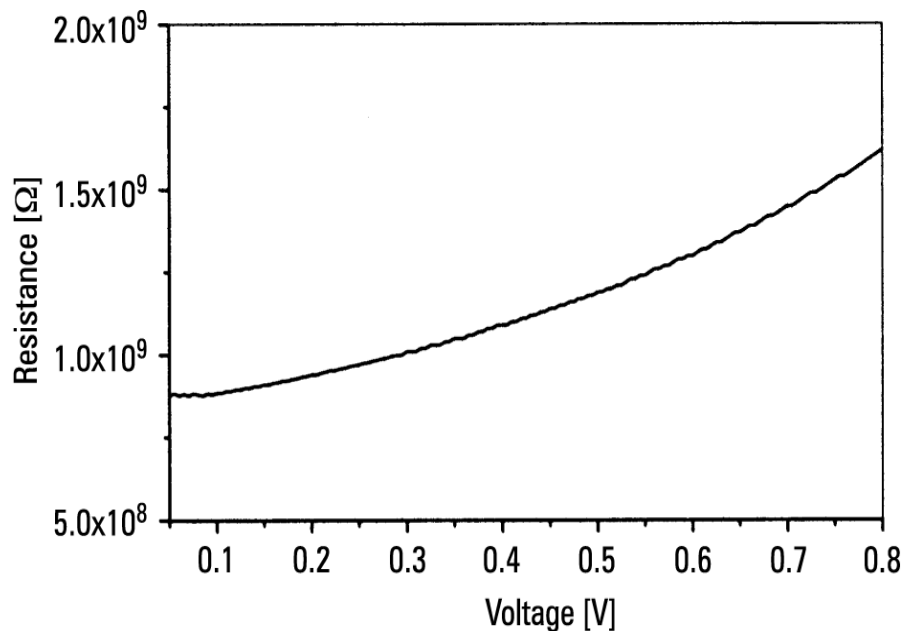
Figure 10 Plot of Resistance Vs drain to source voltage

For devices with equivalent gate widths, short gate lengths typically result in lower output resistances. The output resistance can also be reduced by increasing channel doping concentrations, N_d, or the device epi-thickness. The device transconductance is defined as the slope of the Ids-Vgs characteristics with the drain-source voltage held constant.

Transconductance, gm, and its phase angle in GaAs MESFET's and JFET's exhibits significant low-frequency dispersion. The transconductance measured at very low frequencies usually (5 1 0 Hz) is larger than at high frequencies (2 1 kHz). The phase angle also has a dip appearing around the transition frequency. The transition frequencies typically range from few 10's Hz to few 10's kHz. Moreover, different surface treatment, gate voltage, temperature, and device structures (such as gate length) also have a strong influence on this transconductance dispersion. The low frequency dispersion of g_m has a

profound effect on the microwave behavior of FET-based MMIC's [48]. To understand and to control this effect is essential in obtaining reliable and controllable device.

3.5 Capacitances Cgs, Cgd and Cds

The behavior of the depletion region beneath the gate of a MESFET is determined by the bias applied to the device terminals. The variation of the space charge region is caused by both gate-to-source potential and gate-to-drain potential. Gate charge Qg is considered to be the space charge beneath the gate that varies with gate bias and drain bias. The plot for the gate source capacitance and gate to drain capacitance with respect to the drain to source voltages is shown in figure11and figure12 [49].

The gate-source capacitance Cgs is the derivative of the space charge with respect to the gate-source bias Vgs, when the gate-drain voltage is constant:

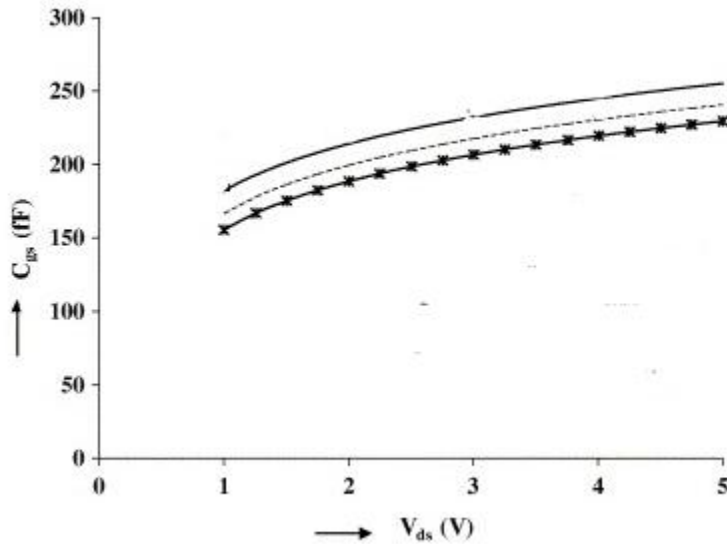$$Cgs = \frac{\partial Qg}{\partial Vgs} \qquad (2)$$

Figure 11 Plot of Gate to Source Capacitance versus Drain to Source Voltage
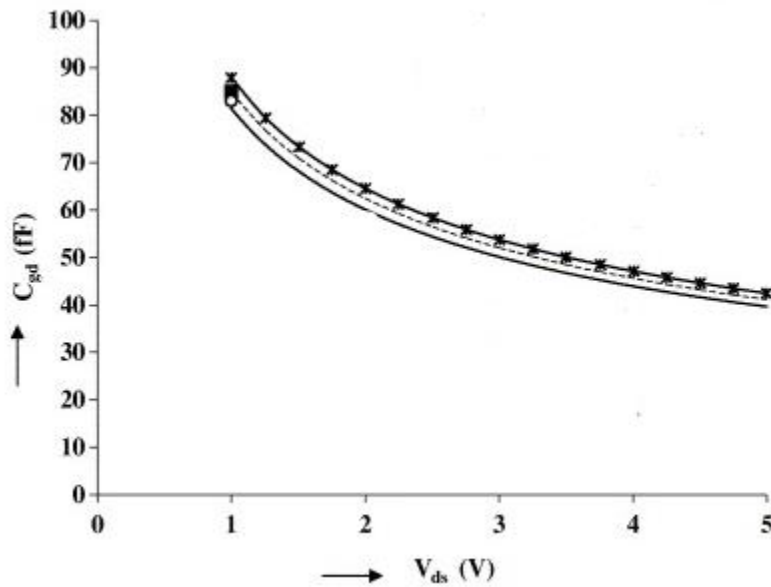
Figure 12 Plot of Gate to Drain Capacitance versus Drain to Source Voltage

$$Cgd = \frac{\partial Qg}{\partial Vgd} \tag{3}$$

The gate drain capacitance Cgd is smaller in magnitude than Cgs under normal bias conditions. However, it is critical in accurate S-parameter prediction. The drain-source capacitance C_{ds} in the equivalent circuit is introduced to model

3.6 Device Models

In a typical application, models are used to predict or estimate performance information that is not available or easily obtainable by direct measurement. Small signal, large-signal and noise models are utilized to obtain information about device characteristics. Small-signal models can offer the designer the ability to predict performance of devices with gate width dimensions that have been scaled from previously measured devices. Another

use of these models is to interpolate or extrapolate measured data to frequencies not covered by measurements. Noise models are used to predict the noise figure for arbitrary circuit topologies, which incorporate a particular device, or to predict the ultimate noise performance of a device [50].

A large-signal model provides a means of obtaining performance information concerning nonlinear operation of a device or device-circuit combination. Models are classified according to how they are derived. Empirical models are derived from describing observed characteristics with arbitrary functions. Physically based models are derived from the physical principles that apply to the device structure. And many models have aspects of both empirical and physical derivations. Physically based models are useful to circuit and device designers who have some control over the fabrication process because they allow simultaneous optimization of both the devices and the circuits in which they are to be used.

Additionally, a physical model is useful for predicting the effects of process variations on the electrical behavior of a device. If the statistical distribution of the process parameters is known, yield predictions can also be obtained. Using such an approach, performance prediction information may be obtained purely from physical data describing the device (i.e., device geometry and semiconductor material properties). No electrical characterization of individual devices is required. But purely physical models are not as accurate as required for most circuit design applications. The inaccuracies arise from the assumptions and approximations required to perform the device analysis. Even the most sophisticated multidimensional numerical device simulation techniques make simplifying assumptions that can severely limit their accuracy. For example, surface state effects, traps, non-homogeneous interfaces, etc., are typically neglected in these analyses. Yet these phenomena have a significant effect on the microwave performance of modern devices.

A second problem with physically based models is that information concerning the physical design of the device can often be difficult or impossible to obtain-especially for

the circuit designer utilizing purchased devices. This problem may be solved by extracting the physical parameter values from measured data in the same way that empirical parameter values are determined. In contrast, empirical models are capable of prediction accuracies that approach measurement capability [51].

The primary difficulty with this approach is that large amounts of tedious characterization data are often required to obtain such accuracy. In addition, minor changes in the device geometry or material require the performance of complete characterizations. Such models are also of questionable value when performing design centering or yield analyses because the empirical parameter distributions do not vary independently. Because physical models are typically less accurate than their empirical counterparts, one attractive implementation is to use an empirical model to simulate nominal device performance and then use the physically based model to predict the deviations about this nominal behavior resulting from process parameter variations. In this chapter, we will give some details of several models. The section is divided into two sections according to the type of performance predictions for which the models are used small signal model and large signal model [52].

3.7 The small-signal Model

MESFET model is extremely important for active microwave circuit work. This model provides a vital link between measured 24S-parameters and the electrical processes occurring within the device. Each of the elements in the equivalent circuit as shown in Figure 13 provides a lumped element approximation to some aspect of the device physics. A properly chosen topology, in addition to being physically meaningful, provides an excellent match to measured S-parameters over a very wide frequency range. When element values are properly extracted, the model is valid above the frequency range of the measurements, providing the possibility of extrapolating device performance to frequencies beyond some equipment's measurement capabilities. In addition, equivalent circuit element values can be scaled with gate width, thereby enabling the designer to predict the S-parameters of different size devices from a given foundry. The

ability to include device gate width scaling as part of the circuit design process is important in MMIC design applications [53].
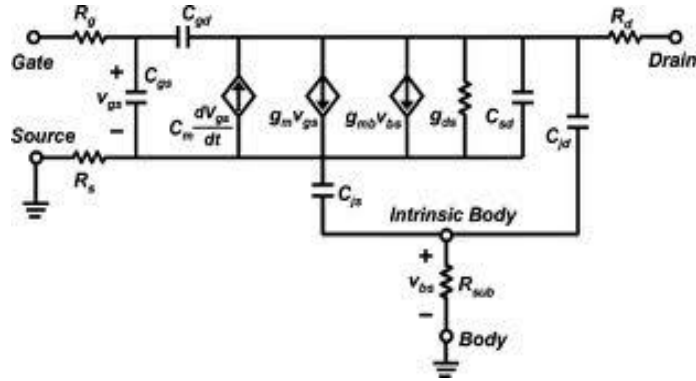
Figure 13 Small signal model equivalent circuits

3.8 Large Signal Models

Several researchers have developed empirical models that describe the operational characteristics of the GaAs MESFET. All of these models are analytical and all are capable of describing the large-signal properties of microwave MESFETs with some success. The MESFET models discussed in this section are available in many of the popular large-signal circuit simulation packages used by microwave engineers. For any given device and application, the optimal choice of models depends on many considerations including model availability, computational efficiency, and prediction accuracy [54].

Figure 14 Large signal model equivalent circuits

Large signal models are required for circuit simulation that is involved in predicting either large signal or nonlinear performance. As in Figure 14 a typical equivalent circuit for a MESFET l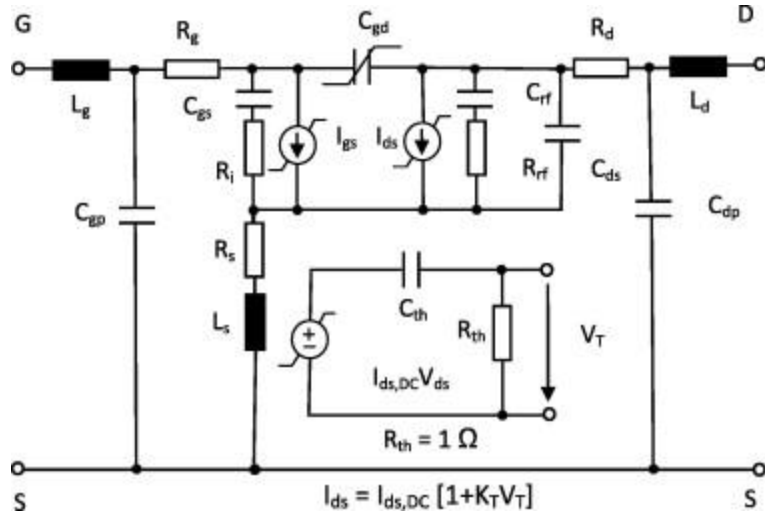arge-signal model is shown. The equivalent circuit is divided into the extrinsic parasitic elements and the intrinsic device. The extrinsic elements include Parasitic capacitance associated with the gate of a MESFET device Cpg, Parasitic capacitance associated with the drain of a MESFET device Cpd, Parasitic gate inductance of a MESFET device Lg, Parasitic drain inductance of a MESFET device Ld, Ls, Parasitic source inductance of a MESFET device, Parasitic gate resistance of a MESFET device Rg, Parasitic drain resistance of a MESFET device Rd, and Parasitic source resistance of a MESFET device Rs, which are independent of biasing conditions. The main nonlinear elements include the drain source current Ids, gate capacitances Cgs and Cgd, as well as diode Dgs Gate-to-Source junction diode and Dgd Gate-to-Drain junction diode Dgs, represents the forward-bias gate current, which is important in modeling device breakdown under inverted drain-source bias condition. Diode Dgd gate to drain junction diode is included to model drain-gate avalanche current. Among these nonlinear properties, the most important are the drain source current and the gate capacitances. They are included in most nonlinear GaAs MESFET models.

CHAPTER-4

Numerical calculations

4.1 Theory on the Model

Simulation of nonlinear microwave circuits utilizing GaAs MESFET devices reveals the circuit simulation accuracy from an ac point of view to be quite sensitive to the precision by which the gate-source and gate-drain capacitances of the device are modeled as function of voltage [55] .Inaccuracies from this view point restrict the bias area over which the accuracy of the overall model remains high from a microwave point of view. The available method for simulating the capacitance has been considered and a new equation is proposed. The new technique is supposed to improve accuracy with a simple parameter estimation process and up to 72% savings in CPU execution speed over some of the available methods [56].In addition, the primary parameters of the equation reflect the physical capacitance value associated with the junction under assessment and it is valid for silicon and GaAs devices.

The current voltage represented by the Curtice model, the dc equation exclusive of parasitic resistances is approximated by

$$I_d = (V_{gs} - V_{to})^2 * (1 + V_{ds}) * \tanh(\alpha V_{ds}) \tag{4}$$

Where, in this equation

I_d is the drain current

V_{ds} is the drain to source voltage

V_{to} is the threshold voltage

λ is the parameter related to drain current

The drain current saturates at the same drain-to-source voltage irrespective of the gate-to-source voltage. This is different from conventional JFET or MOSFET models and occurs because the critical field E_{sat} in the channel is reached at approximately the same voltage $V_{ds}= E_{sat}*L$, where L is the channel length. However, the behavior of I_d as a function of Vgs is only poorly rep- resented, especially if the pinch off voltage of the transistor is large, except for V_{gs} near the pinch off voltage, the saturated drain current Ids is proportional to the height of the undeleted channel region near the source end. This is because the reduction in channel height between the channel entrance and the point where the carrier velocity saturates is usually a negligible fraction of the height at the entrance. Thus the current may be approximately calculated by assuming that all carriers at the channel opening are moving at their saturated velocity[57].For constant channel doping, the saturated drain current I d s should then vary approximately as

$$I_{ds} = Z\ V_{sat}*\sqrt{2\epsilon qNd}\ (\sqrt{(-Vt+Vb)} - \sqrt{(-Vgs+Vb)}) \qquad (5)$$

Z = channel width;

V_{sat} = saturated electron velocity;

ϵ = dielectric constant; q is the electron charge,

N_d = donor density,

V_t = threshold voltage.

V_b = built-in gate junction potential

 It is to be considered that the V_{gs} and V are normally negative. The first term in equation (5) is proportional to the height of the space-charge region at the threshold voltage, and thus is proportional to the thickness of the doped region under the gate. The second term in equation (5) is proportional to the height of the space-charge region when the gate-to-source voltage Vgs is applied. Thus equation (5) is indeed proportional to the height of the undepleted channel.

The equation (5) is obtained by assuming that all carriers in the channel opening move at their saturated velocity. The approximation for the current in equation (5) breaks

velocity saturation of the carriers is comparable to the voltage difference $V_{gs} - V_t$ [58].

4.2 Source and Drain Capacitances

Current GaAs device simulations use a diode-like capacitance between source and gate, where the space-charge region thickness and thus the capacitance is determined by the gate-to-source voltage. A similar diode model is often used to describe the normally much smaller gate-to-drain capacitance [59]

The two most popular methods of representing the junction capacitances C_{gs}, C_{gd} of the device are the p-n junction depletion capacitance formulae and the Statz approach [60] .In the former, which was originally developed for silicon devices, each junction capacitance has been represented as a function of its junction capacitance at thermal equilibrium gate junction capacitance (Cjo), junction voltage (V), built in junction voltage(Ø) and capacitance gradient factor (m). The capacitance can be expressed as:

$$C = \frac{Cjo}{(1-\frac{V}{\emptyset})^m}$$ (6)

Although equation (6) works well with silicon-based devices, its accuracy is poor when applied to GaAs devices because of the equation linear approximation law

$$(\log (CjO/C) = m \; \log (\, V\,) \; - m \log (\emptyset)$$ (7)

Also, it assumes each junction capacitance is only dependent on the voltage appearing across the junction under consideration which is not the case for GaAs MESFET's. A major challenge is to find a simple expression for the gate charge Q, Measurements as well as calculations based confirm that the gate-source capacitance C, is approximated by a simple diode-capacitance model, in the normal bias range Vds >> 0. The gate-to-drain capacitance C_{gd} in this voltage range is small as compared to Cg, (C_{gd}= 0.1 - 0.3 Cg), and furthermore, C_{gd} is approximately constant and nearly independent of Vgs or Vgd. We may thus choose a gate charge (for constant doping under the gate) and for a normally (forward) biased transistor [61].

$$Q_g = 2\ C_{gs0}.V_b\ (1 - \sqrt{1 - \frac{V_{gs}}{V_b}}) + C_{gdo}.V_{gd} \qquad (8)$$

For $V_{ds} \gg 0$, or alternatively, $- V_{gd} \gg - V_{gs}$. (The use of $- V_{gs}$ and $- V_{gd}$ instead of V_{gs} and V_{gd} allows for the fact that both voltages are usually negative. In equation (8), C_{gso} is the gate-to-source capacitance for zero source-to-gate bias, V_b is the built-in junction potential and C_{gdo} is the gate-to-drain capacitance. The charge has been normalized to be zero when $V_{gs} = 0$ and $V_{gd} = 0$. Note that V is negative in the normal bias range. The first part of equation (8) follows directly from Poisson's equation. For a reverse-biased transistor $(V_{ds} \ll 0)$, different equations are needed, since the nominal source now really acts like a drain and the nominal drain like a source. The corresponding charge expression, obtained by interchanging V_{gd} and V_{gs} [62].

$$Q_g = 2\ C_{gs0}.V_b\ (1 - \sqrt{1 - \frac{V_{gs}}{V_b}}) + C_{gdo}.V_{gs} \qquad (9)$$

The transition from equation (8) to equation (9) can be envisioned to occur at $V_{ds} = 0$, or $V_{gd} = V_{gs}$. At $V_d = 0$ Q, is continuous, as may be seen by inspection. The derivatives of Q, with respect to the voltages, however, are discontinuous. In particular, it is found for $V_d > 0$

$$C_{gs} = \frac{dQg}{dVgs} = \frac{Cgs0}{\sqrt{1 - \frac{Vgs}{vb}}} \qquad\qquad C_{gd} = \frac{dQg}{dVgd} = C_{gd0} \qquad (10)$$

And for Vds<0

$$C_{gs} = \frac{dQg}{dVgs} = C_{gdo} \qquad\qquad C_{gdo} = \frac{dQg}{dVgd} = \frac{C_{gdo}}{\sqrt{1 - \frac{Vgd}{vb}}} \qquad (11)$$

Equation (10) approximates the desired behavior but is still deficient in that the abrupt transitions or steps in the values of C_{gs} and C_{gd} at $V_{ds}=0$ are nonphysical and also would cause convergence difficulties in the numerical analysis[63].

Now the equation (8) and equation (9) can be written in the form

$$Q = 2 * C_{gso} * V_b \left\{ 1 + \sqrt{1 - \frac{V_{eff1}}{Vb}} \right\} + C_{gdo} * V_{eff2} \tag{12}$$

Here in equation (12), the terminology $(-V_{eff1})$ is meant to stand for the smaller of the two values of $(-V_{gd})$ or $(-V_{gs})$ and $(- V_{eff2})$ for the larger of the two. Mathematically, we can select these values by using

$$V_{eff1} = \frac{1}{2} \left\{ Vgs + Vgd + \sqrt{(Vgs - vgd)^2 + \Delta^2} \right\} \tag{13}$$

$$V_{eff2} \; \frac{1}{2} \left\{ Vgs + Vgd + \sqrt{(Vgs - vgd)^2 + \Delta^2} \right\} \tag{14}$$

Functions with $\Delta = 0$. The inclusion of a nonzero Δ produces a smooth transition of width Δ in the value of V_{eff1} and V_{eff2} for from -4 to 2 V for $\Delta = 0$ and 0.5 $V_{gs} = -1V$ as a function of V_{gd} from -4 to 2 V for $\Delta = 0$ and 0.5.

The use of V_{eff1} and V_{eff2} in equation (12) also yields a smooth interpolation of C_{gs} and C_{gd} through the former point of discontinuity at $V_{ds}=0$. Differentiating equation (12),the C_{gs} and C_{gd} obtained are as follows

$$C_{gs} = \frac{0.25 * C_{gso}}{\sqrt{1 - \frac{V_{new}}{Vb}}} * 0.5 * \left\{ 1 + \frac{(Vgs - Vgd)}{\sqrt{(Vgs - Vgd)^2 + (\Delta)^2}} \right\} + 0.5 * C_{gdo} * \left\{ 1 - \frac{(Vgs - Vgd)}{\sqrt{(Vgs - Vgd)^2 + (\Delta)^2}} \right\} \tag{15}$$

$$C_{gd} = \frac{0.25 * C_{gso}}{\sqrt{1 - \frac{V_{new}}{Vb}}} * 0.5 * \left\{ 1 - \frac{(Vgs - Vgd)}{\sqrt{(Vgs - Vgd)^2 + (\Delta)^2}} \right\} + 0.5 * C_{gdo} * \left\{ 1 + \frac{(Vgs - Vgd)}{\sqrt{(Vgs - Vgd)^2 + (\Delta)^2}} \right\} \tag{16}$$

The gate-to-source capacitance reaches infinity for $V_{eff} = V_b$, the capacitance is kept constant, when $V_{eff1} > V_{max}$,by using the following function for Q_g as in equation (17)

$$Q_g = C_{gso} \left\{ 2V_s \left(1 - \sqrt{1 - \frac{V_{max}}{Vb}} \right) + \frac{V_{eff1} - V_{max}}{\sqrt{1 - \frac{V_{max}}{V_b}}} \right\} + C_{gdo} V_{eff2} \tag{17}$$

The two most popular methods of representing the junction capacitances C_{gs}, C_{gd} of the device are the p-n junction depletion capacitance formulae and the Statz approach [64].

When FET is pinched off, the gate to source junction capacitance falls to a small value which is determined by the capacitance of the space charge region, setting the capacitance Cgs equals to zero causes discontinuity and results in convergence problems, thus, V_{new} is introduced which is equal to Veff1 in equation (13) before pinch-off and to Vt beyond pinchoff and thus V_{new} is given by

$$V_{new=}\frac{1}{2}(Veff1 + Vt + \sqrt{\Delta^2 + (Veff1 - Vt)^2}) \tag{18}$$

Where Δ is the voltage transition width, its arbitrary value used is 0.2. After introducing the function of equation (18) in place of Veff1, in equation (12), and partially differentiating equation(15) and equation (16) the equations(19) and(20) are obtained as follows

$$C_{gs}=\frac{0.25*Cgso}{\sqrt{1-\frac{Vnew}{Vb}}} \quad * \quad \left\{1 + \frac{(Veff-Vt)}{\sqrt{(Veff-Vt)^2+d^2}}\right\} \quad * \quad \left\{1 + \frac{(Vgs-Vgd)}{\sqrt{(Vgs-Vgd)^2+(\frac{1}{\alpha})^2}}\right\} + 0.5 * Cgdo *$$

$$\left\{1 - \frac{(Vgs-Vgd)}{\sqrt{(Vgs-Vgd)^2+(\frac{1}{\alpha})^2}}\right\} \tag{19}$$

$$C_{gd}=\frac{0.25*Cgso}{\sqrt{1-\frac{Vnew}{Vb}}} \quad * \quad \left\{1 + \frac{(Veff-Vt)}{\sqrt{(Veff-Vt)^2+d^2}}\right\} \quad * \quad \left\{1 - \frac{(Vgs-Vgd)}{\sqrt{(Vgs-Vgd)^2+(\frac{1}{\alpha})^2}}\right\} + 0.5 * Cgdo *$$

$$\left\{1 + \frac{(Vgs-Vgd)}{\sqrt{(Vgs-Vgd)^2+(\frac{1}{\alpha})^2}}\right\} \tag{20}$$

Where

$V_{new}=0.5(V_{eff}+V_t+\sqrt{(Veff - Vt)^2 + \Delta^2})$

$V_{eff}=0.5(V_{gs}+V_{gd}+\sqrt{(Vgs - Vgd)^2 + \Delta^2})$

$\Delta = 1 / \alpha$ = capacitance transition width (dc parameter width (V.),

C_{gs} =Gate-to-Source capacitance of a MESFET device

C_{gso}=Gate-to-Source capacitance at zero Vgs bias.

C_{gdo}=Gate-to-Drain capacitance at zero Vgs bias

C_{gd} = Gate-to-Drain capacitance of a MESFET device

α= parameter for simulating saturation voltage (dc parameter) (V^{-1})

V_t =threshold voltage or pinch-off voltage (V)

Equation (6) is more accurate than equation (17) and each junction capacitance is made as a function of V_{gs} and V_{gd}. The Statz approach is also valid under forward bias whereas the previous equation is not. However, this approach is quite lengthy and for circuits with a large number of devices the CPU execution speed may be unacceptable. Also it utilizes parameters ($V_{to,}$ α and Δ) which define dc behavior so that in many applications, the temptation to compromise the dc accuracy of the model in favor of the ac accuracy is there. This temptation is quite real since improvements in the CV modeling accuracy can be achieved by allowing these dc parameters to vary. Accurate simulation of the voltage dependency, for example C_{gs} on V_{ds}, is also very difficult to achieve [65]. In fact, in the saturation region C_{gs} is effectively independent of V_{ds}. The same restrictions also clearly apply to the simulation of C_{gd}.

CHAPTER-5

Results & Discussions

A physics based analytical modeling has been developed to evaluate the I-V characteristics, and extrinsic parameters: gate-source capacitance and gate-drian capacitance. This model incorporates a new emperical equaition for simulating the bias dependence junction capacitance of GaAs MESFET. The results of gate-source capacitance and gate-drian capacitance show an improvement of device performance by incorporating the new emperical eqution. This model shows the accurate results to develop the GaAs MESFET for high frequency performance.
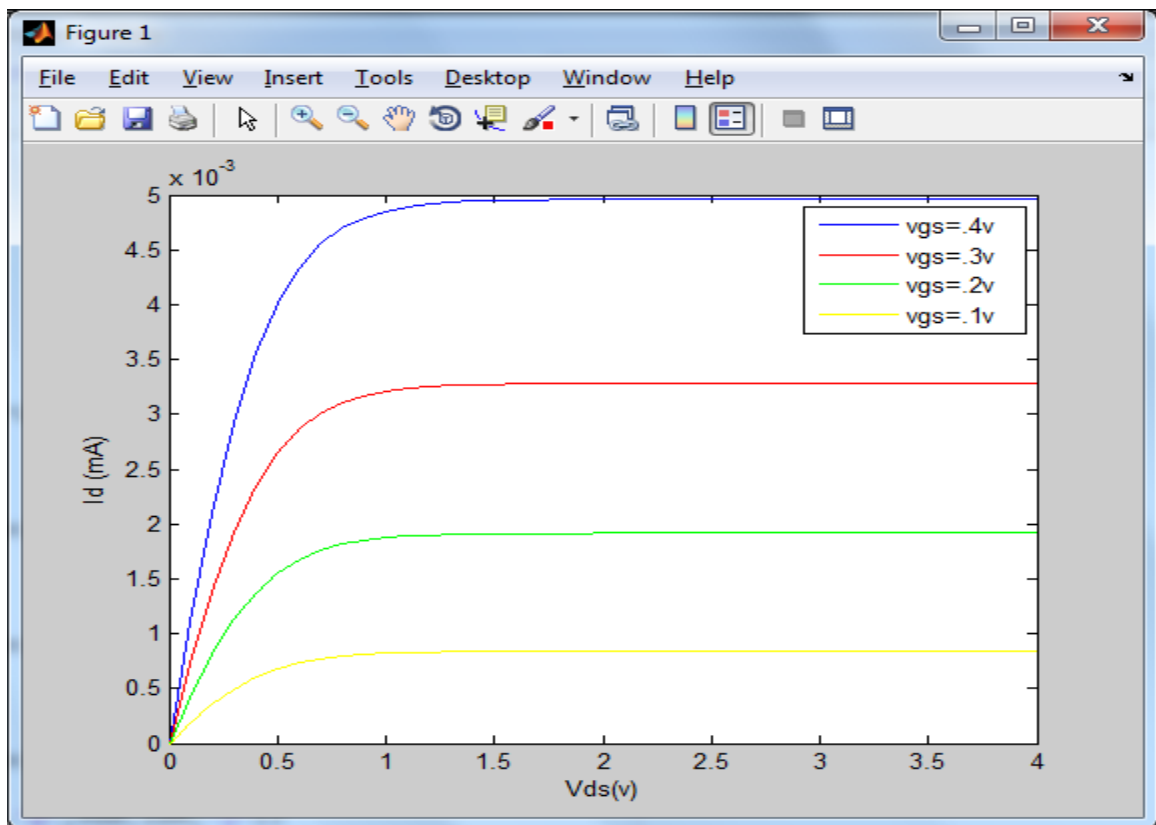

Figure 15 Plot of Current Voltage characteristics of GaAs MESFET for different gate-source biasing

Figure 15 shows a plot of drain current versus drain-source voltage for different gate-source voltage in the order of V_{GS} = 0.1, 0.2, 0.3 and 0.4V. The I-V characteristics in the plot shows that the drain current linearly increases up to 0.5mA at V_{DS} = 0.3V for V_{GS} = 0.1V, 1.25mA at V_{DS} = 0.4V for V_{GS} = 0.2V, 2.5mA at V_{DS} = 0.5V for V_{GS} = 0.3V and 4mA at V_{DS} = 0.65V for V_{GS} = 0.4V. The saturation drain currents in order of 0.65mA, 1.75mA, 3.2mA and 5mA have been observed at V_{Dsat} = 0.75V, 1V, 1.25V and 1.5 V for gate-source voltages V_{GS} = 0.1V, 0.2V, 0.3V and 0.4V respectively. The I-V characteristics obtained from improved analytical model clearly shows excellent properties of the linearity and non-linearity, which shows a potential improvement of device switching performance. The active channel concentration of N_D = 10^{17} cm^{-3} has been used to achieve the active channel depth to support the pinch-off voltaged indicated in the range of 1.5 – 2V and the substrate concentration N_A = 10^{15} cm^{-3} has been used to support the resonable break-down voltage. The curve of drain current versus drain-source voltage for different gate-source voltage has been plotted using the equation (4).

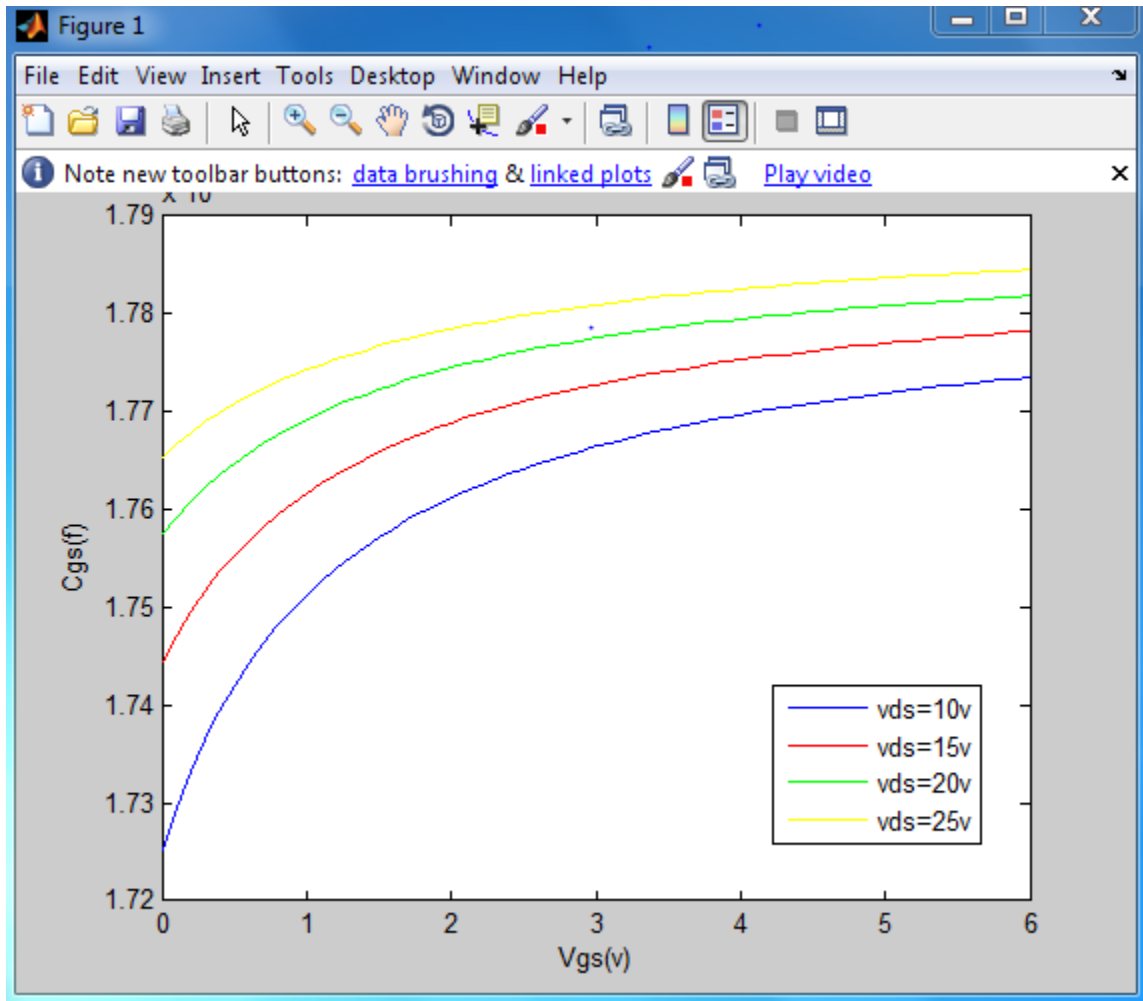**(2) Plot of gate to source capacitance versus the gate to source voltage.**

Figure 16 Plot Of Gate to source capacitance(Cgs) vs the gate to source voltage(vgs)

Figure 16 is a plot of gate-to-source capacitance (C_{gs}) versus the gate-to-source voltage (V_{gs}) for different drain-source voltages V_{DS} = 10, 15, 20 and 25V. The gate-source capacitance (C_{gs}) exponentially increases with increment of gate-source voltage (V_{gs}) in the range of 0-2V for all drain-source voltages and the slope of gate-source capacitance becomes low in the gate-source voltage range of 2 – 6V for all drain-source voltage. At the gate-source voltage variation range from 1V to 6V, the gate-source capaciatnces increase from 1.725 x10^{-13} to 1.774 x10^{-13}f for darin-source voltage V_{ds} =10, 1.745 x10^{-13} to 1.778 x10^{-13}f for darin-source voltage V_{ds} =15, 1.758 x10^{-13} to 1.782 x10^{-13}f for darin-source voltage V_{ds} =20, 1.765 x10^{-13} to 1.763 x10^{-13}f for darin-source voltage vds

=25. The plot of gate-to-source capacitance (C_{gs}) versus the gate-to-source voltage (Vgs) has been obtained by using the equation (19) and the plot shows a similar nature of Figure 11.

(3) Gate to Drain capacitance Vs drain to source voltage
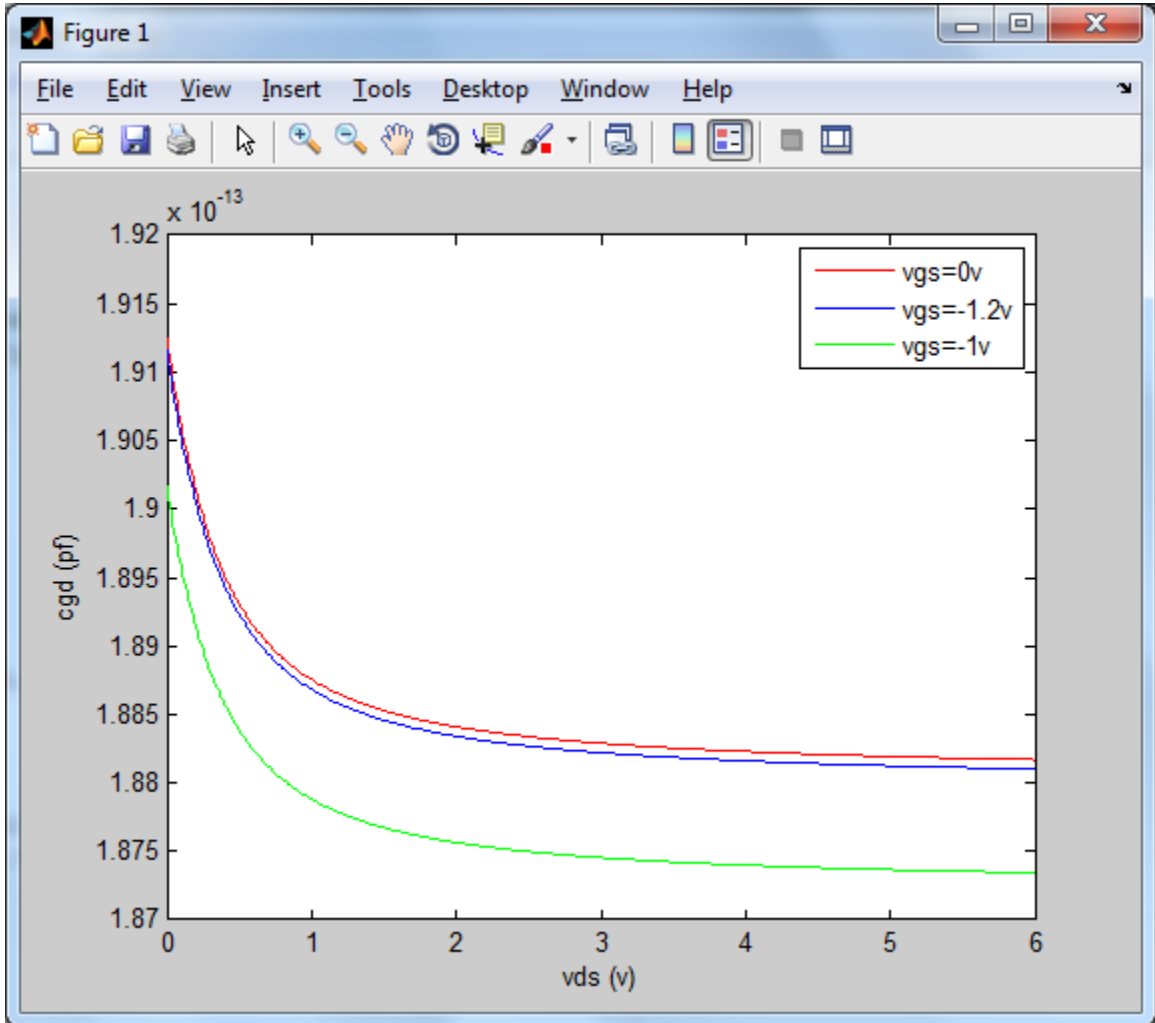
Figure 17 Plot of Gate to Drain capacitance (Cgd) Vs drain to source voltage (Vds)

Figure 17 is a plot of gate to drain capacitance (C_{gd}) versus the drain to source voltage (V_{ds}) for different gate-source voltages $V_{gs}=0$, -1.0, and -1.2. The gate-drain capacitance (C_{gd}) exponentially decreases with increment of drain-source voltage (V_{ds}) in the range of 0-1V for all gate-source voltages and the slope of gate-drain capacitance becomes low at the drain-source voltage range of 1 – 6V for all gate-source voltages. At the drain-source voltage variation range from 0V to 6V, the drain-source capacitance increase from

1.9 x10^{-13} to 1.874x10^{-13}f for gate-source voltage V$_{gs}$ = 0V, 1.91 x10^{-13} to 1.882x10^{-13}f for gate-source voltage V$_{gs}$ = -1.0V, and 1.92 x10^{-13} to 1.883 x10^{-13}f for gate-source voltage V$_{gs}$ = -1.2V. The plot of gate to drain capacitance (C$_{gd}$) versus the drain to source voltage (V$_{ds}$) has been drawn using the equation (20) and the plot shows a similar nature of Figure 12.

The analytical model of GaAs MESFET has been carried out with new emperical equation to determine the drain current, gate-source and gate-drain capacitance. The properties of these plots shows an accurate result of the electrical parameters and extrinsic parameters to precisely develop GaAs MESFET with high frequency performance.

CHAPTER 6

Conclusion

Analytical modeling with numerical calculations has been carried out for the evaluation of intrinsic parameters such as gate capacitances, current voltage characteristics of Gallium Arsenide MESFET with new expression.

The results of those intrinsic parameters such as gate-to-source capacitance and gate-to-drain capacitance indicates the excellent potential of the device over a wide range of silicon and Gallium Arsenide devices for the microwave circuit design applications and savings in the CPU execution speed over the existing techniques.

 The device performance of the Gallium Arsenide has begun to look very promising to use in microwave circuits design applications which leads to a substantial increase in the bias area over which the accuracy of nonlinear model remains high.

REFRENCES

[1]. Zhong, Zheng, Yong-Xin Guo, and Mook Seng Leong. "A Consistent Charge Model of GaAs MESFETs for -Band Power Amplifiers." Microwave Theory and Techniques, IEEE Transactions on (2011): 2246.

[2] Van den Bosch, S, and L Martens. "Fast and Accurate Extraction of Capacitance Parameters for the Statz MESFET Model." Microwave Theory and Techniques, IEEE Transactions on, (1997).

[3] Nguyen, N.X, J.P Ibbetson, J.C Yen, M.H Hashemi, and U.K Mishra. "Encapsulated GaAs Power MESFET." High Speed Semiconductor Devices and Circuits, 1993. Proceedings., IEEE/Cornell Conference on Advanced Concepts in, (1993).

[4]Watts,H.R, Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1993. Technical Digest 1993., 15th Annual

[5] M. Andersson, M. Åberg, H. Pohjonen Simultaneous Extraction of GaAs MESFET Channel and Gate Diode Parameters and its Application to Circuit Simulation Proceedings of IEEE Int. Symp. on Circuits and Systems Espoo, Finland, 7 - 9 June 1988, pp. 2601 – 2604.

[6]C. M. Snowden and R. R. Pantoja, "GaAs MESFET physical models for process-oriented design," IEEE Trans. Microw. Theory Tech., vol.40, no. 7, pp. 1401–1409, Jul. 1992.

[7] T. Takada, K. Yokoyama, M. Ida, and T. Sudo, "A MESFET variable capacitance model for GaAs integrated circuit simulation," IEEE Trans. Microw. Theory Tech., vol. MTT-30, no. 5, pp. 719–723, May 1982.

[8] T. Chen and M. Shur, "A capacitance model for GaAs mefsets," IEEE Trans. Electron Devices, vol. ED-12, no. 5, pp. 883–891, May 1985.

[9] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, and H. Zirath, "An empirical table-based FET model," IEEE Trans. Microw. Theory Tech.,vol. 47, no. 12, pp. 2350–2357, Dec. 1999.

[10] K. Koh, H. M. Park, and S. Hong, "A spline large-signal FET model based on bias-dependent pulsed I–V measurement," IEEE Trans. Microw. Theory Tech., vol. 50, no. 11, pp. 2598–2603, Nov. 2002.

[11] Zhong, Zheng, Yong-Xin Guo, and Mook Seng Leong. "A Consistent Charge Model of GaAs MESFETs for -Band Power Amplifiers." Microwave Theory and Techniques, IEEE Transactions on, (2011): 2246.

[12]. J. Rodriguez-Tellez, M. AI-Daas, and K. A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," IEEE Trans. Electron Devices, Apr. 1993.

[13]. S. M. Sze, Physics of Semiconducror Devices. New York: Wiley,1969.

[14] Handbook of Chemistry and Physics, 74th edition, edited by D. R. Lide (CRC Press, Boca Raton, 1994)] 13C18O

[15] H. Welker, Z. Naturforsch, Vol. A, No. 7, p. 744, 1952.

[16] Gallium Arsenide and Other Semiconductor Application Symposium, 2005. EGAAS 2005.

[17] S. M. Sze, Physics of Semiconductor Devices. New York: Wiley,1969.

[18] R. Williams, Modern GaAs Processing Methods, Artech House, Dedham, MA,

 [19]H. C. Casey, "Diffusion in III-V Compound Semiconductors," Atomic Diffusion in Semiconductors, D. Shaw, Editor, Plenum, New York, 1973.

[20] S. Y. Chiang, "Properties of Vacancy Defects in GaAs Single Crystals," J. Appl. Phys., Vol. 45, p. 2986, 1975.

 [21] S. Markram-Ebied, "Nature of EL2: The Main Native Midgap Electron Trap in VPE and Bulk GaAs," in Semi-insulating III-V Materials, D. Look, Editor, Shiva Publishing Ltd., England, 1984.

 [22] Kramer, D.A. (1988) Gallium and Gallium Arsenide: Supply, Technology, and Uses. Information Circular 9208, Washington DC, US Department of the Interior, Bureau of Mines

[21] Sabot JL, Lauvray H; Kirk-Othmer Encycl Chem Technol. 4th ed. NY, NY: John Wiley and Sons, 12: 299-317 (1994)

[22] Kitsunai, M. & Yuki, T. (1994) Review: How gallium arsenide wafers are made. Appl. organometal.

[23] Kramer, D.A. (2003) Mineral Commodity Summary: Gallium, Reston, VA, US GeologicalSurvey

[24] Harrison, R.J. (1986) Gallium arsenide. In: LaDou, J., ed., Occupational Medicine: The Microelectronics Industry, Vol. 1, Philadelphia, PA, Hanley & Belfus, pp. 49–58

[25] Chakrabarti, N.B. (1992) GaAs integrated circuits. J. Inst. Electron. Telecommun. Eng., 38, 163–178

[26] Greber, J.F. (2003) Gallium and gallium compounds. In: Ullmann's Encyclopedia of Industrial Chemistry, 6th rev. Ed., Vol. 15, Weinheim, Wiley-VCH Verlag GmbH & Co., pp. 235–240

[27]Sabot, J.L. & Lauvray, H. (1994) Gallium and gallium compounds. In: Kroschwitz, J.I. & Howe-Grant, M., eds, Kirk-Othmer Encyclopedia of Chemical Technology, 4th Ed., Vol. 12, New York,John Wiley & Sons, pp. 299–317

[28] Beliles, R.P. (1994) The metals. In: Clayton, G.D. & Clayton, F.E., eds, Patty's Industrial Hygieneand Toxicology, 4th Ed., Vol. 2C, John Wiley & Sons, New York, pp. 1879–2013

[29] Harrison, R.J. (1986) Gallium arsenide. In: LaDou, J., ed., Occupational Medicine: The Microelectronics Industry, Vol. 1, Philadelphia, PA, Hanley & Belfus, pp. 49–58

[30] W. R. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," IEEE Transactions on Microwave

[31] B. Ooi et al., "A Novel Approach for Determining the GaAs MESFET Small-Signal Equivalent-Circuit Elements," IEEE Transactions on Microwave Theory and Techniques, Vol. 45, No. 12, pp. 2084-2088, Dec. 1997.

[32] J. Rodriguez-Tellez, M. AI-Daas, and K. A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," IEEE Trans. Electron Devices, Apr. 1993.

[33]S . M. Sze, Physics of Semiconducror Devices. New York: Wiley, 1969.

[34]W . R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," IEEE Trans. Microwave Theory Te ch. , vol. MTT-28, no. 5, pp. 448-456, 1980. H. Statz, P. Newman, I. W . Smith, R. A. Pucel, and H. A. Haus,

[35] D. Haigh and J. Everard, GaAs Technology and its Impact on Circuits and Systems. UK: Peter Peregrinus Ltd 1989.

 [36]N. Scheinberg, R. J.Bayruns, P. W. Wallace, and R. Goyal, "An accurate MESFET model for linear and microwave circuit design," IEEE J . Solid-State Circuits, vol. 24, no. 2, pp. 532-538, Apr. 1989.

[37] Rodriguez-Tellez, K . A. Mezher, 0. M. Conde Portilla, and J. C. Luengo Patrocinio, "A new highly accurate microwave nonlinear MESFET model," Microwave J . , vol. 36, no. 5, pp. 280-285, May 1993.

[38] J.A. Nelder, "A simplex model for function minimization," Computer. J vol. 7, p. 308, Mar. 1964. D. Haigh and J. Everard, GaAs Technology and its Imp

[38] D. Haigh and J. Everard, GaAs Technology and its Impact on Circuits and Systems. UK: Peter Peregrinus Ltd 1989.

[39] P. H. Ladbrooke, MMIC Design: GaAs F E T s and HEMTs. Nonvood, MA: Artech, 1989, ch. 6.

[40] "GaAs FET device and circuit simulation in SPICE," IEEE Trans. Electron Devices, vol. ED-34, pp. 160-169, Feb. 1987. 1 H. Statz, H. A. Haus, and R. A. Pucel, "Noise characteristics of GaAs field effect transistors," IEEE Trans. Electron Devices, vol. ED-21,

[41] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of GaAs microwave field effect transistors," Advances in Electronics and Electron Physics, L. Marton, Ed., vol. 38. New York: Aca- demic, 1975, pp. 195-265.

[42] S . E. Sussman-Fort, S . Narasimhan, and K . Mayaram, "A complete GaAs MESFET computer model for SPICE," IEEE Trans. Electron Devices, vol. ED-32, pp. 471-473, 1984.

[43] M. S . Shur, "Analytical models of GaAs FET's," IEEE Trans. Elec- tron Devices, vol. ED-32, pp. 70-72, 1985.

[44] J . M. Golio, J . R. Hauser, and P. A. Blakey, "A large-signal GaAs MESFET model implemented on SPICE," IEEE Circuits Devices Mag. , vol. 1, pp. 21-29, 1985.

[45] A. van der Ziel, "Gate noise in field effect transistors at moderately high frequencies," Proc. IEEE, vol. 51, pp. 461-467, 1963.

[46] T.Takada, K.Yokoyama, M. Ida, and T. Sudo, "A MESFET vari- able-capacitance model for GaAs integrated circuit simulation," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp. 719-724, 1982.

[47] T. H. Chen and M. S .Shur, "A capacitance model for GaAs MESFET's," IEEE Trans. Electron Devices, vol. ED-32, pp. 883- 891, 1985. 191 H. C. Poon and H. K. Gummel, "Modeling of emitter capacitance,"

[48] J. Rodriguez-Tellez, M. AI-Daas, and K. A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," IEEE Trans. Electron Devices, Apr. 1993.

[49] W . R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," IEEE Trans. Microwave Theory Te ch. , vol. MTT-28, no. 5, pp. 448-456, 1980. H. Statz, P. Newman, I. W . Smith, R. A. Pucel, and H. A. Haus.

[50] A. van der Ziel, "Gate noise in field effect transistors at moderately high frequencies," Proc. IEEE, vol. 51, pp. 461-467, 1963.

[51] Zhong, Zheng, Yong-Xin Guo, and Mook Seng Leong. "A Consistent Charge Model of GaAs MESFETs for -Band Power Amplifiers." Microwave Theory and Techniques, IEEE Transactions on, (2011): 2246.

[52] M. Andersson, M. Åberg, H. Pohjonen Simultaneous Extraction of GaAs MESFET Channel and Gate Diode Parameters and its Application to Circuit Simulation Proceedings of IEEE Int. Symp. on Circuits and Systems Espoo, Finland, 7 - 9 June 1988, pp. 2601 – 2604.

[53] B. Ooi et al., "A Novel Approach for Determining the GaAs MESFET Small-Signal Equivalent-Circuit Elements," IEEE Transactions on Microwave Theory and Techniques, Vol. 45, No. 12, pp. 2084-2088, Dec. 1997.

[54] J. Rodriguez-Tellez, M. AI-Daas, and K. A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," IEEE Trans. Electron Devices, Apr. 1993.

[55] GaAs FET device and circuit simulation in SPICE," IEEE Trans. Electron Devices, vol. ED-34, pp. 160-169, Feb. 1987. 1 H. Statz, H. A. Haus, and R. A. Pucel, "Noise characteristics of GaAs field effect transistors," IEEE Trans. Electron Devices, vol. ED-21,

[56] T. Takada, K. Yokoyama, M. Ida, and T. Sudo, "A MESFET variable capacitance model for GaAs integrated circuit simulation," IEEE Trans. Microw. Theory Tech., vol. MTT-30, no. 5, pp. 719–723, May 1982.

[57] J. Rodriguez-Tellez, M. AI-Daas, and K. A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," IEEE Trans. Electron Devices, Apr. 1993.

[58] "GaAs FET device and circuit simulation in SPICE," IEEE Trans. Electron Devices, vol. ED-34, pp. 160-169, Feb. 1987. 1 H. Statz, H. A. Haus, and R. A. Pucel, "Noise characteristics of GaAs field effect transistors," IEEE Trans. Electron Devices, vol. ED-21.

[59] T. H. Chen and M. S .Shur, "A capacitance model for GaAs MESFET's," IEEE Trans. Electron Devices, vol. ED-32, pp. 883- 891, 1985. 191 H. C. Poon and H. K. Gummel, "Modeling of emitter capacitance".

[60] N. Scheinberg, R. J.Bayruns, P. W. Wallace, and R. Goyal, "An accurate MESFET model for linear and microwave circuit design," IEEE J . Solid-State Circuits, vol. 24, no. 2, pp. 532-538, Apr. 1989.

[61] B. Ooi et al., "A Novel Approach for Determining the GaAs MESFET Small-Signal Equivalent-Circuit Elements," IEEE Transactions on Microwave Theory and Techniques, Vol. 45, No. 12, pp. 2084-2088, Dec. 1997.

[62] J. Rodriguez-Tellez, M. AI-Daas, and K. A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," IEEE Trans. Electron Devices, Apr. 1993.

[63] Zhong, Zheng, Yong-Xin Guo, and Mook Seng Leong. "A Consistent Charge Model of GaAs MESFETs for -Band Power Amplifiers." Microwave Theory and Techniques, IEEE Transactions on, (2011): 2246.

[64] T.Takada, K.Yokoyama, M. Ida, and T. Sudo, "A MESFET vari- able-capacitance model for GaAs integrated circuit simulation," IEEE Trans. Microwave Theory Tech., vol. MTT-30, pp. 719-724, 1982.

[65] W . R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," IEEE Trans. Microwave Theory Te ch. , vol. MTT-28, no. 5, pp. 448-456, 1980. H. Statz, P. Newman, I. W . Smith, R. A. Pucel, and H. A. Haus.

APPENDIX – A

Notations and Symbols Used:

α alpha   hyperbolic tangent parameter

β BETA   transconductance coefficient

C_{gdo} Zero-bias/asymptotic gate-drain capacitance

C_{gso} Zero-bias/asymptotic gate-source capacitance

Δ   Beyond-pinchoff capacitance interpolation voltage range

Esat   Electron velocity saturation field

FET   Field Effect Transistor

C_{gd} Gate-Drain capacitance

C_{gs} Gate-Source capacitance

G_m Transconductance

V_{bs} Substrate to source voltage

V_{gs} Gate-Source voltage

V_{ds} Drain-Source voltage

V_t Threshold voltage

V_{bi} Build in Voltage of active channel and Substrate junction

V_p Pinch-off Voltage

Z   channel width

APPENDIX – B

Matlab Codes

    (1) Current voltage chracteristics

```
vt=-1.21;
beta=1.36*10e-3;
alpha=2.25;
lambda=35.23*10-3;
vgs=.4;
vds=0:0.1:3;
x=vgs-vt;
x1=(1+lambda*vgs);
x2=alpha*vds;
id=beta*(x).^2*(x1)*tanh(alpha*vds)*10e-4;
vgs1=.3;
x3=vgs1-vt;
x4=(1+lambda*vgs1);
id2=beta*(x3).^2*(x4)*tanh(alpha*vds)*10e-4;
vgs2=.2;
x5=vgs2-vt;
x6=(1+lambda*vgs2);
id3=beta*(x5).^2*(x6)*tanh(alpha*vds)*10e-4;
vgs3=.1;
x7=vgs3-vt;
x8=(1+lambda*vgs3);
id4=beta*(x7).^2*(x8)*tanh(alpha*vds)*10e-4;
 plot(vds,id,'b',vds,id2,'r',vds,id3,'g',vds,id4,'y');
xlabel('Vds(v)');
ylabel('Id (mA)');
```

(2)Gate to source capacitance versus gate to source voltage Cgs vs Vgs

```
cgs0=.103*10e-12;
cgd0=.018*10e-12;
vbi=0.77;
alpha=2.58;
delta=0.1512;
vb=0.77;
d=0.2;
vt0=0.1;
vds=0:0.1:6;
%vds=-3:1:3;

vgs1=10;
vgd=vds-vgs1;
a1=(vgs1-vgd).^2;
a2=(delta)^2;
a3=vgs1+vgd;
a4=sqrt(a1+a2);
veff=0.5*(a3+a4);
b1=(veff-vt0).^2;
b2=(veff+vt0);
b3=(d)^2;
b4=sqrt(b1+b3);
vnew=0.5*(b2+b4);

c1=(1-(vnew./vb));
c2=sqrt(c1);
```

```
c3=0.25*cgs0;
c4=veff-vt0;
c5=(c4).^2;
c6=sqrt(c5+b3);
c7=1+(c4./c6);
c8=vgs1-vgd;
c9=(1/alpha)^2;
c10=(c8).^2.;
c11=sqrt(c10+c9);
c12=1+(c8/c11);

d1=0.5*cgd0;
d2=1-(c8/c11);
d3=d1*d2;

Cgs1=((c3./c1).*(c7).*(c12))+(d3);

vgs2=15;
vgd1=vds-vgs2;
a11=(vgs2-vgd1).^2;
a12=(delta)^2;
a13=vgs2+vgd1;
a14=sqrt(a11+a12);
veff1=0.5*(a13+a14);
b11=(veff1-vt0).^2;
b12=(veff1+vt0);
b13=(d)^2;
b14=sqrt(b11+b13);
vnew1=0.5*(b12+b14);

c11=(1-(vnew1./vb));
```

```
c12=sqrt(c11);
c13=0.25*cgs0;
c14=veff1-vt0;
c15=(c14).^2;
c16=sqrt(c15+b13);
c17=1+(c14./c16);
c18=vgs2-vgd1;
c19=(1/alpha)^2;
c110=(c18).^2.;
c111=sqrt(c110+c19);
c112=1+(c18/c111);

d11=0.5*cgd0;
d12=1-(c18/c111);
d13=d11*d12;

Cgs2=((c13./c11).*(c17).*(c112))+(d13);

 vgs3=20;
vgd2=vds-vgs3;
p11=(vgs3-vgd2).^2;
p12=(delta)^2;
p13=vgs3+vgd2;
p14=sqrt(p11+p12);
veff2=0.5*(p13+p14);
q11=(veff2-vt0).^2;
q12=(veff2+vt0);
q13=(d)^2;
q14=sqrt(q11+q13);
vnew2=0.5*(q12+q14);
```

```
r11=(1-(vnew2./vb));
r12=sqrt(r11);
r13=0.25*cgs0;
r14=veff2-vt0;
r15=(r14).^2;
r16=sqrt(r15+q13);
r17=1+(r14./r16);
r18=vgs3-vgd2;
r19=(1/alpha)^2;
r110=(r18).^2.;
r111=sqrt(r110+r19);
r112=1+(r18/r111);
s11=0.5*cgd0;
s12=1-(r18/r111);
s13=s11*s12
Cgs3=((r13./r11).*(r17).*(r112))+(s13);


Vgs4=25;
Vgd4=vds-vgs4;
t11=(vgs4-vgd4).^2;
t12=(delta)^2;
t13=vgs4+vgd4;
t14=sqrt(t11+t12);
veff2=0.5*(t13+t14);
h11=(veff4-vt0).^2;
h12=(veff4+vt0);
h13=(d)^2;
h14=sqrt(h11+h13);
vnew2=0.5*(h12+h14);
```

```
j11=(1-(vnew4./vb));
j12=sqrt(r11);
j13=0.25*cgs0;
j14=veff4-vt0;
j15=(r14).^2;
j16=sqrt (r15+h13);
j17=1+(r14./r16);
j18=vgs4-vgd4;
j19=(1/alpha)^2;
j110=(r18).^2.;
j111=sqrt(r110+r19);
j112=1+(r18/r111);
j11=0.5*cgd0;
j12=1-(r18/r111);
u13=u11*u12
Cgs4=((j13./j11).*(j17).*(j112))+(u13);

plot(vgs,Cgs1,'r',vgs,Cgs2,'g',vgs,Cgs3,'b',vgs,Cgs4,'y');
```

(3) Gate to drain capacitance versus drain to source voltage Cgd vs Vds
```
cgs0=.103*10e-12;
cgd0=.018*10e-12;
vto=-2.183;
vb=0.77;
delta=0.663;
d=0.2;
alpha=1.508;
vgs=0;
vds=0:0.01:6;
vgd=vgs-vds;
```

```
veff=0.5*(vgs+vgd+sqrt((vgs-vgd).^2+delta.^2));
vnew=0.5*(veff+vto+sqrt((veff-vto).^2+d.^2));
x2=sqrt(1-(vnew/vb));
x1=0.25*cgs0;
x3=veff-vto;
x4=sqrt((veff-vto).^2+d.^2);
x5=x3/x4;
x6=vgs-vgd;
x7=sqrt((vgs-vgd).^2+(1/alpha).^2);
x8=x6/x7;
w=(x1.*(1+x5).*(1-x8))./x2+0.5.*cgd0.*(1+x8);


vgs1=-1.2;
vgd1=vgs1-vds;
veff1=0.5*(vgs1+vgd1+sqrt((vgs1-vgd1).^2+delta.^2));
vnew1=0.5*(veff+vto+sqrt((veff-vto).^2+d.^2));
x21=sqrt(1-(vnew1/vb));
x11=0.25*cgs0;
x31=veff1-vto;
x41=sqrt((veff1-vto).^2+d.^2);
x51=x31/x41;
x61=vgs1-vgd1;
x71=sqrt((vgs1-vgd1).^2+(1/alpha).^2);
x81=x61/x71;
w1=(x11.*(1+x51).*(1-x81))./x21+0.5.*cgd0.*(1+x81);


 vgs2=-1;
vgd2=vgs2-vds;
veff2=0.5*(vgs2+vgd2+sqrt((vgs2-vgd2).^2+delta.^2));
vnew2=0.5*(veff+vto+sqrt((veff-vto).^2+d.^2));
x22=sqrt(1-(vnew2/vb));
```

```
x12=0.25*cgs0;

x32=veff1-vto;

x42=sqrt((veff2-vto).^2+d.^2);

x52=x32/x42;

x62=vgs2-vgd2;

x72=sqrt((vgs2-vgd2).^2+(1/alpha).^2);

x82=x62/x72;

w2=(x12.*(1+x52).*(1-x82))./x22+0.5.*cgd0.*(1+x82);

plot(vds,w,'r',vds,w1,'b',vds,w2,'g');

xlabel('vds (v)');

ylabel('cgd (pf)');
```