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ANALYTICAL MODELING OF SILICON CARBIDE MESFET

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By:

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ABSTRACT

ANALYTICAL MODELING OF SILICON CARBIDE MESFET USING MATLAB

By

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This study concentrates on analytical modeling of silicon carbide MESFET device using MATH Lab software. In this study, an analytical simulation has been proposed to find the characteristics of SIC MESFET, firstly the complete theory and physics of the MESFET device, the conception of the MESFET device include the Schottky barrier, Schottky contact, and the charge phenomena in the channel of the MESFET device. In addition, the includes the discussion of theoretical simulations of channel current versus device thickness, channel versus device thickness, transconductance versus device thickness, charge versus device thickness, gate to source capacitance, drain to gate capacitance, switching time versus device thickness, switching time versus power in SIC MESFET. Finally, this analytical modeling has been concluded by using simulation of MATH LAB software. The simulation results of a silicon carbide (SiC) substrate MESFET device, it is including the channel current versus device thickness, channel versus device thickness, transconductance versus device thickness, charge versus device thickness, switching time versus thickness, switching time versus gate voltage, switching time versus gate length.

1. INTRODUCTION

Silicon carbide (SiC)-based semiconductor electronic devices and circuits are presently being developed for use in high-temperature, high-power, and high-radiation conditions under which conventional semiconductors cannot adequately perform. Silicon carbide's ability to function under such extreme conditions is expected to enable significant improvements to a far-ranging variety of applications and systems. These range from greatly improved high-voltage switching for energy savings in public electric power distribution and electric motor drives to more powerful microwave electronics for radar and communications to sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines [1-2].

Silicon carbide devices have received increased attention in recent years for high-power microwave devices due to the unique combination of high electron velocity, high electric field breakdown strength, and high thermal conductivity of Sic. Among the various poly types of Sic, 6H has received the most attention so far due to the maturity of its crystal growth procedures. Half-micron gate length MESFET's fabricated in high-resistivity 6H-Sic have already shown f_{max} of 25 GHz [3], and RF power output [4] of 3.5 W at 6 GHz with 45.5% power added efficiency. Further significant improvements in both the frequency and power performance of Sic MESFET's can be obtained by using the 4H-polytype of Sic due to its higher electron mobility, and lower ionization energy for donors compared to 6H-Sic. Weitzel et al. [5] have reported power density of 2.8 W/mm at 1.8 GHz and f_{max} of 12.8 GHz for 4H-MESFET's on conducting p-type substrates. The Sic polytype that has received the most attention in the last few years has been 6H-SiC, since it has the best crystal quality of the established polytype. Submicron's MESFET's have been fabricated in 6H-Sic and have demonstrated desirable microwave performance [6]-[7].

1.1 Power Aided Efficiency of SiC and GaN based MESFET

High power Silicon Carbide devices are expected to play an important role in the switching circuit, protection circuits in to the power system. In addition, it is also applied on the rectifier circuit. The future for SiC looks very bright indeed now that commercial

Products have hit the marketplace [8]. Packaged 30mm SiC MESFET transistors were demonstrated with peak power density of 1.9W/mm and power-added-efficiency (PAE) of 53%. The target application of these devices is L-band communication. Discrete devices with gate dimension of 2□~ 400μm show a saturation current density of 320mA/mm and an extrinsic trans conductance of 25mS/mm. The cut-off and maximum oscillation frequency of these devices was 12GHz and 17GHz, respectively. Large periphery devices with 10W CW output power rating exhibit stable electrical performance over a period of 1100 hours, with less than ±10% drift in drain-source current under continuous DC stress [9]. Previous efforts have revealed instabilities in standard SiC MESFET device electrical characteristics, which have been attributed to charged surface states. This work describes the use of an undoped "spacer" layer on top of a SiC MESFET to form a "buried-channel" structure where the active current carrying channel is removed from the surface. By using this approach, the induced surface traps are physically removed from the channel region, such that the depletion depth caused by the un-neutralized surface states cannot reach the conductive channel. This results in minimal RF dispersion ("gate lag") and, thus, improved RF performance [10].

Furthermore, the buried-channel approach provides for a relatively broad and uniform transconductance (g_m) with gate bias (V_{gs}), resulting in higher efficiency MESFETs with improved linearity and lower signal distortion. SiC MESFETs having 4.8-mm gate periphery were fabricated using this buried-channel structure and were measured to have an output power of 21 W (4. 4 W/mm), 62% power added efficiency, and 10.6 dB power gain at 3 GHz under pulse operation. When operated at continuous wave, similar 4.8-mm gate periphery SiC MESFETs produced 9.2W output power (2 W/mm), 40% PAE, and 7 dB associated gain at 3 GHz . Silicon carbide MESFET's with 0.7 pm x 332 pm gates under Class B bias at 1.8 GHz had 28.3 dB/m (2 W/mm CW) and 'iO.4% PAE. At the same power density, these FET's had 66% PAE at 0.85 GHz. This high power density combined with the extremely high thermal conductivity off Sic makes it a promising technology for high power microwave applications [11]. A high-efficiency and low-distortion GaAs power MESFET using direct ion implantation technology for the digital wireless personal handy-phone system (PHS). When qualified by 1.9-GHz Pi/4-shifted quadrature phase shift keying (QPSK) modulated PHS standard signals, the

2.2-V-operation device with a gate width (Wg) of 2 mm exhibited a power-added efficiency (PAE) of 57.2% and an adjacent channel leakage power (P_{adj}) of 58 dB at an output power of 21.3 dB. The MESFET with the optimized direct ion implantation conditions and fabrication process achieved the highest PAE for PHS applications. The low-cost MMIC-oriented direct ion implantation technology has demonstrated the state-of-the-art results for new-generation PHS handsets for the first time [12].

Silicon carbide (SiC) MESFETs were fabricated using a standard SiC MESFET structure with the application of the "buried-channel" and field-plate (FP) techniques in the process. FPs combined with a buried-gate is shown to be favorable concerning output power density and power-added efficiency (PAE), due to higher breakdown voltage and decreased output conductance. A very high power density of 7.8 W/mm was measured on-wafer at 3 GHz for a two-finger 400-μm gate periphery SiC MESFET. The PAE for this device was 70% at class AB bias. Two-tone measurements at 3 GHz±100 kHz indicate an optimum FP length for high linearity operation. Significant results of measurement and calculation of power-added efficiency (PAE) and drain efficiency are presented for MESFET's that use GaAs-on-insulator. Ultrahigh PAE of 89% was obtained at 8 GHz with a gain of 9.6 dB using a 3-V supply. When the voltage was increased to 4 V, the peak PAE was 93% at 210 mW/mm with 9.2-dB gain. The ideal current–voltage characteristics with practically zero leakage current and large trans conductance near pinch off yielded PAE values approaching the theoretical limits of overdriven operation. The application of conventional assumptions concerning drain efficiency is discussed relative to devices that approach these theoretical limits. Also discussed are the pitfalls of various figures of merit of efficiency when applied to these devices [13].

SiC MESFET's for high power output; we recently reported 80 watts CW output power with 31% power-added efficiency (PAE) at 3.1 GHz, from a single MESFET device with 48 mm of gate periphery operated in a hybrid circuit [14]. For much smaller devices (W, = 250 pm), we have recently achieved 5.2 W/mm with 11.1 dB associated gain and 63% PAE at 3.5 GHz, a result we have not previously reported. We have extended this S-band MESFET technology to X band, and we now report the

demonstration of over 30 watts of output power at 10 GHz from a single 12-mm Sic transistor under pulsed-mode conditions. FEATURES of wide-bandgap semiconductors that provide high RF power density, excellent power-added efficiency (PAE) performance, high breakdown voltage, high-frequency operation, small die size, and less complex amplifier arrangement make such technology a serious challenge to silicon LDMOS devices for high-power applications [15]–[19].

Over the last years, many authors have utilized these superior features of SiC MESFETs and have applied them in the development of different generations of power amplifiers (PAs) for use in digital audio and video broadcasting [20], [21] and aerospace and military systems [22]–[24]. A comparison of Si, GaAs, and SiC MESFET power densities indicates that SiC is a very promising material for high-power and high-frequency operation [25]. A serious problem of wide-band PAs, especially in the GaAs field effect transistor (FET) and GaAs monolithic-microwave integrated- circuit (MMIC) cases [26, 27] is the output matching because of the low intrinsic device impedance. Depending on the amplifier data, this problem can be mostly overcame only by using (external) transmission-line transformers that strongly limit the total bandwidth. The SiC-MESFET technology avoids this drawback and provides high large-signal output impedance because of its high drain–source breakdown voltage. In hybrid arrangements, as in this study, the advantages of GaAs and SiC can be combined successfully. As a first step, we have introduced an ultra-broad-band SiC MESFET 5-W single-stage PA in [28].

A comparison of Si, GaAs and SiC MESFET power densities indicates, that SiC is a promising material for high power operation [29]. The high breakdown voltage, large energy band gap and high thermal conductivity [30]-[31] are the main advantages of wide band gap semiconductors. To deliver large amounts of power to the antenna the mobile unit of many of today's wireless communications systems require a power amplifier; for this reason, the PA can dominate the power consumption of the transceiver. As a result, one of the key performance measures of a PA is the efficiency (a), which is the ratio of the power delivered to the antenna to the power drawn from the supply. In general, high efficiency PAs are achieved at the cost of linearity. Several communications standards utilize constant envelope modulation schemes, which allow for the use of non-linear PA

topologies. Class a PA provides high linearity but have poor efficiency (around 3000 in practice). Class B and AB Power Amplifiers provide higher efficiencies at the cost of a reduction in linearity, but still the efficiency can be boosted by using an even more non-linear PA. In Class-C operation, the power consumed in the device is less (the simultaneous high voltage and current is almost zero for the greater portion of the cycle). Therefore the class-C power amplifier can achieve higher efficiencies than Class A, AB & B. A common application of Class-C amplifiers is in Radio Frequency (RF) transmitters, where the input signal is used to switch the device on and off. These current pulses flow through a tuned circuit, which reduce the distortion by using tuned loads on the amplifier stage. In this paper the high efficiency, pulse input Class C PA topology is being investigated at 500MHz and 1GHz using physical model of SiC MESFET in TCAD [32]. Ion-implantation GaAs MESFETs were improved for Ku-band applications. Over 20% of the power added efficiency (PAE) was achieved at -25 dB of third order of intermodulation distortion ratio (IM3) at 14.5 GHz. In order to achieve high PAE and low IM3, the carrier profile was designed by using ion-implantations and the Trans conductance (gm) along the load-line was measured. This PAE was 5% higher than conventional MESFET, HFET and pHEMT [33]. Metal-semiconductor-field-effect-transistors (MESFETs) have been fabricated using a 150 nm partially depleted silicon-on-insulator CMOS technology. A peak f_{max} of 40GHz and peak breakdown voltages of up to 12V were measured. Comparatively, the CMOS transistors on the same process have a maximum steady-state voltage limit of 1.95V. TOM3 model for MESFET developed in ADS. The demonstrated high cut-off frequency and high voltage operation capability make the SOI MESFET a good device candidate for integrated radio frequency (RF) power amplifiers (PA). A cascaded MOS-MES RF PA architecture is proposed and simulated in ADS using the TOM3 model. Simulation results show 75% PAE while delivering 24dBm output power [34]. Very high power densities have been shown for both Sic MESFET and GaN HEMT devices. Both of these active devices benefit from the high breakdown voltages afforded by their wide-bandgap semiconductor properties. The GaN device also benefits from current densities as high as 1 A/mm^2 .This high power density, along with good efficiency and linearity, provide an excellent base for future military and commercial power amplifier applications. High power densities are possible

using narrow band power-matching networks. Although the gain bandwidth limitation is due to the high impedance load lines required, high power design is possible even over multiactive bandwidths [35].

A state-of-the-art GaAs power MESFET operating at a drain bias of 2.9 V has been developed using the high-low doped channel structure grown by molecular beam epitaxy. The device has 0.6 pm gate length and 16 mm gate width. The power frequency was output power of 31.5 dB with 11.5 dB gain and 64% power-added efficiency [36]. Advanced high performance hand-held phone requires highly efficient medium-power transistors with a low operation voltage since the total size and weight of the phone can be drastically reduced as the number of battery cells decreases. Recent advances in material preparation and device fabrication techniques have resulted in L-band GaAs power FET's operating at low drain voltages of 3.0 V to 3.5 V with respectable output power and efficiencies [37]-[39]. In this paper, we report a low-high doped GaAs power MESFET that was optimized for highly efficient medium-power operation at a drain bias lower than 3.0 V. The state-of-the-art RF performance of power FET has been achieved in this work, which is better than the best results reported in GaAs power MESFET [40]. A SiC MESFET with 42mm of gate periphery on a single die had a maximum RF output power of 53 watts CW with 37% power added efficiency (PAE) at 3.0 GHz. The Un precedence power from a die with an area od only mm^2 demonstrates the extremely high power handling capability of Sic microwave devices, Additionally there few SiC MESFET showing 2.5 W/mm with 41% PAE at 8 GHz [41]. In recent years, SiC has emerged as the ideal material for high power, high frequency and high temperature applications [42]. SiC have a wider bandgap of 3.3 eV and a higher thermal conductivity of 4.5 W/cm-K compared to Si for which the respective quantities are l. l eV and 1.5 W/cm-K [43, 44]. These allow SiC-based devices to operate at higher power levels. Besides, the lower relative dielectric constant of SiC (9.7) as compared to Si (11.8) and moderate electron mobility of SiC (900 cm2/V-s) as compared to Si (1350 cm W/V-s) allow SiC based devices to operate at higher frequencies.

Better thermal stability of SiC allows the device to operate at higher temperature. The performances of SiC-based devices are limited by the presence of traps located at the

surface between gate and drain, and in the substrate. Recently, both surface and substrate trapping effects of SiC MESFETs have been reported [45-47]. The surface trapping effects can be limited by using a passivation layer of Si3N4 [48]. It has been shown by Noblanc et al. [49] that the buffer layer plays a critical role in the mitigation of the substrate trapping phenomena. Presently, the use of a buffer layer is a ubiquitous method for combating the substrate trapping effects in SiC MESFETs.

In order to study compares current and projected state-of-the-art microwave power amplifiers used in spaceborne transmitter technologies at frequencies through 100 GHz. Projected are future trends in power PHEMTs and in wide bandgap semiconductor devices such as GaN and Sic. Also, the more established InP HEMT low-noise devices are examined for possible power amp applications specifically in the millimeter wave region. Three key power amplifier technologies, including the Traveling Wave Tube Amplifier (TWTA), the Solid State Power Amplifier (SSPA), and the Microwave Power Module (MPM), have emerged in varying degrees as heritage and or viable components in spacebome transmitters. Addressed as figures of merit are significant discriminators such as long term reliability, space heritage (Murfree on orbit performance), process/device maturity, size, weight, and efficiency [50].The comparisons for GaN and SiC IV characteristics is a given in below figures 1-6 [51]. The graphs clearly explain that the GaN has higher drain current when compared to SiC MESFET. Figures 1 and 2 has same gate length of 2 µm and figures 3 and 4 have the same gate length of 2.6 µm.

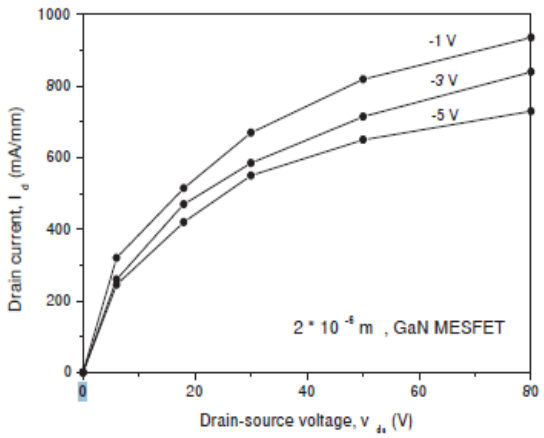

Figure 1

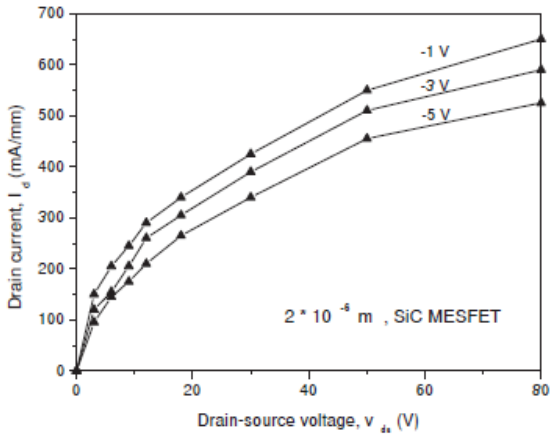

Figure2

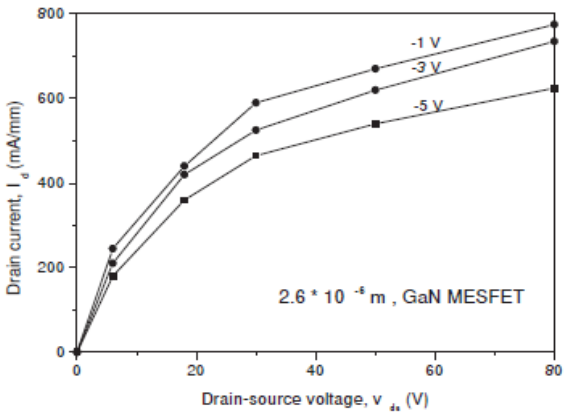

Figure 3

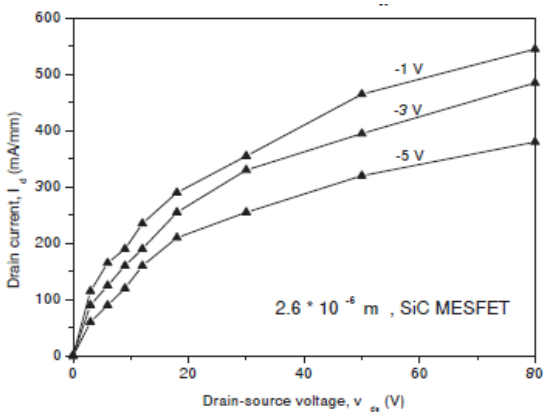

Figure 4

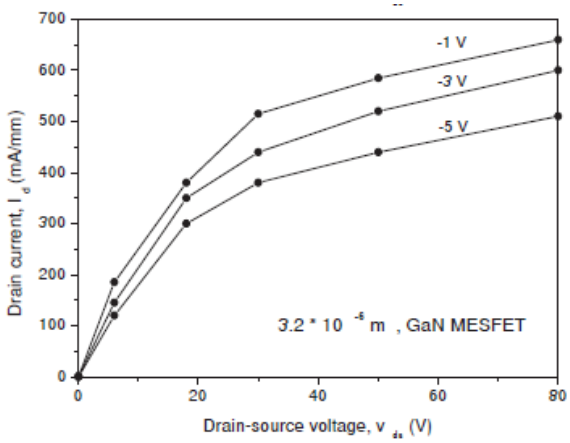

Figure 5

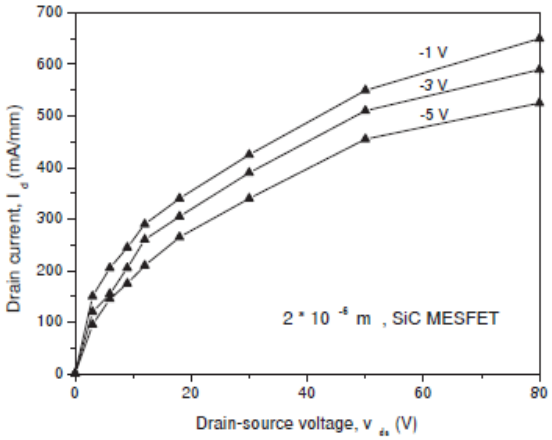

Figure 6

1.2. Frequency performance of SiC MESFET:

Sic MESFET's for high power output; we recently reported 80 watts CW output power with 31% power-added efficiency (PAE) at 3.1 GHz, from a single MESFET device with 48 mm of gate periphery operated in a hybrid circuit. For much smaller devices (W, = 250 pm), we have recently achieved 5.2 W/mm with 11.1 dB associated gain and 63% PAE at 3.5 GHz, a result we have not previously reported. We have extended this S-band MESFET technology to X band, and we now report the demonstration of over 30 watts of output power at 10 GHz from a single 12-mm Sic transistor under pulsed-mode conditions[52]. RF power performance of microwave amplifiers fabricated from wide bandgap semiconductor transistors and demonstrates that

microwave power amplifiers fabricated from 4H-SiC and AlGaN/GaN transistors offer superior RF power performance, particularly at elevated temperatures. Theoretical models predict room temperature RF output power on the order of 4-6 W/mm and 10-12 W/mm, with power-added efficiency (PAE) approaching the ideal values for class A and B operation, available from 4H-SiC MESFETs and AlGaN/GaN HFETs, respectively. All calculations were thoroughly calibrated against dc and RF experimental data. The simulations indicate operation at elevated temperature at least up to 5000°C is possible. The RF output power capability of these devices compares very favorably with the 1 W/mm available from GaAs MESFETs. The wide bandgap semiconductor devices will find application in power amplifiers for base station transmitters for wireless telephone systems, HDTV transmitters, power modules for phased-array radars, and other applications. The devices are particularly attractive for applications that require operation at elevated temperature. SiC MESFET's showing a record high f_{max} of 26 GHz and RF gain of 8.5 dB at 10 GHz are described in this paper. These results were obtained by using high-resistivity SiC substrates for the first time to minimize substrate [53]. 5-GHz SiC MESFET performance and the effects on device shows the above results.

Bulk growth of 6H-SiC was performed using a physical vapor transport process, and the resultant un-doped single-crystal boules were sliced and polished to generate 1-in-diameter wafers. These wafers were then used as substrates for the chemical vapor deposition of doped silicon carbide active layers. Wafers contained 24 chips, each consisting of an array of MESFETs having systematically varied geometry. A sample DC characteristic from a 320-μm periphery MESFET showed a knee voltage of 8 V, a trans conductance of 20 ms/mm, a maximum channel current of 210 mA/mm, and a gate-to-drain breakdown voltage of 100 V. Automated RF probing was used to obtain wafer maps of small signal gain, F_T, and F_{max}, revealing an excellent transistor yield of 87%. The highest-gain MESFETs in the array developed 12 dB of gain at 2 GHz with a cutoff frequency of 5 GHz [54].

Next generation cell phones require wider bandwidth up to the range of the millimeter wave with improved efficiency. The development of satellite communications and TV broadcasting requires amplifiers operating at higher frequencies with higher

power to reduce the antenna size for terminal users. The same requirement holds for broadband wireless internet connections as well. This high power and high frequency applications require transistors with large breakdown voltage, high electron velocity and high thermal conductivity. The wide band gap materials, like GaN and SiC are preferable for meeting the high frequency and high power applications [55]-[59]. The high output power density of WBG transistors allows the fabrication of much smaller size devices with the same output power. Higher impedance due to the smaller size allows for easier and lower loss matching in amplifiers. The operation at higher voltage due to its high breakdown electric field not only reduces the need for voltage conversion, but also provides the potential to obtain high efficiency, which is a critical parameter for amplifiers. The wide band gap also enables it to operate at high temperatures. These attractive features in amplifier applications enabled by the superior semiconductor properties make SiC and GaN devices promising candidates for microwave power applications. SiC based MESFET has the operational frequency limitation of X-band. This is the reason that they have been mostly employed in microwave, broadband radio frequency (RF), radar and wireless communication power amplifiers. [60]– [65]

1.3 UV photo detectors of SiC photodiodes and FETs

WBG semiconductors suitable for ultraviolet light detection, 4H-SiC detectors are successful due to the high signal-to-noise ratio and excellent visible blindness. Thanks to their properties, these devices have been extensively used for flame detection monitoring, UV sterilization and astronomy and solar blind detector. In many applications such as bio-aerosol detection and low-light imaging, the most important parameters are the sensitivity to low photon fluxes and the dynamic performance [66], [67]. The detector's timing performances are strongly influenced by the capacitance of the device which should be kept small to prevent the time constant from limiting the response time. Trade-offs between fast transit times and low capacitance are required for high-speed response. However, any change in photodiode parameters to optimize the transit time and capacitance can also affect other parameters like photoresponsivity and dark current [68]. The Schottky UV photodiodes analyzed in this work were fabricated in STMicroelectronics-Catania R&D facilities on -type 4H-SiC epitaxial layers, 4 m thick,

grown by CREE Inc, onto an -type heavily doped substrate cm . The doping concentration of the epilayer was 1– cm, as indicated by the supplier. Ohmic contacts on the sample back side were formed by sputtering of a 200 nm Ni film, followed by a rapid annealing at 1000 ˚C. Schottky contacts on the wafer front were obtained by defining integrated structures. The definition of 2 m wide stripes was obtained by combining standard optical lithography and highly selective metal etch. A rapid thermal processing at low temperature (700˚C) was used for the formation of, Schottky barrier [69]. An Al-Si-Cu metal layer (1 m thick) was sputtered on the top side of the device to define the pad for the anode contact by photolithography. Finally a metallic multilayer Ti/Ni/Au (1 Å/5 Å /0.5 Å) was sputtered on the rear of the wafer for the cathode ohmic contact [70].

The quantum efficiency of p-n junction 6H-SiC ultraviolet (UV) photodiodes has been theoretically modeled for the doping concentration range of 10^{14} -$10^{20}$$cm^{-3}$. The calculations take into account the contribution from the depletion region and the doping dependence of charge carrier transport characteristics. Data on optical and physical properties of 6H-SiC that determine the charge carrier transport and bandgap energy are collected and analyzed. The highest average external efficiency of up to 76%, through a working wavelength range of 200-400 nm, can be achieved at lower doping that result in a fully depleted top active photo absorbing layer. This is different from the current technology of commercial higher doped SiC UV photo detectors. The detectivity is shown to be conformal to the quantum efficiency in response to the design variations. The temperature dependence of the device does not change the design tradeoffs that depend on the electrical characteristics. The model presented can be extended to elevated temperatures when optical data become available at these temperatures [71].

Silicon Carbide (SiC) photodiodes have been proposed for ultraviolet (UV) light detection because of their robustness even in harsh environments, high quantum efficiency in all the UV range (200 nm-400 nm), excellent visible blindness, low dark current and high speed. Here, we report on the electro-optical performances and use in application of high signal-to noise ratio low reverse biased 4H-SiC vertical Schottky photodiodes based on the pinch-off surface effect, obtained by means of self-aligned Nickel Silicide (Ni_2Si) interdigitated contacts. The characteristics of these devices could

make their use appealing also in nuclear applications like for example scintillation light detection [72]. 4H-SiC (3.25 eV) makes it a suitable material for visible-blind UV detection. In the paper, the performance of 4H-SiC avalanche photodiodes (APDs) with a thin avalanche width of 0.1 μm is evaluated. Avalanche photodiodes with thin multiplication regions can greatly improve the signal-to-noise ratio of photo receiver systems by providing internal gain while maintaining a high operating speed and low operating voltage. The diodes exhibit a peak unity-gain responsivity of 144 mA/W at a wavelength of 265 nm. Photo multiplication measurements carried out on these diodes showed that $\beta>\alpha$ in 4H-SiC, where β and α are the hole and electron ionization coefficients, respectively. The 4H-SiC APDs also exhibit very low excess noise corresponding to $k=0.1$ (where $k=\alpha/\beta$ for hole multiplication) in the local model when illuminated by 325 nm light. This is much lower than that of commonly used Si APDs with identical thickness and indicates that 4H-SiC is well suited for high gain, low noise UV detection. In view of the large β/α ratio measured in these thin 4H-SiC APDs, multiplication must be initiated by hole injection to ensure a low excess-noise performance [73].

1.4 Prospect of SiC MESFET for MMICs

Monolithic microwave integrated circuit (MMIC) process based on an in-house SiC MESFET technology has been developed. The process uses micro strip technology, and a complete set of passive components, including MIM capacitors, spiral inductors, thin-film resistors, and via-holes, has been developed. The potential of the process is demonstrated by an 8-W power amplifier at 3 GHz, a high-linearity S-band mixer showing a third-order intercept point of 38 dB , and a high-power limiter [74].

An overview of hybrid and monolithic high-power microwave amplifiers using SiC MESFET and GaN HEMT active devices is presented. High power densities of 5.2 W/mm and 63% power added efficiency (PAE) have been demonstrated for SiC MESFETs at 3.5 GHz. This performance has driven the development of wide-bandwidth MMIC amplifiers, which have yielded 37 W of pulsed power at 3.5 GHz. GaN HEMTs on SiC substrates can achieve these high performance levels at frequencies where SiC cannot operate. At 10 GHz, a 12-mm GaN HEMT hybrid amplifier achieved a CW output

power level of 38 W with an associated gain of 8 dB and PAE of 29%, complementing a previous pulsed result of 50.1 W. MMIC amplifiers have also been demonstrated using GaN-on-SiC technology. At 16 GHz, a two-stage GaN HEMT MMIC wide-bandwidth amplifier was capable of a peak power level of 24.2 watts with an associated gain of 12.8 dB and PAE of 22%. Recently, a 6-mm single-stage narrow-band MMIC amplifier has produced 32 watts of pulsed power at 10 GHz with an associated gain of 8.3 dB and a PAE of 35.3%. Finally, to validate progress in scaling unit cell performance to large devices, we have demonstrated 103 W of CW power from a single GaN HEMT transistor at 2 GHz with an associated drain efficiency of 52% [75].

High power densities of 5.2 W/mm and 63% power added efficiency (PAE) have been demonstrated for SiC MESFETs at 3.5 GHz. Wide bandwidth MMICs have also been demonstrated with SiC MESFETs, yielding 37 W at 3.5 GHz. Even higher power densities have been obtained with GaN HEMTs, showing up to 12 W/mm under pulsed conditions. Hybrid amplifiers using GaN HEMTs on SiC substrates have demonstrated a pulsed output power level of 50.1 W, with 8 dB gain and PAE of 28% at 10 GHz, and CW power levels of 36 W have also been obtained. A wide bandwidth GaN MMIC amplifier had a peak pulsed power level of 24.2 watts, with a gain of 12.8 dB and PAE of 22% at 16 GHz [76].monolithic microwave integrated circuit (MMIC) W-band reactor doubler that delivers 30 mW of output power at 93 GHz with 12% conversion efficiency has been developed U-band MMIC MESFET power amplifier chips that exhibit 0.23 W of output power with 13 dB from 45.5 to 46.5 GHz were also developed. A doubler/amplifier chain has been integrated to deliver 30 mW of output power at 93 GHz with an overall gain of 7 dB [77].

D-LDD (Double Lightly-Doped Drain) structure for InGaP-InGaAs H-MESFETs (Heterostructure-MESFET). A D-LDD H-MESFET has three kinds of low resistance layers in the drain region, while a conventional H-MESFET has two layers. This structure improves MAG accompanied by Rd reduction with minimized gate-breakdown-voltage degradation and C_{gd} increase. This trade-offs between Rd and breakdown voltages are discussed in detail. Consequently, a typical MAG at 50 GHz exhibits 8.9 dB in a

MESFET and 7.7 dB S21 in a 1-stage amplifier. The high-frequency circuit operation proves that this technology is one of the most promising for MMIC applications [78].

2. STUDY OF SILICON CARBIDE MATERIAL

2.1 BACKGROUND

The enormous advances in the progress of SiC technology over the past 10 - 15 years have made it possible to develop almost all the basic types of semiconductor devices based on SiC, including the first integrated circuits (ICs) [79]. The fundamental parameters of SiC material are very attractive for the fabrication of semiconductor devices with superior characteristics for military and industrial needs in the aircraft and space electronics, nuclear power, automotive, and power utility industries. Because of their fundamental material parameters, SiC devices have been predicted to have a higher breakdown voltage (at the same doping level) and to operate at a higher forward current density than Si devices. The unique physical properties of SiC include a large energy band-gap, high thermal conductivity, and a high electric breakdown field. The high thermal conductivity coupled with low thermal expansion and high strength gives this material exceptional thermal shock resistant quality [80]. SiC is the first semiconductor material to result in the realization of blue LEDs. Today Si is the material dominating the electronics industry for IC design. SiC materials however are currently metamorphosing from research and development into a market driven manufacturing product. Emerging markets for SiC homo-epitaxy include high-power switching devices and microwave devices. The unipolar Silicon Schottky (Si) and Silicon carbide Schottky (SiC) diodes are commonly used in power converter circuits. In spite of both diodes come from the same unipolar family, the issues of higher switching losses with regards to reverse recovery losses have yet been solved. Nevertheless, the new SiC diode has emerged in the market in recent years where they are expected to improve the efficiency of the converter by allowing a further reduction in reverse recovery energy losses and hence increasing the performance. The additional substance of carbide element in the power Schottky diode may eventually lower the reverse charge current and thus, improve the overall transient response in the converter. These exciting device results stem primarily from the exploitation of the unique electrical and thermo-physical properties offered by SiC compared to Si and GaAs. [81].

3C-SiC material:

3C-SiC has an advantage as it is able to be grown on silicon substrates, however at the moment with reduced quality. This allows for the possibility in the future of integration of 3C-SiC devices with silicon technology on the same chip. Another advantage is that 3C-SiC does not suffer from stacking faults growth, as these tend to grow towards 3C-SiC. 3C-SiC has larger electron mobility than for 4H-SiC but has reduced hole mobility. The main disadvantages when compared to other poly types are the lower band-gap and breakdown field and the advantage of replacing existing silicon devices is strongly reduced. [82]

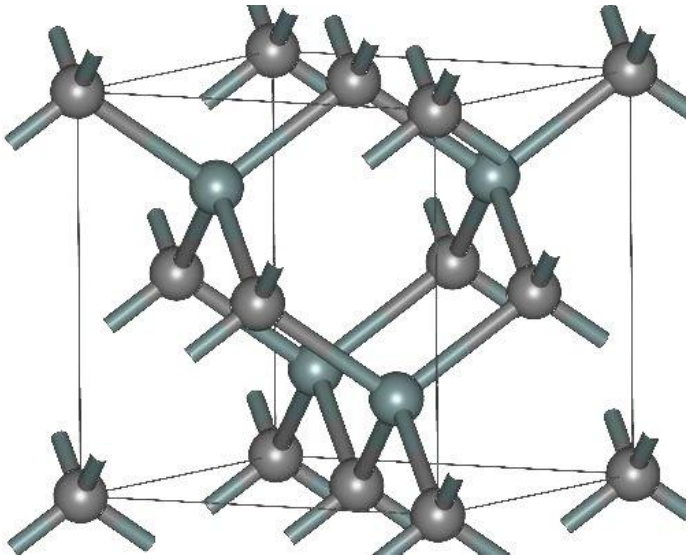

Figure 7 Structure of (β) 3C-SiC

The above figure 7 shows the structure of 3C-SiC. The beta form has had relatively few commercial uses, although there is now increasing interest in its use as a support for heterogeneous catalysts, owing to its higher surface area compared to the alpha form [83].

4H-SiC

The low-field mobility for 4H-SiC is about half that of silicon with a small anisotropy (20% higher in the direction parallel to the c-axis) The anisotropy in 4H-SiC depends on the electric field, and at high electric fields the saturation velocity is 20% lower in the c-axis direction. 4H-SiC and 6H-SiC are the most mature polytypes and they are the ones which have been characterized most thoroughly. The transport properties are better for 4H-SiC and, at present, this polytype forms the basis for most of the commercial products [84]. The figure 8 shows the crystal structure of 4H SiC.

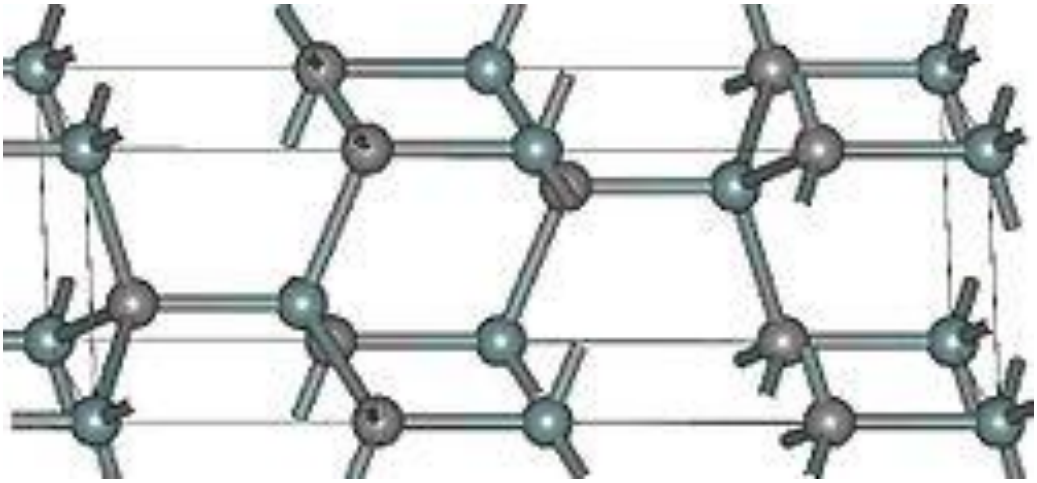

Figure 8 Structure of 4H-SiC

6H-SiC

6H-SiC has a large anisotropy due to the long repetition length in the crystallographic lattice. The mobility in the direction perpendicular to the c- axis (commonly parallel to the surface) is four times greater than in the c- axis direction. Compared with Si the mobility in 6H-SiC is about 25% in the direction perpendicular to the c-axis, and 7% in the direction parallel to it. The saturation velocity for 6H-SiC is $2 \cdot 10^7$cm/s in the direction perpendicular to the c-axis, but only $0.6 \cdot 10^7$cm/s in the direction parallel to it [85]. The figure 9 shows the crystal structure of 6H-SiC.

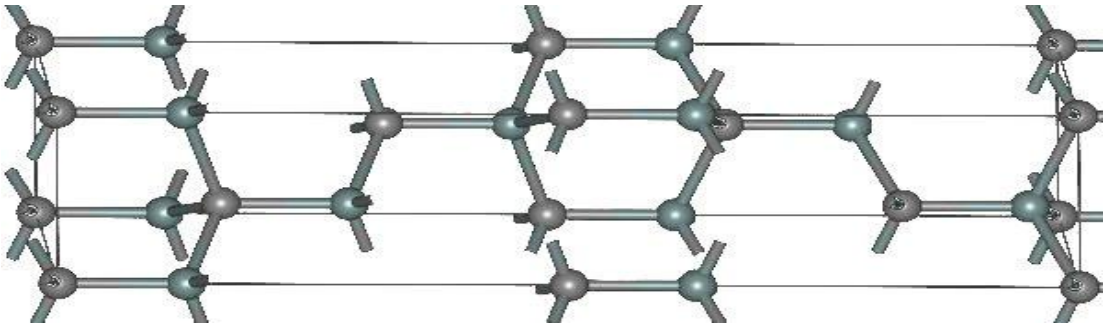

Figure 9 Structure of 6H-SiC

In the past decade, tremendous progress has been made in the material growth and processing of wide band-gap semiconductors, particularly SiC and GaN, and high quality SiC and GaN wafers are now commercially available [86]. Both types of semiconductors have very wide band-gap (4H–SiC = 3.2 eV and GaN = 3.4 eV) and are visible blind. Moreover, 4H-SiC has very high breakdown field, outstanding radiation hardness, and excellent chemical and mechanical rigidity, good thermal conductivity and as such are excellent candidates for photo detection in high temperature and high radiation environment conditions. The Figure 1.1 and 1.2 shows the breakdown voltage and thermal conductivity of different semiconductor materials. Due to the wide band-gap of SiC and GaN, the leakage current can be many orders of magnitude lower than the leakage current of Si detectors, making SiC and GaN good candidates for high sensitivity visible blind UV detection. GaN has the advantages of the availability of hetero-structures, which allows designing cutoff wavelength in the UV range by using AlGaN with different Al percentage. It therefore adds great flexibility in detector design and relieves or eliminates the requirement of optical filters. SiC, however, has much better material maturity compared to GaN material. Additionally, SiC substrate and epi-growth technologies have developed to such a level as to allow the fabrication of many different types of SiC photo detectors with desired features. SiC UV p-i-n photodiodes have already been fabricated and are commercially available. SiC avalanche photodiodes with extremely high gain and low excess noise have also been demonstrated [87]. Figure 10 shows the breakdown voltages of different semiconductor materials. Figure 11 shows the thermal conductivity for different semiconductor materials.

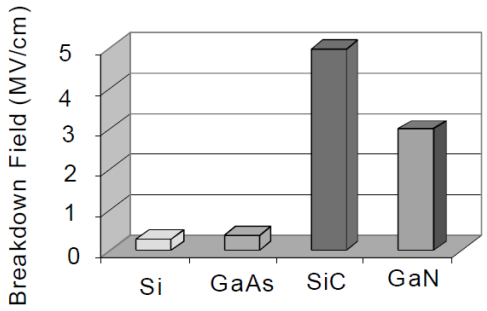

FIGURE 10 Breakdown voltages for different semiconductors materials.

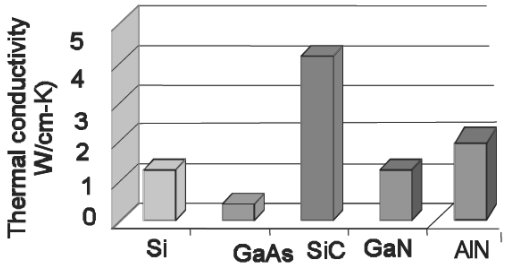

FIGURE 11 Thermal conductivity for different semiconductors materials.

The 6H-SiC poly-type has a wide band-gap (3 eV), high critical field strength (300-400 MV/m), high-saturated electron velocity (2.0 x 10^7 cm/s) and high thermal conductivity (4.9 W/cm ^oC). These material properties make semi-insulating 6H-SiC an attractive semiconductor material for the Photoconductive Semiconductor Switch (PCSS) application [88].

2.2 Manufacturing of SiC

Acheson process is a process which is used mainly for the manufacture of silicon carbide. Currently coke and quartz are used as major raw materials to produce SiC in bulk quantities. A schematic of a resistance furnace of the type used in the Acheson process is shown in Figure 2.5. SiC has extreme hardness, sharpness and good thermal properties and hence it is employed as abrasive and refractory material. Acheson process is a carbothermal synthesis of SiC [89].

The main raw materials are SiO_2 and C which are made to react at high a temperature. Saw dust and salt are also added, so that saw dust burns and provides pores

facilitating escape of evolved gases (at high temperatures). Firing is done for about 40 hours and after cooling, the side walls are removed. An outer layer of uncombined mixture is broken away, exposing the cylindrical mass of sharp, brilliant crystals. A cross sectional view of the resistor furnace after cooling is given in Figure 2.5 illustrating the silicon carbide is segregated by particle size of the product. This is the silicon carbide [90]. Figure 12 is the correctional view which illustrates SiC during manufacturing.

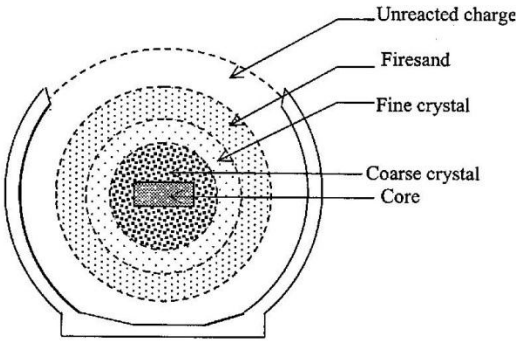

Figure 12 Illustration of Silicon Carbide when Manufacturing

2.2.1 Acheson process

Acheson developed the first technique employed for a large – scale production of silicon carbide in 1885, in order to obtain an abrasive SiC powder. Starter raw materials as silica sand, petroleum coke, (with percentages of common salt and saw dust) are pressed in a electrical furnace, heated up to 2500 °C for 7 – 10 days. During the Acheson process small hexagonal SiC crystallites are produced, and these substrates (with an area typically on the order of 1 cm2) were used for the early studies on the semiconductor behavior of SiC [91].

2.2.2 Lely and Lely modified processes

Acheson process was improved by Lely in 1955, introducing the first vapour phase transport technique SiC crystallites as those produced in Acheson furnaces are pressed on the walls of a reactor constituted by a graphitic cylindrical crucible. After the loading, the crucible is closed with a graphitic lid and heated usually up to 2500 °C in an inert gas atmosphere. In these conditions SiC sublimes and the gaseous species nucleate

on the walls of the reactor, guided by a temperature gradient, with the growth of a small amount of SiC hexagonal platelets with high crystal quality. A SiC high – purity crystal seed is inserted into a crucible very similar to those employed in the Lely technique, together with SiC powder as starter material. The crucible can be then heated up to 2200 °C in an argon inert atmosphere, with a temperature gradient between the seed and the source material. When sublimation of SiC occurs, the crucible is totally saturated of vapours constituted by Si2C, SiC2, Si2 and Si that readily nucleate on the colder crystal seed. The distance between the source and the seed, the temperature gradient and the pressure of the gaseous species determine the SiC boule growth rate. Generally, a low pressure inside the crucible can improve the diffusion of the gases, with high growth rates. The growth rates for high quality SiC crystal production are normally in the range between 0.5 and 1 mm/h, with a growth duration extended up to 40 h. figure 13 shows the Lely modified growth process.

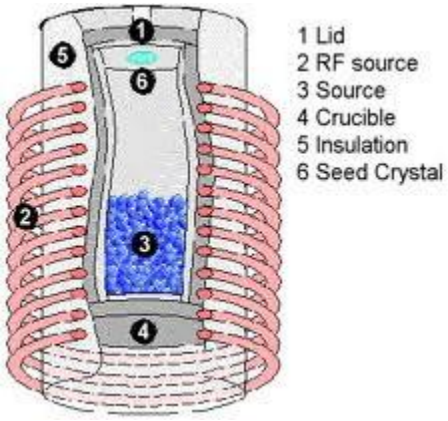

Figure 13 Reactor for “Lely modified” growth process

2.2.3 Liquid phase epitaxy (LPE)

SiC melting can take place only at pressures of around 100 000 bar and at a temperature of about 3200 °C. However, in the recent years the study of the Si – C phase diagram has revealed the possibility of an increase in the C solubility adding transition metals impurities to the melt. In such a way, a new bulk growth technique, based on the liquid phase epitaxy, has been introduced. A reactor with a resistance heater and provided with a stainless high pressure lid is internally covered by a graphite heat shield. In an

internal graphite crucible, a SiC crystal seed is kept in contact with a Si – C melt. Argon is present in the reactor, and the crucible containing the melt can be rotated in order to improve the growth homogeneity. The cooling of the solution on the seed crystal surface results in SiC solidification at a maximum growth rate of 0.5 m/h. This technique offers the possibility to dope the SiC during the growth (with Al or N for p or n – type doping), with a good control on the polytype and on the defect density. Figure 14 shows LPE reactor for SiC material growth.

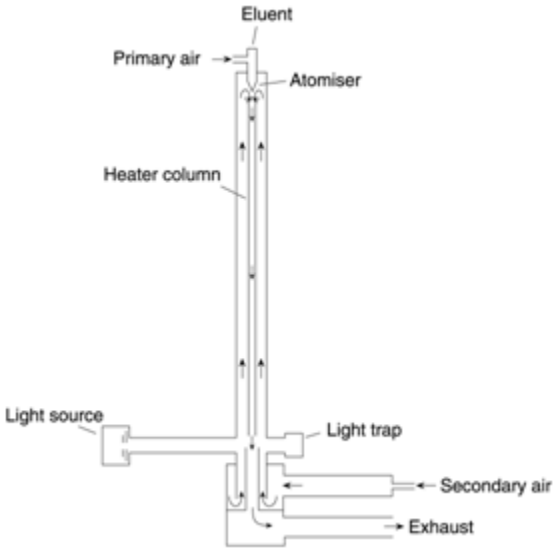

Figure 14 Schematic of a reactor for SiC LPE

2.2.4 High temperature chemical vapor deposition (HTCVD)

The vertical HTCVD reactor is made of graphite, and its shape is very similar to the reactors for the liquid phase epitaxial, but with substantial differences in the process. The seed is situated on the reactor's top, and the source for the growth is constituted by precursor gases containing Si and C, such as silane or propane, entered in the reactor with a carrier inert gas (helium is a good candidate). The cracking of the precursors in a hot zone leads to the formation of chemical radicals. These species can migrate through the colder seed crystal surface, where nucleation takes place. A growth rate as high as 1 m/h

can be obtained with this technique, if the precursor and carrier gases fluxes, the pressure of the reactor and the temperature of the seed crystal are optimized.

2.2.5 Bulk growth techniques comparison

The most important growth techniques are compared discussing the following parameters:

- Growth rate: Seeded sublimation growth can provide substrate growth at a rate of 1 mm/h with a good crystal quality, and both LPE and HTCVD must be improved in order to achieve a sufficient growth rate for a large commercial production.

- Boule dimensions: the diameter and the maximum number of SiC wafers produced during a run in a reactor are closely related to the boule diameter and length Seeded sublimation growth offers the best results in terms of process maturity and control, while LPE is limited by the possibility of a reactant depletion during long lasting growths; further HTCVD improvements can be hampered by difficulties in the process scaling up to large wafer diameter.

- Growth costs: both equipment (reactors) and precursor costs should be taken into account in this factor Seeded sublimation growth reactors are probably less expensive when compared to the more complex equipment used in the HTCVD and LPE techniques, with high demands on the gases purity, and on the material robustness and stability. Furthermore, the source materials used in the seeded sublimation growth are not so expensive as the high purity gases employed by a HTCVD reactor.

- Maturity and future developments: Seeded sublimation growth is the most advanced technique up to now, but it shows a steady improvement. The high defect control offered by the LPE and the wide range of adjustable process parameters that characterize HTCVD are the main driving forces for a future improvement of these techniques.

2.3 Differences between the forms of SiC

3C-SiC has some important material property advantages over 6H-SiC, such as higher low-field electron mobility, which could be exploited to produce superior devices

and circuits for microwave power and other applications [92]. Because no technique has been developed for obtaining semiconductor device quality 3C-SiC on suitably large substrates, these property advantages have not been realized in electrical devices or circuits. Given the lack of 3C substrates suitable for mass production, efforts have focused on heteroepitaxial growth of 3C-SiC layers on silicon and other potentially large-area, reproducible substrate materials. To date however, the crystallographic quality of the 3C-SiC resulting from these efforts has been poor, and this has been reflected in poor electrical characteristics of diodes and transistors fabricated in the resulting 3C-SiC material. Diode junctions at room temperature have been very leaky and incapable of rectification beyond a few 10's of volts reverse bias, and 3C-SiC transistors on substrates suitable for mass production have likewise been extremely limited in their capabilities [93]. Some of the most common SiC polytypes can be identified by their color, when different doping concentrations are considered. 4H – SiC is brown when N – doped with a high concentration, while in the same conditions 6H shows a green color. Another interesting feature of silicon carbide is its polarity along the c – axis and the presence of different surface modifications.

3. MESFET (Metal Semiconductor Field Effect Transistor)

3.1 INTRODUCTION

The MESFET was proposed and first demonstrated by Mead in 1966. Shortly after, microwave performance was reported by Hooper and Lehrer in 1967, using a GaAs epitaxial layer on semi insulating GaAs substrate. Both JFET and MESFET have the advantage of avoiding problems related to the oxide-semiconductor interface in a MOSFET, such as interface traps and reliability issues arising from hot-electron injection and trapping. However, they have limitation on bias range allowed on the input gate. In comparison, the MESFET offers certain processing and performance advantages over the JFET. The metal gate requires only low-temperature processing compared to a p-n junction made by diffusion or implant-anneal sequence. The low gate resistance and low IR drop along the channel width is a big factor in microwave performance such as noise and f_{max}. The metal gate has better control in defining short channel lengths for high-speed applications. It can also serve as an efficient heat sink for power applications [94].

The key advantage of the MESFET is the higher mobility of the majority carriers in the channel and less scattering effect as compared to the MOSFET. Since the carriers located in the inversion layer of a MOSFET have a Wave function, which extends into the oxide, their mobility – also referred to as surface mobility – is less than half of the mobility of bulk material. As the depletion region separates the carriers from the surface their mobility is close to that of bulk material. The higher mobility leads to a higher current, trans-conductance and transit frequency of the device. The channel length of MOSFET is dependent with gate length, whereas this issue is not occurred for MESFET device.

The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically 0.7 V for Schottky diodes. The threshold voltage therefore must be lower than this turn-on voltage. As a result it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFET.

The higher transit frequency of the MESFET makes it particularly of interest for microwave circuits. While the advantage of the MESFET provides a superior microwave amplifier or circuit, the limitation by the diode turn-on is easily tolerated. Typically depletion-mode devices are used since they provide a larger current and larger trans-conductance and the circuits contain only a few transistors, so that threshold control is not a limiting factor. The buried channel also yields a better noise performance as trapping and release of carriers into and from surface states and defects is eliminated [95].

3.2 BASIC STRUCTURE OF MESFET

The base material on which the transistor is fabricated is a SiC substrate. The cross sectional view of MESFET is shown in Figure 15. A buffer layer is epitaxial grown over the SiC substrate to isolate defects in the substrate from the transistor. The channel or the conducting layer is a thin, lightly doped (n) conducting layer of semiconducting material epitaxial grown over the buffer layer. Finally, a highly doped (n+) layer is grown on the surface to aid in the fabrication of low-resistance ohmic contacts to the transistor. This layer is etched away in the channel region. Alternatively, ion implantation may be used to create the n channel and the highly doped ohmic contact regions directly in the semi-insulating substrate. Two ohmic contacts, the source and drain, are fabricated on the highly doped layer to provide access to the external circuit. Between the two ohmic contacts, a rectifying or Schottky contact is fabricated. Typically, the ohmic contacts are Au–Ge based and the Schottky contact is Ti–Pt–Au.

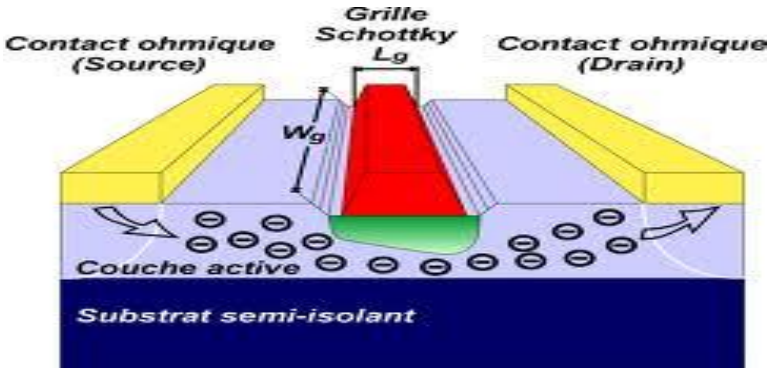

FIGURE 15 Cross sectional view of MESFET

3.3 PHYSICS OF MESFET

The carrier flow from source to drain is controlled by a Schottky metal gate. The control of the channel is obtained by varying the depletion layer width underneath the metal contact which modulates the thickness of the conducting channel and thereby the current between source and drain. Spacing of the source and drain with respect to the gate, and the lateral extent of the gate are important though somewhat less critical design parameters. MESFET current handling ability improves as the gate is elongated laterally, keeping the active region constant, however is limited by phase shift along the gate due to the transmission line effect. The MESFET differs from the common insulated gate FET in that there is no insulator under the gate over the active switching region. This implies that the MESFET gate should, in transistor mode, be biased such that one does not have a forward conducting metal semiconductor diode instead of a reversed biased depletion zone controlling the underlying channel. While this restriction inhibits certain circuit possibilities, MESFET analog and digital devices work reasonably well if kept within the confines of design limits. The most critical aspect of the design is the gate metal extent over the switching region. Generally the narrower the gate modulated carrier channel the better the frequency handling abilities [96-97].

3.4 SiC MESFET

SiC based MESFET are made of n-type material because of the higher electron mobility and is fabricated using epitaxial layers on semi-insulating substrates to minimize parasitic capacitances. A MESFET has three metal semiconductor contacts. The ohmic contacts are labeled source and drain, and the Schottky barrier is labeled gate. A MESFET is often described in terms of the gate dimensions. The effective thickness of channel can be altered by reverse bias of Schottky diode which is created by deposition of appropriate metal on the N-type GaAs layer and the active channel depth translate the pinch off voltage related to many fabrication parameters.

3.4.1 4H-SiC PLANAR MESFET

SiC (Silicon Carbide) is very good material due to its superior electrical, chemical and thermal properties and its high electric breakdown field, high saturated electron drift velocity and high thermal conductivity makes it suitable for high power microwave devices. 4H-SiC means four bi-layer stacking periodicity and hexagonal symmetry of Silicon Carbide, and it is one type of Poly-type (i, e. variations of the same chemical compound that are identical in two dimensions and differ in the third). 4H-SiC MESFET has the capability of high voltage, high output impedance, easy matching and wide bandwidth through X-band (8.2-12.4 GHz). This is fabricated using ion-implantation without recess gate etching to eliminate potential damage to gate region and to lower contact resistance [98].

3.4.2 SiC MESFET PRINCIPLE OF OPERATION

The current-voltage characteristics of a thin n-type 4H-SiC layer in which electrons are carrying the current are discussed in detail. If a positive voltage V_{ds} is applied to the drain, electrons will flow from source to drain. Hence the source acts as the origin of carriers and the drain as a sink. For small voltages, the 4H-SiC layer behaves like a linear resistor. For bigger voltages, the electron drift velocity does not increase at the same rate as the electric field E. As a result, the current-voltage characteristic falls below the initial resistor line. As V_{ds} is further increased, E reaches a critical field, E_c for which the electrons reach a maximum velocity v_s. At this drain voltage, the current starts to saturate.

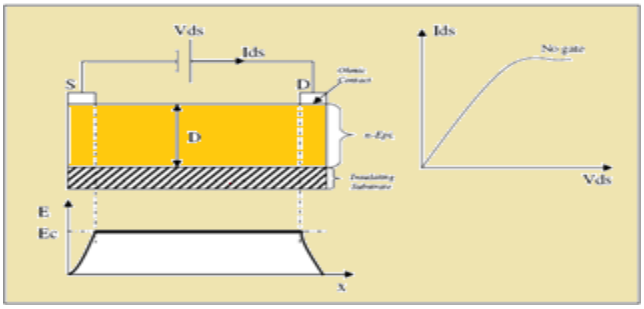

FIGURE 16 I-V characteristics of an n-type 4H-SiC layer with two ohmic contacts and without gate

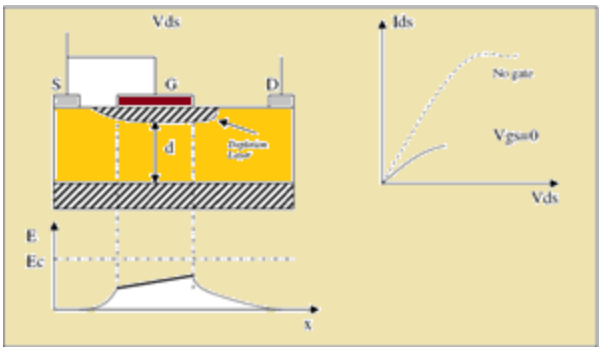

FIGURE 17 I-V characteristics of an n-type 4H-SiC layer with two ohmic contacts and a metal contact as gate

In Figure 16, a metal-to-semiconductor contact, called the gate, has been added between source and drain. This contact creates a layer in the semiconductor that is completely depleted of free-carrier electrons. This depletion layer acts like an insulating region and constricts the channel available for current flow in the n layer. The width of the depletion region depends on the voltage applied between the semiconductor and the gate. In Figure 17 the gate is shorted to the source and a small drain voltage is applied. Under these conditions, the depletion layer has a finite width and the conductive channel beneath has a smaller cross section d than in Figure 18. Consequently, the resistance between source and drain is larger.

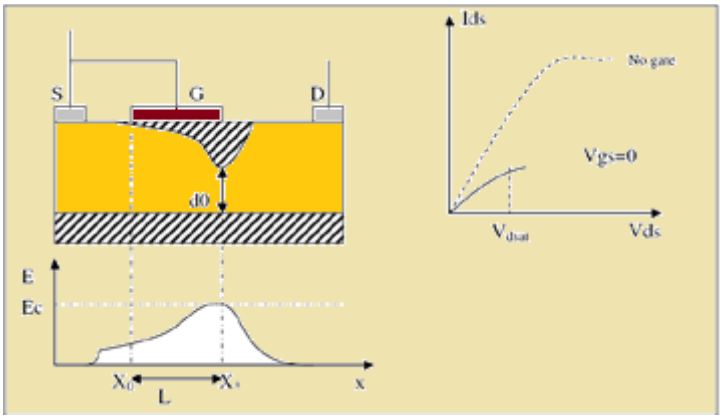

FIGURE 18 $V_{ds}-I_{ds}$ Representation with respect to V_{gs} with shorted source and gate

If the drain voltage is increased beyond V_{dsat} the depletion region widens toward the drain. The point x_1, where the electrons reach the limiting velocity, moves slightly

toward the source in Figure 19. As moves x_1 closer to the source, the voltage at x_1 decreases. Therefore, the conductive cross section d_1 widens and more current is injected into the velocity-limited region. This results in a positive slope of the I_{ds} curve and a finite drain-to-source resistance beyond current saturation. The effect is particularly prominent in microwave MESFETs with short gate lengths. going on from x_1 toward the drain, the channel potential increases, the depletion layer widens, and the channel cross section d becomes narrower than d_1. Since the electron velocity is saturated, the change in channel width must be compensated for by a change in carrier concentration to maintain constant current. An electron accumulation layer forms between x_1 and x_2, where d is smaller than d_1. At x_2 the channel cross section is again d_1 and the negative space charge changes to a positive space charge to preserve constant current. The positive space charge is caused by partial electron depletion. The electron velocity remains saturated between x_2 and x_3 due to the field added by the negative space charge. In short, the drain voltage applied in excess of V_{dsat} forms a dipole layer in a channel that extends beyond the drain end of the gate.

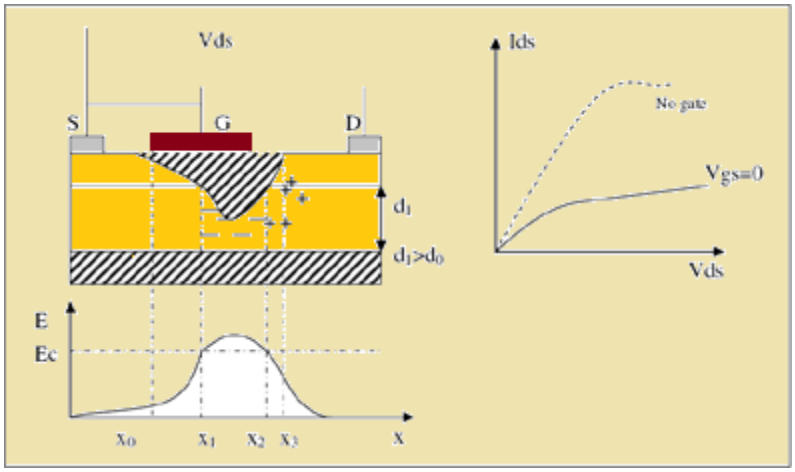

FIGURE 19 : I_{ds} versus V_{ds} Representation with respect to V_{gs} with more widening of depletion region

When a negative voltage is applied to the gate (Figure 20), the gate-to channel junction is reverse biased, and the depletion region grows wider. For small values of V_{ds}, the channel will act as a linear resistor, but its resistance will be larger due to a narrower cross section available for current flow. As V_{ds} is increased, the critical field is reached at

a lower drain current than in the $V_{gs} = 0$ case, due to the larger channel resistance. For a further increase in V_{ds}, the current remains saturated. In essence, the MESFET consists of a semiconducting channel whose thickness can be varied by widening the depletion region under the metal-to-semiconductor junction. The depletion region widening is the effect of a field or voltage applied between gate and channel of the transistor.

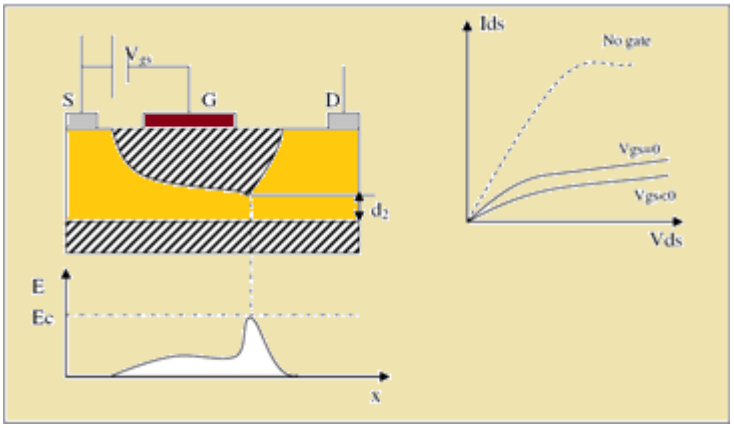

FIGURE 20 I_{ds} versus V_{ds} representation with respect to negative gate to source voltage

3.4.3 I-V Characteristics of MESFET

As mentioned above the source and drain terminals are ohmic contacts and gates are Schottky contact. Most MESFET devices are Depletion Mode Devices i.e., the device with n-type conductive channel at $V_g = 0$ V. This means that in the presence of applied reverse gate bias, current can flow between the source and drain contacts. Enhancement Mode Devices do not conduct current between the drain and source unless forward gate bias is applied (no conductive channel at $V_g = 0$ V). For depletion mode devices, when low bias voltages are applied between the source and the drain contacts, a current flows through the channel. The current is linearly related to the voltage across the terminals. For higher drain-source voltage levels, the electrons in the semiconductor material will attain their maximum carrier. The gate contact in a MESFET device is a Schottky barrier. The energy band bending produced by making Schottky barrier contact with the semiconductor creates a layer below the gate that is completely depleted of free charge carriers. As no free carriers exist in this depletion layer, no current can flow through it. The available channel region for current flow is reduced due to existence of this depletion

layer. As reverse bias is applied to the gate, the depletion layer penetrates deeper into the active channel. These further reductions in channel region result in further reduction of current. Then the gate voltage acts as a means for limiting the maximum amount of source-drain current that can flow. When enough reverse bias is applied, the depletionregion will extend across the entire active channel and allow essentially no current to flow. That gate-source potential is termed as the “Pinch-off voltage” [99].

4. THEORY ON THE ANALYTICAL MODEL

We assume that the current saturation occurs when the average electric field under the gate reaches the domain sustaining field where $\mathbf{V_s}$ is the saturation electron drift velocity, is the low field mobility.

$$Es = Vs/\mu \quad \text{.....(1)}$$

Where

E_s = Domain sustaining field.

V_s = Voltage across the gate region at the saturation point.

μ= Low field mobility.

In fact, if the doping fluctuations are small and rather special boundary conditions are satisfied under the gate, the domain might form in the GaAs based MESFET when the electric field is larger than the electron peak velocity field Ep (rather than **Es),** so that the hysterisis effects and negative differential resistance due to the domain formation are observed [100, 101]. From the formal point of view, the assumption is similar to the condition previously treated in [102, 103] where the MESFET saturation at the peak velocity (avoiding domain and formation) was envisaged. But the physical interpretation and the approximations are considered different.

4.1. **SATURATION CURRENT**

We start from the fundamental equation of field-effect transistors.

$$I_{ch} = g_0\{V_i - (2/3)((\sqrt[3]{V_i + V_{Bi} - V_G} - \sqrt[3]{V_{Bi} - V_G})/\sqrt{V_{po}})\} \quad \text{.....(2)}$$

Where

I_{ch} = Channel Current.

V_i = Voltage drop across the gate at the saturation.

V_{bi} = Built in voltage.

V_G = Gate voltage.

V_{po} = Pinch – off voltage.

g_0 = Conductance.

$$g_o = q\mu N_D WA/W_G \quad \text{.....3}$$

$$V_{po} = qN_D A^2/2 \in_0 \in \quad \text{.....4}$$

Where

q = Electronic Charge.

N_D = Doping Density

W=Gate Width

A = Device active channel Thickness

W_G= Gate length.

is the pinchoff voltage, q is the electronic charge, $\mathbf{N_d}$ is the doping density, Є Є $_0$is the permittivity, **A** is the device thickness, $\mathbf{W_G}$ is the gate length, **W** is the gate width is valid when

$$V_i \leq V_s = E_s W_G \quad \text{..... (5)}$$

For typical MESFET parameters (W_G~ 1μm)

$$V_s \ll V_{Bi} - V_G \quad \text{..... (6)}$$

The Channel current is almost linear up to the saturation point

$$I_{ch} = g_0[1 - (A_0/A)]V_i \quad \text{..... (7)}$$

Where

g_d = Channel Conductance.

Here

$$A_0 = A(\sqrt{(V_{bi} - V_G)/V_{po}}) \quad \text{(8)}$$

And

$$g_d = g_0(1 - (A_0/A)) \quad \text{(9)}$$

Where

g_d = drain conductance.

The saturation current I_{sat} is equal to

$$I_{sat} = g_d V_s \quad \text{(10)}$$

In order to check (9), (10) we calculated the dependences of I_{sat} and g_d on the device thickness A in the frame of the two-dimensional model developed in [104]. We also compared our results with experimental data [l05], [106] and with the results of a two-dimensional computer analysis [107]. This comparison shows a good agreement. The trans conductance in the saturation region is equal to

$$g_m = g_0\left(\frac{\sqrt{V_s + V_{Bi} - V_G} - \sqrt{V_{Bi} - V_G}}{\sqrt{V_{po}}}\right) \quad \text{(11)}$$

From equation 4.6

$$g_m = g_o(V_s/2(V_{po}(\sqrt{V_{Bi} - V_G}))) \quad \text{(12)}$$

In the frame of the Shockley theory, the depletion layer width $\mathbf{d_d(X)}$ is given by the following expression

$$d_d(x) = A((V(x) + V_{Bi} - V_G)/V_{po}) \quad \text{(13)}$$

where **V(x)** is the potential drop between points 0 and x ($V(W_g> = V_i$). Inequality (13) gives a possibility to derive simple expression for $\mathbf{d_d(x)}$ using an iteration method. In the zero approximation we have

$$E(x) = V_i/W_G \quad \text{(14)}$$

Where

E(x) = Electric field between 0 and x.

$$d_d(x) = A(\sqrt{E_i x + V_{Bi} - V_G/V_{po}}) \quad \text{(15)}$$

Then using (14) and the condition of the current continuity under the gate we can derive the expression for E(x) in the first approximation, substitute it into (13), find the first-order approximation for $d_d(x)$, and so on. This analysis shows that for typical MESFET parameters when inequality is valid, a zero- order approximation for $d_d(x)$ (15) is very accurate. Using (15) we can find the total charge Q under the gate in the linear region when $\mathbf{Vi} < V_s$.

$$Q = qN_D W \int_o^{Wg} d_d(x)$$

$$Q = \left(\frac{2\sqrt{2}}{3}\right)\left(\frac{WW_G\sqrt{\epsilon\epsilon_o N_D}}{V_i}\right)\left[\left(\sqrt[3]{(V_i + V_{Bi} - V_G)}\right) - \left(\sqrt[3]{V_{Bi} - V_G}\right)\right] \quad \text{(16)}$$

Where

Q= Total positive charge under the gate.

d_d = Depletion layer width.

$$Q = qN_D A_o W W_G \quad \text{(17)}$$

We can define a characteristic switching time of a SiC MESFET as [108].

$$\tau = (Q(Vs)/V_{Sat}) \quad \text{.....(18)}$$

Where

I_{sat} = saturation current

$$\tau = (\frac{Wg}{Vs})(Ao/(A - Ao)) \quad \text{.....(19)}$$

Where

τ = Switching time.

W_G = Gate Length.

V_s = Electron saturation drift velocity.

5. RESULTS AND DISCUSSIONS

The SiC MESFET has been studied by analytical modeling using Mat-Lab. The study of analytical modeling of SiC MESFET has been performed to understand the device performance. SiC MESFET device with a physical dimension of device gate Width = 100µm, gate length L= 1µm, and the fabrication parameters ion dose Q=3e^{19}cm^{-2} was preferred to select the channel depth for the pinch-off voltage, threshold voltage and break-down voltage to obtain a responsible value.

1) Channel conductance versus thickness

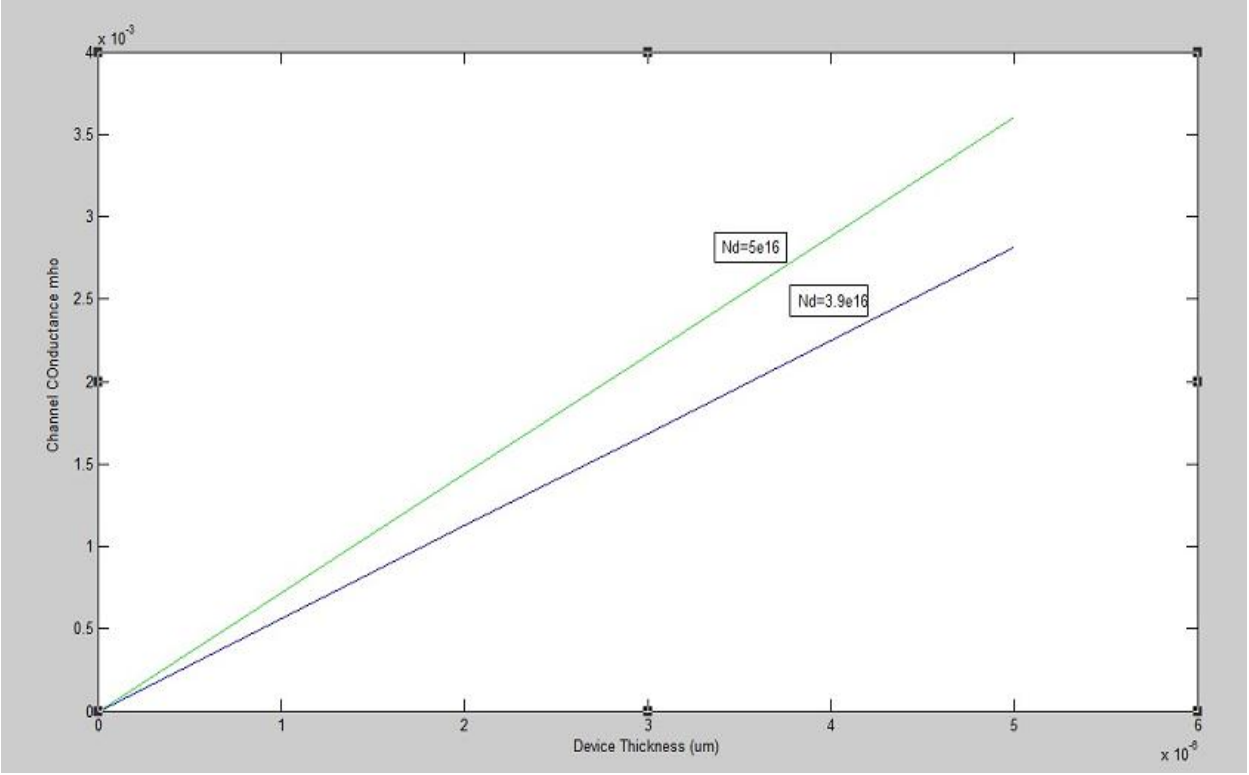

Figure 21 Channel conductance G_0 vs thickness A with different N_D values

The figure 21 shows a plot of channel conductance (G_0) versus channel depth thickness (A) for different donor impurities N_D values of $3.9x10^{16}$ cm^{-3} and $5x10^{16}$ cm^{-3} and this plot has been extracted using equation (7). At any specific channel depth, the variation of channel conductance for high and low values is responsible for high doping concentration and low doping concentration. The active channel depth directly reflects the pinch-off

voltage which translates the channel saturation current. Hence, highly doped active channel shows the high conductance and consequent the active channel thickness also contributes the break-down properties of the device. The following plot will describe the MESFET under saturation mode.

Channel current versus thickness

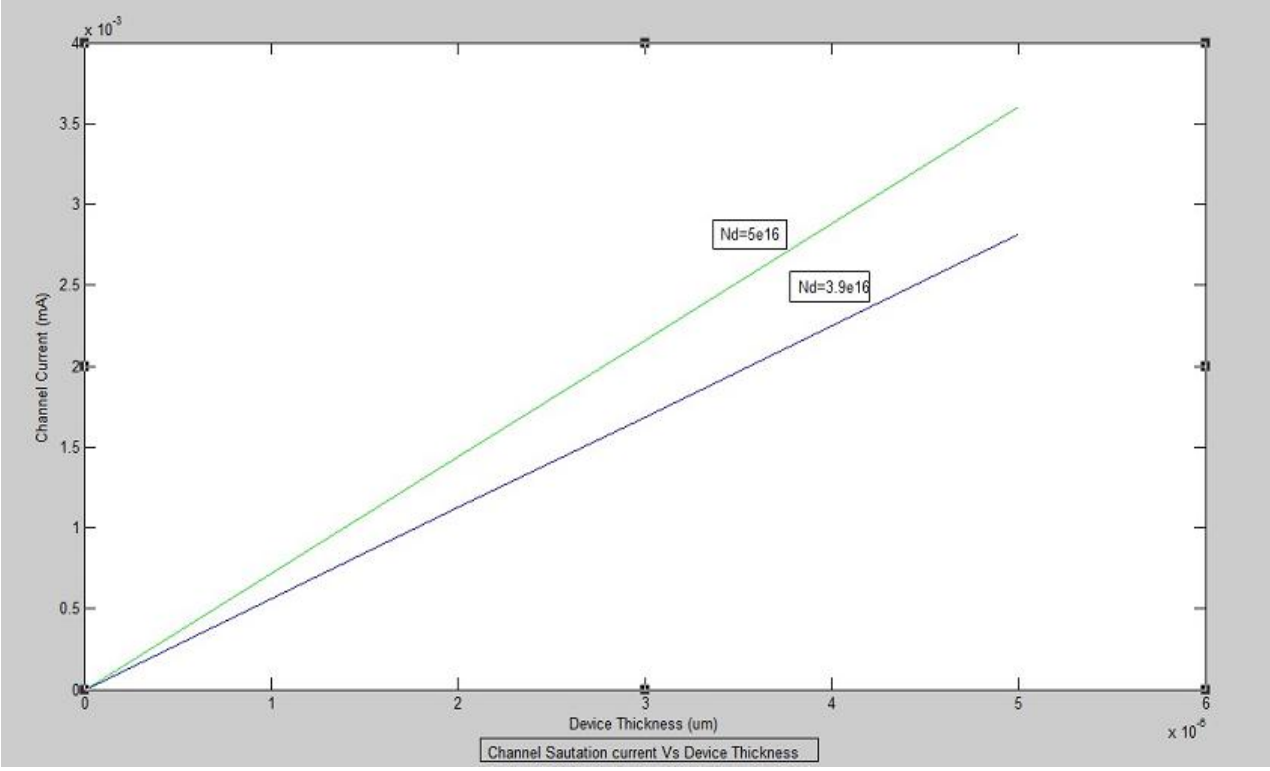

Figure 22 Channel Current (I_{sat}) vs Thickness (A) with different N_D values

The figure 22 demonstrates a plot of channel saturation (I_{sat}) versus channel thickness (A) for different donor impurities N_D values of $3.9x10^{16}$ cm^{-3} and $5x10^{16}$ cm^{-3} and this plot has been obtained by using equation (35). The saturation channel current is higher for large channel doping donor concentration N_D of $5x10^{16}$ cm^{-3} compared to low channel doping donor concentration N_D of $3.9x10^{16}$ cm^{-3} for any specific channel thickness. The channel thickness with high doping channel concentration will show high pinch-off voltage and hence the channel saturation current is larger for high channel doping concentration compared to low channel doping concentration.

Channel current versus Gate Voltage

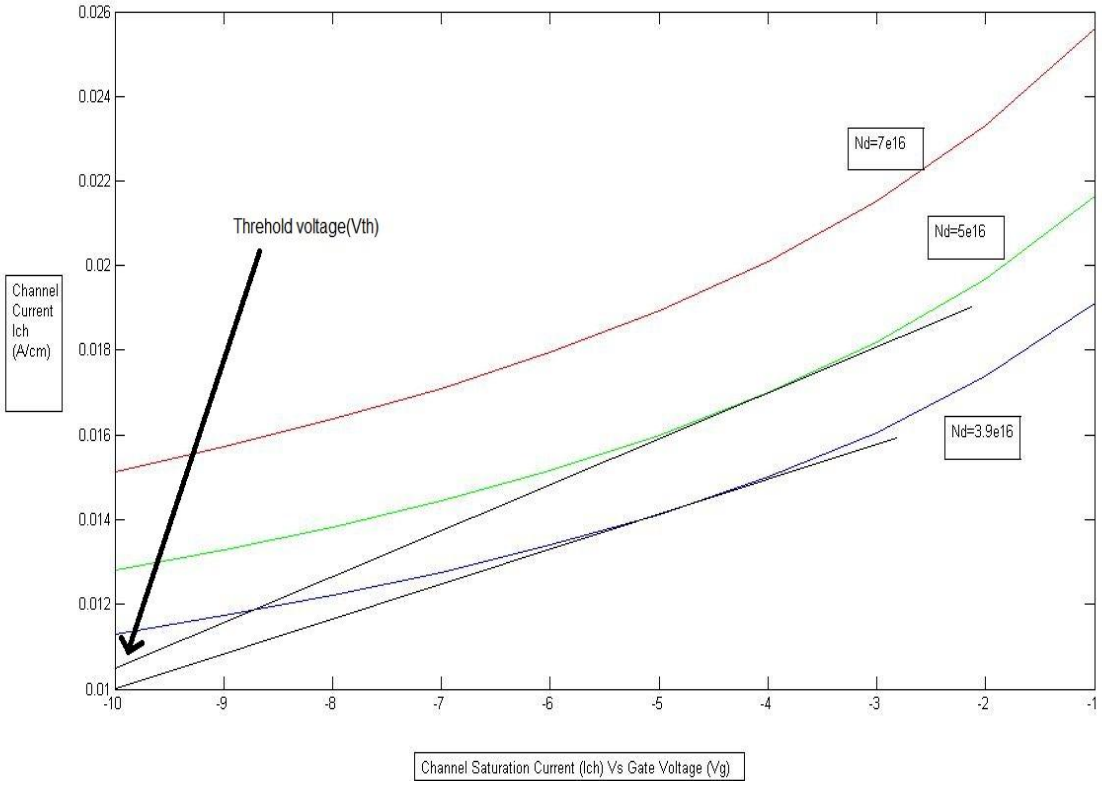

Figure 23 Channel current (I_{ch}) vs Gate Voltage (V_g) with different N_D values

Figure 23 exhibits the input and output transfer characteristics plot of channel current (I_{ch}) versus gate Voltage (V_g) for different donor impurities N_D values of $3.9x10^{16}$ cm^{-3}, $5x10^{16}$ cm^{-3} and $7x10^{16}$ cm^{-3} in the channel active region and this figure has been plotted by using equation (27) for different N_D values. All channel saturation current shows a non-linear nature and increases with the increment of gate voltage (V_G), which indicates the better switching performance compared to other devices. The lowest saturation current in the range of 0.0155A, 0.0129A and 0.0117A has been observed for different donor impurities N_D values of $3.9x10^{16}$ cm^{-3}, $5x10^{16}$ cm^{-3} and $7x10^{16}$ cm^{-3} respectively. The highest saturation current in the range of 0.019A, 0.0218A and 0.0258A has been observed for different donor impurities N_D values of $3.9x10^{16}$ cm^{-3}, $5x10^{16}$ cm^{-3} and $7x10^{16}$ cm^{-3} respectively. The threshold voltage can be estimated from the intersection

point of channel saturation current Isat and gate voltage V_G at Isat = 0 for different donor doping impurity concentration N_D values of $3.9x10^{16}$ cm^{-3}, $5x10^{16}$ cm^{-3}. The threshold voltage VT is found approximate value of -11V.

Device Thickness versus switching time

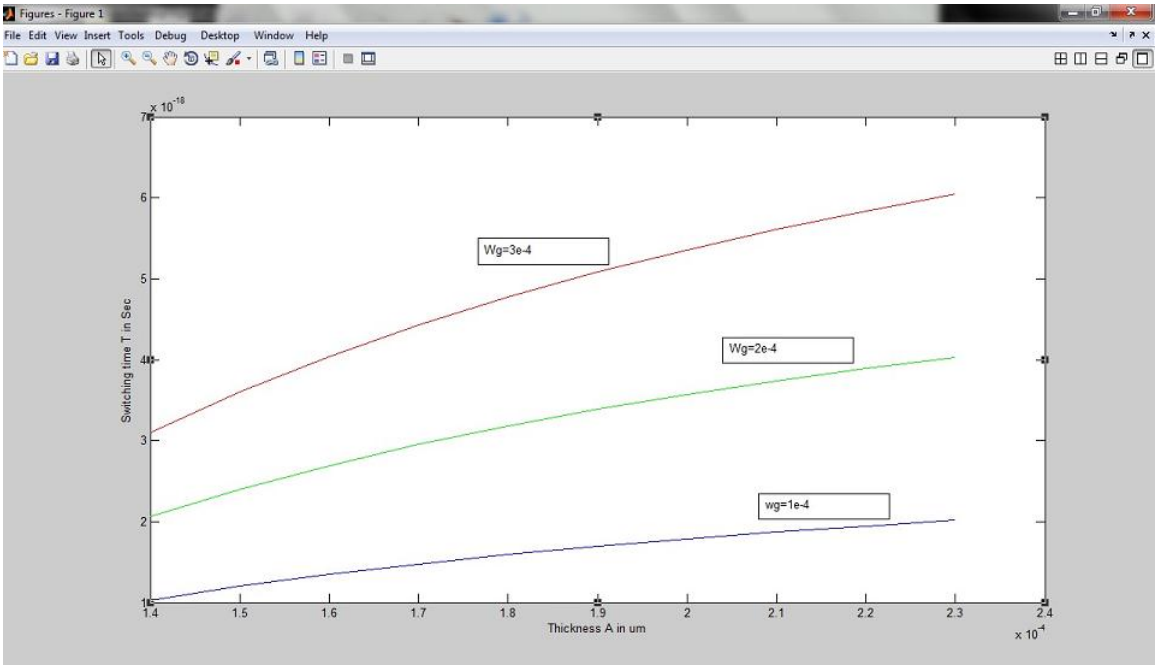

Figure 24 switching time (τ) vs thickness (A) with variation in gate length (Wg)

Figure 24 shows a plot of switching time (τ) versus thickness (A) for different gate length Wg = $1x10^{-4}$ cm, $2x10^{-4}$ cm and $3x10^{-4}$ cm and the plot has been drawn from the result of equation (44). For any specific channel depth, the switch time shows a nature of non-linear increment for different gate length Wg = $1x10^{-4}$ cm, $2x10^{-4}$ cm and $3x10^{-4}$ cm. The low switching time in the order of $1x10^{-18}$s, $2.1x10^{-18}$s and $3.15x10^{-18}$s is obtained at the channel depth of $1.4x10^{-4}$ cm and high switching time in the order of 1 $.75x10^{-18}$s, $3.47x10^{-18}$s and $5.85x10^{-18}$s is obtained at the channel depth of $2.4x10^{-4}$ cm. The lowest switching time is obtained for small gate length of $1x10^{-4}$ cm because the short gate length offers a short transit time.

Switching Time versus Gate Length

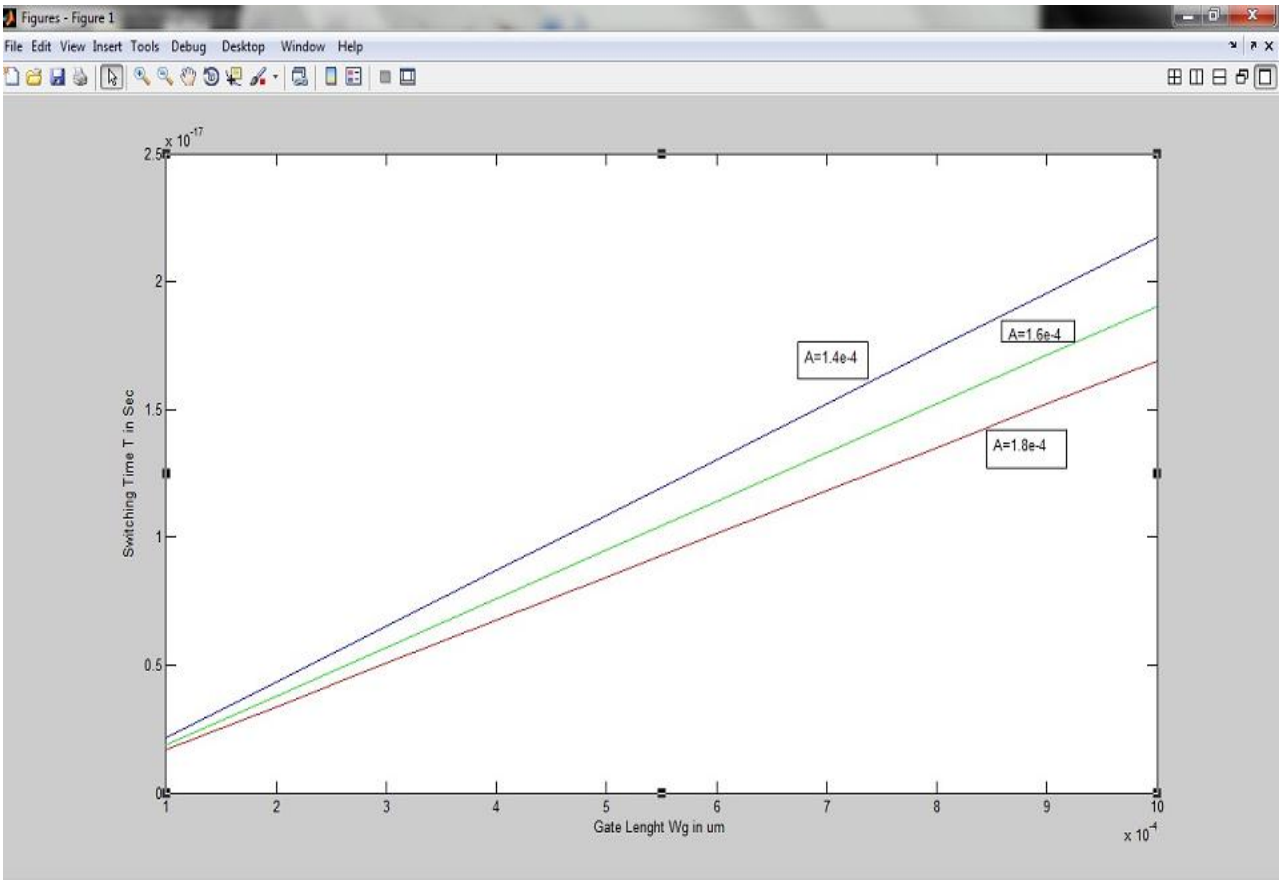

Figure 25 Switching time (τ) vs Gate length (Wg) keeping Thickness (A) as constant

Figure 25 presents a plot of **s**witching time (τ) versus gate length (Wg) for different channel thickness (A) and the plot has been prepared by using the equation (19). The switching time shows the value of approximately $0.25x10^{-17}$sec at the gate length of $1.0x10^{-4}$cm for active channel depth of $1.4x10^{-4}$cm, $1.6x10^{-4}$cm and $1.8x10^{-4}$cm , whereas the switching times increase up to $1.6x10^{-17}$sec, $1.9x10^{-17}$sec and $2.2x10^{-17}$sec at the gate length of $1x10^{-3}$cm for different active channel thickness of $1.4x10^{-4}$cm, $1.6x10^{-4}$cm and $1.8x10^{-4}$cm respectively. The plot shows that the highest switching speed can be obtained from deep channel thickness of $1.8x10^{-4}$cm, where the pinch-off voltage plays an important role for high speed performance.

6 CONCLUSION

The analytical model of the SiC MESFET presented here includes the theoretical calculation and practical simulation using Mat-lab software. The simulation results of a SiC MESFET device discussed in chapter 5 shows that highly doped active channel shows the high conductance and consequent the active channel thickness also contributes the break-down properties of the device as shown in conductance versus device thickness graph. The channel thickness with high channel doping concentration will show high pinch-off voltage and hence the channel saturation current is larger for high channel doping concentration compared to low channel doping concentration as shown in channel current versus device thickness graph. The channel saturation current shows a non-linear nature and increases with the increment of gate voltage as shown in channel current versus gate voltage graph. switching time versus thickness, switching time versus gate voltage, switching time versus gate length plots basically assist us to gain a conceptual understanding of the switching speed performance of SiC MESFET and the active channel thickness and gate length play an important role to develop SiC MESFET.

Finally, the SiC MESFET device is quite capable of handling high radiation effects without change in switching performance. Hence this device can be used in application to advanced avionics, satellites and space crafts. The research needs further advanced development of SiC based MESFET in future.

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APPENDIX -A

A	Device Thickness.
d_d	Depletion layer width.
$\varepsilon_0\ \varepsilon_s$	Permittivity of semiconductor.
q	Electronic charge.
μ	Carrier mobility in silicon carbide.
N_A	Substrate doping concentration.
N_D	Average channel doping concentration.
V_{bi}	Built-in voltage of active channel and substrate junction.
V_g	Gate-source voltage.
V_T	Threshold voltage.
V_P	Pinch off voltage.
V_{ds}	Drain-source voltage.
g_d	Channel Conductance.
g_m	Transconductance.
I_{ch}	Channel Current.
I_D	Drain Current.
I_{sat}	Saturation Current.
T	Switching time.
V_i	Voltage drop across the gate.

V_s Voltage across the gate region at the saturation point.

W Gate width.

W_g Gate length.

APPENDIX-B

MATLAB CODE

Channel conductance vs thickness

```
A=1.4e-4:0.1e-4:2.3e-4;

A1=1.4e-5:0.1e-5:2.3e-5;

W=1e-4;

Wg=1e-4;

Nd=3e19;

u=5300;

q=1.60213e-19;

e=8.859e-13;

k=1.38e-23;

T=300;

Na=1e16;

ni=5e-10;

Vg=0:-1:-10;

Vi=0.15;

Vp0=1.5;

%Vbi=0.7;

Vbi=(k*T/q)*log (Na*Nd/(ni*ni));

g0=(q*u*Nd*W*A)/Wg;
```

```
g01=(q*u*Nd*W*A1)/Wg;

A0 =A*sqrt((Vbi-Vg)/Vp0);

Gd=g0*(1-(A0/A));

plot(A,g0,'g',A1,g01,'b');
```

Channel current vs Gate Voltage

```
A=4e-4;

W=1e-4;

Wg=1e-4;

Nd=3e19;

u=5300;

q=1.60213e-19;

e=8.859e-13;

k=1.38e-23;

T=300;

Na=1e16;

ni=5e-10;

Vg=0:-1:-10;

Vi=0.15;

Vp0=1.5;

%Vbi=0.7;

Vbi=(k*T/q)*log (Na*Nd/(ni*ni));
```

```
g0=(q*u*Nd*W*A)/Wg;

A0 =A*sqrt((Vbi-Vg)/Vp0);

% A0=(2*e*(Vbi-Vg))/(q*Nd);

Gd=g0*(1-(A0/A));

Ich=Gd*Vi;

plot(Vg,Ich,'g');
```

Switching time vs Gate length

```
A=1.4e-4:0.1e-4:2.3e-4;

A1=1.4e-4;

A2=1.6e-4;

A3=1.5e-4;

W=100e-4;

Wg1=1e-4:1e-4:10e-4;

Wg0=1e-4;

Wg01=2e-4;

Wg02=3e-4;

Nd=3.9e16;

u=500;

q=1.60213e-17;

e=8.859e-13;

k=1.38e-23;
```

```
T=300;

Na=3e16;

ni=5e-10;

Vs=0.8e7;

Vd=0.1;

Vg=-1;

Es=Vs/u;

Vbi=0.0259*log (Na*Nd/(ni*ni));

A0=(2*e*(Vbi-Vg))/(q*Nd);

t0=(Wg0/Vs)*(A0./(A-A0));

t01=(Wg01/Vs)*(A0./(A-A0));

t02=(Wg02/Vs)*(A0./(A-A0));

t1=(Wg1/Vs)*(A0./(A1-A0));

t2=(Wg1/Vs)*(A0./(A2-A0));

t3=(Wg1/Vs)*(A0./(A3-A0));

plot(A,t0,'b', A,t01,'g',A,t02,'r');
```

Switching time vs Gate voltage

```
A=1.4e-4:0.1e-4:2.3e-4;

A1=1.4e-4;

A2=1.6e-4;

A3=1.8e-4;
```

```
W=100e-4;

Wg1=1e-4:1e-4:10e-4;

Wg0=1e-4;

Wg01=2e-4;

Wg02=3e-4;

Nd=3.9e16;

u=500;

q=1.60213e-17;

e=8.859e-13;

k=1.38e-23;

T=300;

Na=3e16;

ni=5e-10;

Vs=0.8e7;

Vd=0.1;

Vg=-1:-1:-10;

Es=Vs/u;

Vbi=0.0259*log (Na*Nd/(ni*ni));

A0=(2*e*(Vbi-Vg))/(q*Nd);

t0=(Wg0/Vs)*(A0./(A1-A0));

t01=(Wg01/Vs)*(A0./(A2-A0));
```

```
t02=(Wg02/Vs)*(A0./(A3-A0));

plot(Vg,t0,'b',Vg,t01,'g',Vg,t02,'r');
```

Switching time vs thickness

```
A=1.4e-4:0.1e-4:2.3e-4;

A1=1.4e-4;

A2=1.6e-4;

A3=1.5e-4;

W=100e-4;

Wg1=1e-4:1e-4:10e-4;

Wg0=1e-4;

Wg01=2e-4;

Wg02=3e-4;

Nd=3.9e16;

u=500;

q=1.60213e-17;

e=8.859e-13;

k=1.38e-23;

T=300;

Na=3e16;

ni=5e-10;

Vs=0.8e7;
```

```
Vd=0.1;

Vg=-1;

Es=Vs/u;

Vbi=0.0259*log (Na*Nd/(ni*ni));

A0= (2*e*(Vbi-Vg))/(q*Nd);

t0= (Wg0/Vs)*(A0./(A-A0));

t01= (Wg01/Vs)*(A0./(A-A0));

t02= (Wg02/Vs)*(A0./(A-A0));

t1= (Wg1/Vs)*(A0./(A1-A0));

t2=(Wg1/Vs)*(A0./(A2-A0));

t3=(Wg1/Vs)*(A0./(A3-A0));

plot(A,t0,'b', A,t01,'g',A,t02,'r');
```