CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

Study of Analytical Determination of Parasitic Resistances in Gallium Nitride (GaN) MESFET'S

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By

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ABSTRACT

STUDY OF ANALYTICAL DERTERMINATION OF PARASITIC RESISTANCES IN GALLIUM NITRIDE (GaN) MESFET'S

By

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Master of Science in Electrical Engineering

In this project, a physics based analytical model is proposed for Gallium Nitride (GaN) based metal semiconductor field effect transistor (MESFET) by using MATLAB software. The analytical model has been developed to extract the parasitic resistances and the result shows an accurate simulation to understand the intrinsic and extrinsic parameters of GaN MESFET device. In order to understand the transit properties, the electrical parameters such as drain resistance, gate resistance and source resistance have been determined by varying the drain and gate voltages. The Microwave FET's in digital and analog applications shows the degradation by these parasitic resistances. The source resistance R_s and drain resistance R_d are exponentially decreased and R_g is exponentially increased by varying the drain voltage V_{d2} for different values at this constant gate voltage and the conductance of source and drain is increased when the conductance of gate is decreased. These effects reflected to the device performance by degrading frequency response and switching performance. The results of drain voltage versus source resistance, drain resistance and gate resistance are shown in results and discussion chapter.

CHAPTER-1

INTRODUCTION

In recent years the wide-band gap semiconductors, Gallium Nitride (GaN) and Silicon Carbide (SiC), have received increased attention because of their potential for use in a wide variety of high-power high-frequency device [1, 2]. Their unique material properties, high electric filed breakdown due to the wide band gap, and high saturates electron drift velocity are what give these materials their tremendous potential in the high frequency power device area. In future these devices will become the microwave amplifier of choice for the rising wireless communication market. In this regard, few studies have been achieved on GaN MESFET's as compared to HFET's, whereas the MESFET's epilayers are easier to realize and the physical effects are easier to interpret (no heterojunction and piezoelectric strain effects). Hence, GaN MESFET's devices have been investigated [3].

The Gallium Nitride (GaN) material has excellent electrical properties that make it a viable alternative to SiC for microwave high-power and high temperature application. GaN based devices are extensively pursued for potential applications in high power microwave circuitries. GaN HEMT's with output power of 9.8W/mm at 8 GHz [4], f_T=101GHz and f_{max}= 155 GHz, and operating temperature of 750^0 C have been reported [5]. There is much interest in nitride semiconductor material for a variety of applications. Growth technology is rapidly progressing and theoretical work is yielding material transport data. GaN also has potential for producing microwave power devices capable of high-temperature operation. For a doping concentration of $1 \times 10^{17} cm^{-3}$, the theoretical low field electron mobility of GaN is about 1500 cm^2/Vs, which is higher than the values for any of the SiC polytypes. The power losses of GaN devices will be lower than those in SiC devices at high frequency operation as well as at low- frequency operation. Recently, Kahn et al, have demonstrated microwave operation of AlN/GaN heterostructure field-effect transistors (HFETs) with a maximum oscillation frequency f_{max} of 3 5 G H, this number is compared favorably with that for a 6H-SiC MESFET. In particular GaN is of interest for optical devices throughout the entire visible spectrum and extending far in to the UV, a blue-light-emit-ting GaN diode has been demonstrated,

along with its potential for optical devices. GaN-based heterojunction field effect transistors (FETs) that offer low field mobility, high band gap energy of 3.4eV and a high breakdown electric field of 4 V/cm are highly attractive for high power and high-temperature applications at microwave frequencies [6]. Recently, GaN HEMTs with a power output up to 9.8W/mm at 8GHz have been demonstrated. With SiC as a substrate, GaN FETs have been operated up to 750^0 have been demonstrated by Daumiller [7]. With a high electron saturation velocity of 3×10^7 cm/s and low dielectric constant with a commensurate lower capacitance, GaN –based devices are potential choices for high-frequency operation [8, 9]. The heat tolerant heterojunction bipolar transistor (HBT's) and high power is the GaN electronic device can be important components of integrated systems designed for high frequency and high speed applications, for example, in satellites and all electric aircraft. GaN based field- effect transistors (FET's) are projected to be highly useful for power amplification and switching in high temperature and high power environment [10]. There is a strong development effort on wide gap power devices, with lesser efforts in GaN for achieving the higher stand-off voltages, which should have benefits that Si-based or electromechanical power electronics cannot attain. The higher stand-off voltages should eliminate the need for series stacking of devices and the associated packaging difficulties. In addition, these wide bandgap devices should have higher switching frequency in pulse-width-modulated rectifiers and inverters [11].

The power solid –state devices by deploying Kw Level RF power source for energizing super conducting structures [12]. Earlier, utility of Solid State Power Amplifier (SSPA), at Radio frequency and microwave (RFM), was limited to driver amplifier [13], providing few hundreds of watts, for driving vacuum tube amplifiers. Now, with the advent of superconducting accelerating structures, solid state technology, in parallel, has crossed kW level power regime as demonstrated in particle accelerators like Soleil synchrotron in France [14]. Along with getting clean RFM power (free from phase noise and spurious) solid state device failure rate reported from Soleil is 3% per year including infant mortality. Numerous advantages of SSPA, compared to vacuum tube counterpart, is the main driving force behind rapid development of kW level SSPA [15]. Output power of individual solid state device is rather modest, being of the order of few hundred of Watts. Hence kW level RF power is obtained by summing power output

of multiple devices, developed in the form of amplifier modules. Power summing action is achieved by power divider and combiner (PDC) structures. Unlike communication field, RFM signal is monotonic except pulse modulation in some cases. For amplifier modules, in present work, focus was set on suitable, efficient and easily realizable impedance matching network. Apart from amplifier design, design of novel PDC, based on simplified method, incorporating radial strip line structure; without isolation resistor and external tuning mechanism, has been demonstrated. For directional coupler, method suggested by Teppati has been modified by removing micro strip line [16, 17]. All of these components developed and tested independently, should work as ensemble also. To demonstrate this, SSPA with 2kW output power was developed, initially at 352MHz and later on at 505.8 MHz from this, improved 16-way power combiner has been developed for upcoming higher power (8kW) amplifier. For all of these RF components, vector and scalar measurements were carried out for validating design procedure. Followed this, high power continuous wave (CW) and pulse RF testing was carried out.

In the past few years, growing interest has been paid to the wide band gap materials such as GaN, because of its low thermal generation rates and high breakdown fields. The use of GaN-based devices for efficient, linear and high power RF amplifiers are expected to create an entirely new and low life cost advances to create an entirely new and low life cycle cost advanced multifunctional RF systems (AMRFS) for military applications GaN MESFETs have received much attention as its structure is simpler to analyse than that of HEMTs [18]. Transconductance g_m of the device is most important indicators of the device quality of microwave applications. It is significantly affected by device dimensions and channel material properties. In semi empirical model of GaN MESFET, when operating under small signal conditions, the microwave transistors are characterized by admittance (Y) and scattering (S) parameters. Most of the reported work in this area is either experimental [19, 20] or based on Monte Carlo simulations [21, 22]. Recently, Islam and Anwar have modeled nonlinearities in GaN MESFETs using large signal physics-based model, which takes in account frequency dispersion of transconductance and output resistance [23]. The RF and microwave designing of FETs using neural networks physics-based training for active device models [24]. All other parameters of the MESFET equivalent circuit including input resistance (R_i) assumed to

be constant, the model has been demonstrated and verified for a uniformly doped 0.3μm×100μm GaN MESFET using ATLAS 2D device simulator over a wide frequency ranging from 1 to 100GHz [25]. To depict the significant of taking into account the frequency dependence of parasitic capacitances, the results are also compared with the parasitic elements-dependent analytical model for admittance [26]. Short circuit connections are required for the measurement of Y parameters, and at microwave frequencies, stray inductances can cause short circuits to act like open circuits. Therefore, scattering parameters that measure the incident and reflected waves from both ports of the device can be used , S parameters can be derived from Y parameters [27].

GaN also has the required properties for these applications and can be incorporated into heterojunction device structures. The DC characteristics of GaN MESFETs with a 4μm gate length have been recently reported, the device fabrication and microwave performance of 0.7μm gate length GaN MESFETS where the active channel was grown on a highly resistive GaN layer. GaN epilayers are grown on (1 1 1) oriented single crystal diamond substrate by ammonia- source molecular beam epitaxy [28]. It is found that a two-dimensional epitaxial wurtzite GaN film is obtained and in each step of the growth is monitored in situ by reflection high energy electron diffraction. The two dimensional epitaxial wurtzite GaN film is obtained and the surface morphology is smooth the rms is roughness is as low as 1.3nm for $2\times 2\ \mu m^2$ scan. The GAN band edge is centered at 3.469 eV with a line width of 5 meV and these results demonstrate that GaN heteroepitaxially grown on diamond opens new rooms for high power electronic applications [29].

Wide band gap semiconductors are extremely attractive for the gamut of power electronics applications from power conditioning to microwave transmitters for communications and RADAR The AlGaN/GaN HEMT seems the most promising in terms of various materials and device technologies. There is strong interest in developing wide band gap power devices for use in the electric power devices for use in the electric power utility industry. With the onset of deregulation in the industry, there will be increasing numbers of transactions on the power grid in the US, with different companies buying and selling power. The main applications are in the primary distribution system

~100-2000kVA and in subsidiary transmission systems ~ 1-50MVA. A major problem in the current grid is momentary voltage sags, which affect motor drives, computers and digital controls. Therefore, a system for eliminating power sags and switching transient would dramatically improve power quality [30-33]. Some desirable attributes of next generation, wide gap power electronics include the ability to withstand current excess of 25kv, provides rapid switching, maintain good thermal stability while operating at temperature above 250 C without bulky heat-dissipating systems. In particular, the absence of Si devices capable of application to 13.8KV distribution lines opens a major opportunity for wide gap electronics [34]. The use of GAN material and GaN-based heterostructure in high power applications has received considerable attention now a days. The study of energy flow between hot electrons and their surroundings is therefore of particular interest in the GaN. Through the application of an electric field the electrons gain the energy, they cease to be in equilibrium with the photons, but equilibrate with each other via electron- electron interactions. This forms a hot electron system whose temperature may significantly exceed that of the lattice phonons. The emission of acoustic and optical phonons by a hot electron gas sets the energy relaxation time, which in turn determines the characteristic time for hot electrons to relax to the lattice temperature. At low temperatures, we expect the dominant method of cooling to be the emission of acoustic phonons through acoustic deformation potential scattering. At higher temperatures ~ above 100 K the faster emission of polar optical photons is expected to dominate electron cooling. Energy then flows from the GaN lattice photons to the photons in the sapphire substrate before flowing to the bath. Knowledge of the energy relaxation time is of fundamental importance and is also relevant to device design. In high-power devices in particular, understanding the processes that govern the cooling of hot carriers is useful in accessing device performance [35].

The modern communication systems urged the need of monolithic microwave integrated circuits (MMICs), which consists of many metalized semiconductor field effect transistors MESFETs on the same chip. The need of accurate MESFET devices would facilitate the use of circuit design and analysis tool to allow better use and evaluation of these devices. Most of the currently available models in computer-aided design (CAD) packages are circuit models. It is well known that small-signal model

provides a useful tool for the device performance analysis such as Gain, noise. The small-signal equivalent circuit (SSEC) which is commonly accepted is formed of fifteen different frequency-independent elements in that eight of them corresponding to the external parasitic effects and normally considered independent of the bias point, and the other seven describing the intrinsic behavior of the FET and dependent on the biasing conditions [36].

About Parasitic Resistances

Parasitic Resistances is an extrinsic parameter; the extrinsic device adds the external parasitic elements which are associated with the leads and contacts to the devices. In the MESFET, the gate is close to the drain. Falls of tensions that produced in parasitic elements situated between the contacts of the source and the drain and the active region under the gate degrade very appreciably the noise figure and limit the power gain of the transistor. It is therefore essential to understand the origin of these parasitic resistances. Several techniques have been proposed to determine these parameters,' R_s' and 'R_d'. Most of the methods require measurements at different drain and gate voltages [37-39]. In cold Field effect transistor (ColdFET) the drain-to source bias V_{DS} is set to zero, while the gate electrode is sufficiently forward-biased $V_{DS} > 0V$. Although, S-parameter measurements give an accurate determination of the total source-to-drain resistance, it is difficult to determine accurately the temperature coefficient of the separate parameters R_s , R_d and the channel resistance is difficult to determine accurately [40]. The gate resistance R_g has long been recognized as a critical parameter that degrades the noise figure and limits the power gain of MESFET's [41].

In the development of microwave FET nonlinear models like GaN, GaAs or SiC, the bias dependence of the intrinsic elements should be known in order to establish an appropriate mathematical function to describe it. De-embedding of parasitic elements is needed to determine the intrinsic device elements.one of the first approaches to determine the parasitic elements of GaN FET was developed by Chigaeva , the method is based on the ides used for GaAs [42, 43]. The large gate forward currents could produce irreversible and catastrophic damage to the gate. The knowledge on the schottky diode resistance R_0 is used to calculate the gate resistance R_g [44, 45]. AlGaN/GaN high-

electron mobility transistors (HEMTs) have attracted much attention because of their excellent potential for microwave power performance. Despite steadily improving performances, AlGaN/GaN HEMTs have not yet fully lived up to power output, linearity, and amplifier efficiency expectations because of no idealities such as the current collapse effect [46]. MESFET and HEMT parasitic resistances of R_S and R_D are commonly determined by so-called "ColdFET" microwave measurements, wherein the drain-to-source bias V_{Ds} is set to zero, while the gate electrode is sufficiently forward-biased (V_{DS}> 0V), the use of ColdFET measurements implicitly assumes that R_s and R_D are bias-independent because the ColdFET test conditions have little to do with actual device operating biases, and do not allow for R_s and $R_D$variation [47, 48].

For the development of Gallium Nitride device technology an accurate modeling and characterization and optimization of GaN field-effect transistors (FET's) are very important. The dc measurement techniques including the so-called end-resistance and gate-probe measurements have been widely used because of their simple and direct measurements .The most of dc measurement techniques are based on well-known diode current equation, they can measure the parasitic resistances only at the gate conduction region (forwardly biased gate region). The ac techniques usually for normal ColdFET technique for V_{ds} = 0V and V_{gs} >V_t is most popular. While designing and developing microwave circuits an accurate and fast parameter extraction for modeling of MESFET's is important. The performance of both digital and analog/microwave FET's is degraded by parasitic resistances [49]. The transconductance and noise figure and power consumption are strongly affected by parasitic resistances [50]. Measurement of the series parasitic resistance is difficult requiring multiple measurements, accurate determination of parameters such as threshold voltage, build-in- voltage, and gate diode ideality factor and curve fitting to a region of applicability of a particular conduction model [51]. The source R_S and drain R_d resistances as well as the channel R_{ch} resistance and gate diode ideality factor which meets the aforementioned specifications is presented and this technique is similar to the end contact resistance method, expect that the gate electrodes to measure the source and drain resistances, respectively[52]. The Channel resistance is determined by subtracting the source and drain resistance from the total

source to drain resistance, and the gate ideality factor is determined from linear fit to the data at high values of drain current. The technique relays on the current crowding phenomenon utilized in the contact end resistance measurements [53]. It offers the advantage of having the same probe configuration utilized for the other standard I-V characteristics measurements and thus, can be performed with a series of tests in a automated setup on a wafer probe test level. The tests are performed at relatively low source-drain biases so that the effects of backgating in nonpolar structures should be insignificant [54]. There are two different types of coldFET extraction, one is reverse coldFET and other one is forward coldFET. The reverse coldFET is used to extract the parasitic capacitance, the MESFET gate is biased below pinch off whereas the drain is biased at zero volts, therefore no DC currents flows in the devices. In forward coldFET is used to extract the series resistance and series inductance, the MESFET gate is forward biased above the gate turn on voltage, the drain is biased at zero volts, the depletion region becomes small with forward gate bias [55].

CHAPTER-2

STUDY OF GALLIUM NITRIDE (GaN) MATERIAL

2.1 Background

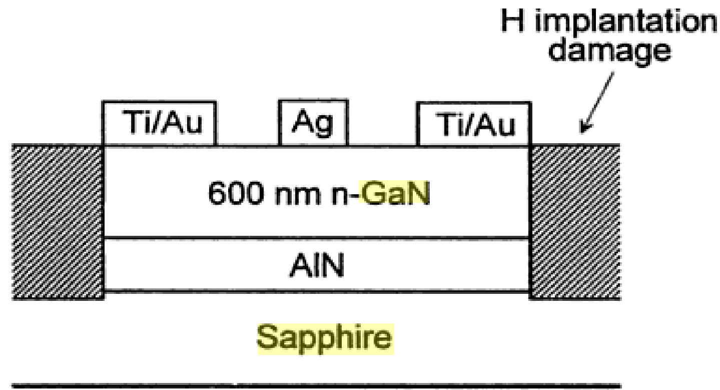

Fig. 2.1: Cross section of the first reported GaN MESFET

The first GaN MESFET was reported in 1993 by Cree Inc. The cross section of this device is shown in Fig. 2.1. Unintentionally-doped-type GaN was grown on a sapphire substrate using a thin AlN nucleation layer. The thickness of the GaN is 6000A^{o}and it had 300K hall mobility of 350 cm^2/Vs. and with a device transconductance of 23mS/mm. For the last three decades or so, the III-nitride semiconductor material system has been viewed as highly promising for semiconductor device applications at blue and ultraviolet (UV) wavelengths in much the same manner that its highly successful As-based and P-based counterparts have been exploited for infrared, red and yellow wavelengths. As members of the III-V nitrides family, AlN, GaN, InN and their alloys are all wide band gap materials, and can crystallize in both wurtzite and zinc-blende polytypes. Another area gaining a lot of attention for III-V nitrides is high temperature/high power electronics. The interest stems from two intrinsic properties of this group of semiconductors. The first is their wide bandgap nature. The wide bandgap materials such as GaN and SiC are promising for high temperature applications because they go intrinsic at much higher temperatures than materials like Ge, Si and GaAs. The Fig.2.2: shows the bandgap of hexagonal and cubic GaN, AlN and InN and their alloys

Vs lattice constant and have direct room temperature band gaps of 3.4, 6.2 and 1.9 eV, respectively [56].

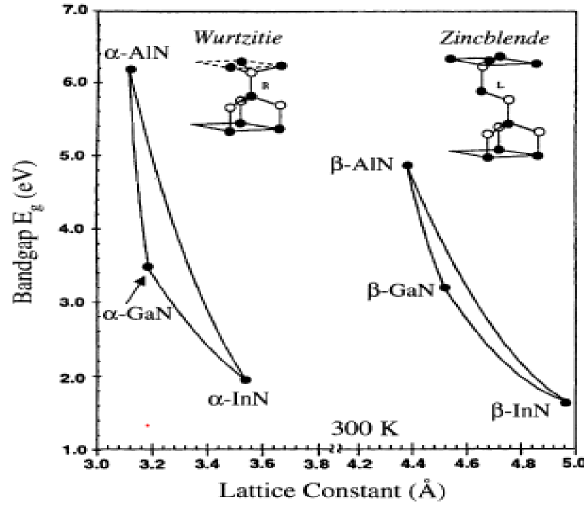

Fig. 2.2: Bandgap of hexagonal and cubic InN, GaN, and AlN and their alloys Vs lattice constant

It means that GaN power devices can operate with less cooling and fewer high cost processing steps associated with complicated structures designed to maximize heat extraction. The second attractive property of III-V nitrides is that they have high breakdown fields. The critical electric field of the breakdown scales roughly with the square of the energy band gap, and is estimated to be > 4 MV/cm for GaN as compared to 0.2 and 0.4 MV/cm for Si and GaAs, respectively. The Fig. 2.3 is a plot of avalanche and punch through breakdown of GaN Schottky diodes calculated as a function of doping concentration and standoff layer thickness.

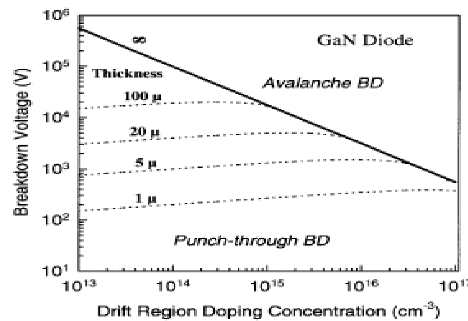

Fig. 2.3: Calculated breakdown voltage as a function doping concentration and thickness of the drift region in GaN M- n- n+ diodes

It can be seen that 20 kV device may be obtained with approximately 100 μm thick GaN layer with doping concentration <10^{15} cm^{-3} [57].

GaN has also excellent electron transport properties, including good mobility, and high saturated drift velocity as shown in Fig. 2.4, thus making this material suitable for general electronics, and promising for microwave rectifiers, particularly. The material properties associated with high temperature, high power, and high frequency application of GaN and several conventional semiconductors are summarized in Table 1. CFOM stands for Combined Figure of merit for high temperature/high power/high/frequency applications. It is anticipated that GaN may eventually prove to be superior to SiC in this area [58].

Property	Si	GaAs	4H-SiC	GaN
Bandgap E_g(eV)	1.12	1.42	3.25	3.40
Breakdown field E_B(MV/cm)	0.25	0.4	3.0	4.0
Electron Mobility $\mu(cm^2/Vs)$	1350	6000	800	1300
Maximum Velocity $V_s(10^7 cm/Vs)$	1.0	2.0	2.0	3.0
Thermal conductivity % (W/cm K)	1.5	0.5	4.9	1.3
Dielectric constant ε	11.8	12.8	9.7	9.0
CFOM	1	8	458	489

Table 1: Comparison of 300K semiconductor material properties

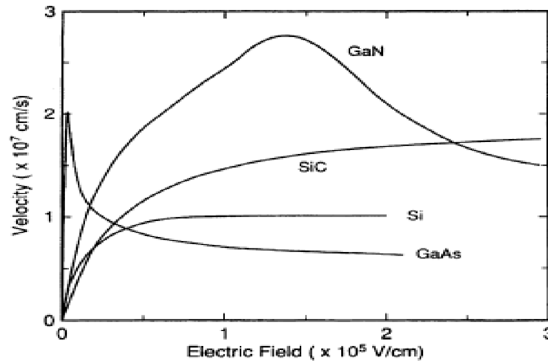

Fig. 2.4: Electron drift velocity at 300 K in GaN, SiC, and GaAs computed using Monte Carlo technique

The strongest feature of the III-V nitrides compared to SiC is the heterostructure technology it can support. Quantum well, modulation-doped heterointerface, and heterojunction structure can all be made in this system, giving access to new spectral regions for optical devices and new operation regimes for electronic devices. From this point of view, III-V nitrides can be considered the wide band gap equivalent of the AlGaAs/InGaAs system which has set the modern benchmark for microwave device performance.

Other attractive properties of III-V nitrides include high mechanical and thermal stability, large piezoelectric constants and the possibility of passivation by forming thin layers of or with band gaps of 4.3 and 9.2 eV, respectively. In addition, AlN has received considerable attention for its insulating property, particularly as a potential isoelectronic insulator for GaAs field effect transistors (FETs). Substantial research on III-V nitrides growth was initiated in early 1960s. However, they have trailed way behind the easier-to-grow Si and GaAs semiconductors on the development curve. Nearly 30 years later, Si and GaAs have been pushed to their theoretical limits, while nitrides are just beginning to show their promise. The technological spin-offs came late because ideal substrates could not be found and the consequent growth of GaN thin films contained substantial concentration of defects and had high n-type background. Even in films having relatively small background electron concentration, p-type doping could not be achieved until recently [59].

2.2 GaN Material Growth Limitations

One particular difficulty in the growth of GaN thin films is the unavailability of sufficiently large (>1 cm) single crystals for use as substrate for homoepitaxial growth. Thus up to now, heteroepitaxial growth has been a practical necessity and the choice of substrate is critical. Possible substrate materials should have low thermal expansion and lattice mismatch with the grown crystals. Also, they should be unaffected by the growth chemistries (such as NH_3 or H_3) at high growth temperatures (in excess of 1000 Degree Celsius in some cases). Under these constraints, sapphire Al_2O_3 and SiC are the most popular substrate materials used currently. When hexagonal GaN is grown on the (0 0 0 1) basal plane of Al_2O_3, a lattice misfit of ~13% exists at the growth temperatures. A high density of threading dislocations is observed in GaN layers. The residual strain is

comparable to the lattice misfit between 6H-SiC and GaN, and result is comparable dislocation densities observed [60]. Today, SiC substrates, though more costly, are of increasing interest for high temperature high power devices like transistors due to their good thermal conductivity and possibility of n- and p-type doping. The materials with a close lattice match with GaN, such as $LiAlO_2$ and $LiGaO_2$ were also used for epitaxial substrates [61, 62]. However, the grown GaN lacked the desired electronic properties due to either the rough growth or unintentional contamination from the substrates. The ideal candidate substrate is clearly a GaN wafer. Several research groups are investigating the growth of the bulk GaN crystals and very thick films through various techniques. However commercially available large area GaN wafers appear to be at least an away. The nitride community is, therefore, challenge faced with growing of heteroepitaxial films having large MISFITs [63-65].

Many epitaxial thin film growth processes have been developed, including molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE) metal organic chemical vapor deposition (MOCVD) and derivatives of these methods. In the past few years, MOCVD has evolved as a leading technique for production of III-V nitrides optoelectronic and microelectronic devices. One remarkable application worthy to be mentioned is the achievement of super-bright blue LEDs. Characteristics of this method include the use of high purity chemical sources, a high degree of composition control and uniformity, high growth rates, large scale manufacturing potential and the ability to grow abrupt junctions [66-68].

Initially the growth of GaN was performed directly on sapphire and SiC substrates, with large crystalline defects threading vertically from the substrate interface through the newly deposited thin film. The wafer usually had rough surfaces mainly caused by the 3D - growth mode. In 1986, Amano succeeded in remarkably improving the GaN surface morphology as well as the electrical and optical properties by deposition of a thin low temperature AlN buffer layer prior to the high temperature growth of GaN. The essential role of this buffer is serving as a template for the nucleation of growth and promotes lateral growth of the GaN film due to the decrease in interfacial free energy between the film and the substrate. Although the buffer layer has reduced the effects of

the lattice mismatch, the densities of the threading defects in these thin films are still in the range of 10^9–10^{10}cm^2, and on the order of one million times higher than in other semiconductor systems. These defect-laden materials, to date, have had a surprisingly small effect on the performance of both optical and electronic devices, but they may raise major questions as to the long-term stability of these devices. It is unlikely that the full promise of GaN and related alloys can be realized without a major reduction in the defect densities in the grown materials [69].

In 1994, the lateral epitaxial overgrowth (LEO) technique was employed to further improve the quality of the heteroepitaxially grown GaN, resulting in a marked reduction in defect density [70]. In this method, a layer of GaN grown by MOCVD is covered with 100-200 nm of amorphous $Sio_2$and Si_2N_4 with ex situ techniques. Small circular or rectangular windows are then etched through to the underlying GaN. A GaN film is subsequently regrown under conditions such that growth occurs epitaxially only in the windows and not on the mask. If growth continues, lateral growth over the mask eventually occurs. Since most of the extended dislocations propagate in the growth direction through GaN, very few threading dislocations are visible in the regrown GaN that extends laterally over the mask, the density of dislocations reaching the surface of LEO GaN was in the 10^4 - 10^5 cm^2 range, while the film over the window regions still contained high levels of the threading defects [71].

A refined approach to a nearly dislocation free GaN substrate for devices can be employed by two successive LEO steps with the mask of the second step positioned over the opening defined by the mask of the first step, thus blocking the defects that grown out of the first windows. This complicated procedure offers the possibility of eliminating the disadvantages of heteroepitaxy, and will be important until GaN substrates become available.

In addition to growing GaN films with low defect densities, another key requirement for fabricating devices is the ability to precisely control the desired electrical properties of the thin film. In general, wide bandgap semiconductors are difficult to dope due to native defects. When the enthalpy for defect formation is lower than the band gap energy, the probability of generating a defect increases with the bandgap, i.e. the energy

released by donor-to-acceptor transition. Particularly for GaN, MOCVD grown material is commonly n-type, and N-vacancy was long believed to be the dominant donor. Many attempts have been made to avoid N-vacancy formation by growing GaN at high pressures and high temperatures. Efficient n-type doping of GaN through incorporation of Si during the growth proved relatively easy to achieve. High doping can also be achieved by implantation of Si or Group VI donors. Recently, Burm have shown a shallow Si implant at high dose to produce a doping density of, resulted in an extremely low ohmic contact resistance of using Ti/Au contacts [72, 73].

2.3 Defects in a Bulk GaN

Bulk GaN crystals of the wurtzite structure were grown from a solution of atomic nitrogen in liquid gallium under high nitrogen pressure (up to20 kbars) at temperatures in the range 1500 -1800 K. GaN crystals of platelet shape were typically of 1-3 mm in lateral size and 0.1-0.5 mm in thickness. They often had the shape of elongated hexagons with the longest dimension along axis and the surfaces of the platelets parallel to c-plane. The two platelet faces differ in their roughness: one is almost atomically flat while the opposite one can be very rough. In some cases a series of inverted pyramids terminated the rough surface. However, about 70-90% of the total plate thickness was defect-free.

The more rough the surface, the higher was the defect density observed. Formation of SFs is considered as a growth mistake. The structure of basal and prismatic faults in wurtzite has been described by Blank. From a crystallography point of view the basal faults are equivalent to local transitions from the hexagonal to the cubic structure within a few (0001) atomic planes. In hexagonal GaN the bonds have mirror symmetry while in the cubic structure bonds are rotated 600 with respect to nearest neighbors. The local change of crystal symmetry is from 2H to 3C. The Fig.2.5 shows three types of (I_1,I_2 and E) of basal stacking faults observed in the bulk GaN with one, two and three cubic bilayers, respectively. Each bilayer of the cubic GaN is situated in one of three possible positions assigned as A, B, C with the ideal stacking sequence of ... ABCABC ... while in hexagonal GaN each bilayer has only two possible positions, A and B, with the perfect sequence being ..ABABAB.. SFs locally change the bond arrangement and

introduce a number of atomic planes with the zinc-blende structure (ABC) in the Wurtzite GaN (AB).

2.4 Defects in Epitaxial GaN Crystals

While stacking faults are the predominant defects in bulk GaN crystals, dislocations lying almost parallel to the c-axis dominate in epitaxial GaN layers in Fig.2.6. Dislocations in the epitaxial GaN often are arranged as a network of small angle boundaries forming the columnar structure typical for epitaxial layers of hexagonal materials. The difference in defects for bulk as compared to epitaxial crystals is associated with the totally different growth conditions. Indeed, epitaxial GaN layers grow in the c-direction on top of the substrate with a high lattice and thermal mismatch. Therefore, most defects in epitaxial GaN layers are generated at the interface and then propagate in the growth direction. Due to a high density of vertical dislocations and the c-axis growth direction, SFs in the epilayer cannot propagate for long distances as was observed in bulk crystals in, the lengths of SFs in epitaxial GaN were much smaller than those in the bulk crystals.

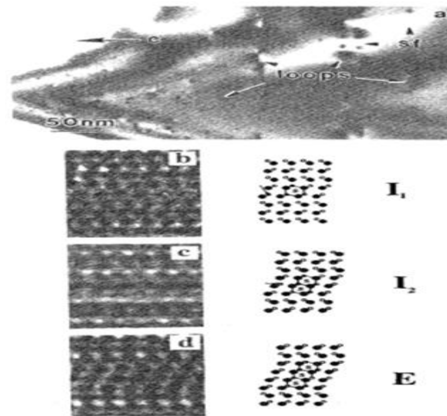

Fig.2.5: Three types of basal stacking faults (b-d) observed in such a region

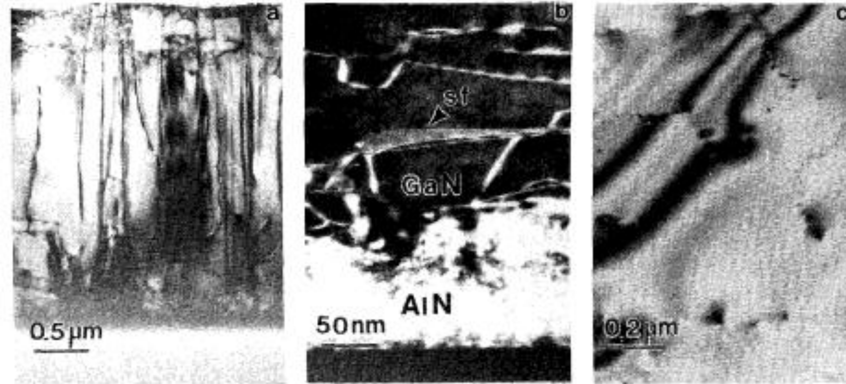

Fig.2.6: Cross-sectional TEM image of epitaxial GaN layers of grown on sapphire substrate with a AlN buffer layer

Most of the dislocation interactions resulting in annihilation of dislocations happen near the interface where dislocation density is high and spacing between them are relatively small. Threading dislocations can propagate from the substrate or can be formed during coalescence of 3D islands during the initial stages of the GaN growth. Therefore, a buffer layer might decrease the dislocation density in the GaN layer. A buffer layer can reduce the roughness of the substrate surface and prevent the detoriation of GaN at the interface due to diffusion of nitrogen into the substrate. An AlN buffer layer typically has a “mosaic” structure with a high density of defects. It contains small crystalline sub-grains slightly disoriented around the c-axis, but perfectly oriented in the c-plane. The structure of the buffer layer influences the arrangement of threading dislocations in the GaN layer resulting in the formation of a network of small angle boundaries with both tilt and twist components. Some of threading dislocations bend into the basal plane to become segments of misfit dislocations parallel to the interface.

Since conductivity is proportional to the product of carrier concentration and Hall mobility, another goal for GaN used in device applications is to obtain highest Hall mobilities possible. Fig. 2.7 summarizes the measured electron mobility in n-type GaN, along with the results obtained from Monte Carlo simulation. As can be seen, the experimental data is roughly half of the calculated value, possibly due to significant scattering from impurities and defects in the state-of the- art materials.

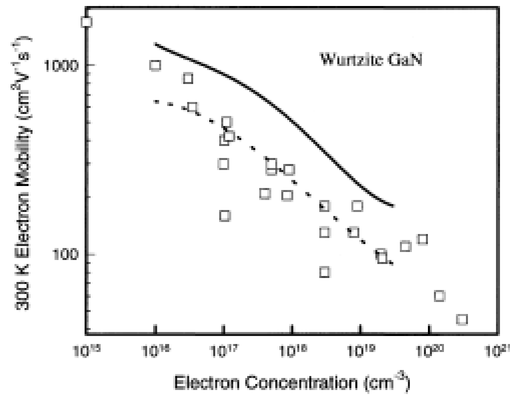

Fig. 2.7: A survey of 300 K GaN electron Hall mobility values as reported by various groups

The solid line shows the calculated results for uncompensated n-GaN. The III-V nitrides are expected to be made p-type by substituting Column II elements such as Zn, Mg Be and Ca on for Ga sites to form single acceptors. However, all of these divalent elements form deep acceptors, the shallowest being Mg with ionization level of 0.17 eV which is still many kTs above the valence band edge of GaN. At this acceptor level, one should only expect <10% of the Mg atoms to be ionized at room temperature, which means the Mg concentration needs to be approximately two-orders of magnitude larger than the desired hole concentration. When MOCVD is used as the growth method, it has been difficult to obtain p-type conductivity. It was later found that hydrogen plays a crucial role in passivating the Mg acceptors, and creates a neutral complex Mg-H that prevents the formation of holes in GaN. It was first shown by Amano, that p-type conductivity can be achieved by activating Mg-doped GaN using low-energy electron irradiation. Nakamura demonstrated subsequently that the activation of Mg can also be realized by thermal annealing at ~7000 C. Note that MBE grown GaN doped with Mg may be p-type without a thermal activation process, because of the absence of hydrogen and H-N radicals during growth. In addition, p-type doping was also achieved by implant of Ca or Mg into GaN, followed by high temperature annealing (~11000 C). The highest hole concentration reported so far is ~10^{18} cm^{-3}, and the typical hole mobility is very low, often 10 cm^2/Vs or below, but allowing the realization of p-n junctions. Achieving low resistance Ohmic contacts to the GaN layers with poor p-type doping concentrations has proved to be troublesome. Recently, Brandt found that by compensating be with O, a

neutral dipole is formed that does not scatter the holes. Hence a record high hole mobility of 150 cm^2/Vs was obtained. This may be the ideal contact layer for GaN based devices requiring a p-type ohmic contact.

The current level of the progress in the development of GaN commercially viable devices, namely GaN based-LEDs, LDs and UV detectors, has been the direct result of the realization of high quality layers of GaN, AlGaN, InGaN, and relatively recent achievement of p-type conduction in GaN. The first p-n junction LED was demonstrated by Amano in 1989. Following this, Nichia Chemical Industries announced the commercial availability of blue LEDs with high efficiency and luminous intensities over 1 cd. In subsequent years, high brightness single quantum well structure blue, green and yellow InGaN LEDs with luminous intensities above 10 cd have been commercialized. In 1996, Nakamura reported the first current-injection GaN-based LDs with separate confinement heterostructure, and subsequently achieved continuous wave (CW) lasing at room temperature. Fig. 2.8 schematically shows the cross-section of a nitride-based laser diode. The active layer is an InGaN multi-quantum well with a large number of well layers. GaN and AlGaN were used as the waveguide and cladding layers, respectively. The mirror facet was formed by numerous methods, including dry etching, polishing or cleaving.

Surprisingly, the high-density dislocations resulting from the heteroepitaxial growth on sapphire in these optical devices did not appear to be efficient non-radiative centers, as they are in other III-V materials. However, the crystalline defects do affect the device reliability. Nichia employed the LEO growth technique for their blue LDs and achieved an increase in device lifetime from a few hundred hours to an estimated 10,000 h. Another major problem limiting diode performance is high specific contact resistance of Ohmic contact on the p-GaN side of the junction. Present lateral GaN lasers suffer significant IR drops due to poor p-type doping and Ohmic metallization.

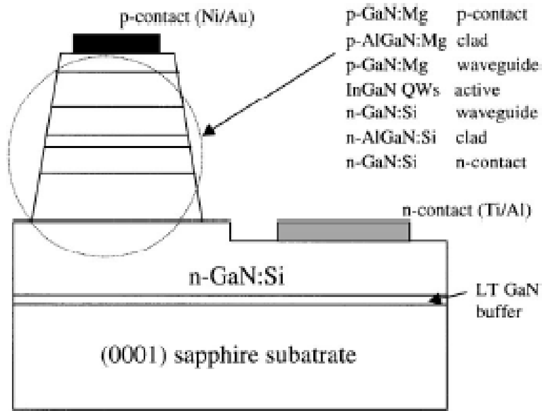

Fig. 2.8: Cross- sectional view of a typical structure of GaN-based laser diode

The nitride material growth technology that supports the optical device efforts has also proven to be compatible with the development of electronic devices. In the past several years, the electronic device development has emphasized field effect transistor (FET) structures, because this important class of devices places smaller demands on the growth and fabrication technique compared to bipolar transistors. The rapid progress that has been made, especially in modulation-doped FETs (MODFETs), has been sufficient to show that GaN and related alloys will play a significant role in the future development of high temperature, high power, and high frequency electronic devices.

The Fig.2.9 presents a schematic representation of a GaN/AlGaN heterostructure. Due to the large conduction band discontinuity, the electrons diffusing from the large bandgap AlGaN into the smaller bandgap GaN form a two-dimensional electron gas (2DEG) in the triangle quantum well at the interface, which is the hallmark of MODFET. The sheet carrier density of the 2DEG was found to be further enhanced by the strong pizeoelectronic effect in GaN.

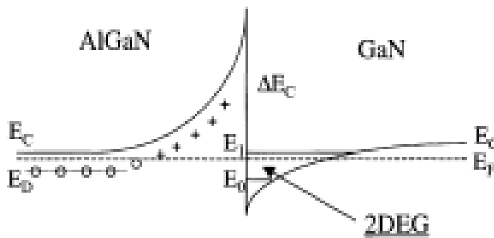

Fig. 2.9: Condition band structure of a modulation-doped structure

Pizeoelectronic coefficients in nitrides were measured to be about an order of magnitude higher than in traditional Group III-V semiconductors. Theoretical simulations have predicted a high peak electron velocity of ~ cm/s and an electron mobility of ~2000 cm2 /Vs in the GaN channel at room temperature at a carrier concentration of. Gaska investigated the highest measured Hall mobility at room temperature was 2019 cm2 /Vs , and increased approximately fivefold to 10,250 cm2 /Vs below 10 K for growth on 6H SiC substrate. In 1993, Khan demonstrated the first AlGaN/GaN MODFET, with a g_m of 23 ms/mm and 2DEG mobility of 563 cm^2 /Vs at 300 K. They also reported the first microwave results with f_T of 11 GHz and f_{MAX} of 14 GHz. In the early stages, the MODFETs exhibited very low transconductance and relatively poor frequency response. This is consistent with the defect-laden nature of the early GaN and AlGaN layers. With improvements in the materials quality, the transconductance, current capacity, drain breakdown voltage are all increased to the point that GaN based MODFETs are now strong contenders in the arena of high power devices/amplifiers. To date, the highest power density achieved for a $0.45 \times 125\mu m$ GaN MODFET is 6.8 W/mm at 10 GHz and associated gain of 10.65 dB. The operation temperature has been pushed to 750^0 C by employing a thermally stable Pt/Au gate contact.

The published performances of epitaxial GaN-based MESFETs demonstrate that all the required components for a MESFET based technology are in place, i.e. an appropriate high resistivity buffer/substrate combination has been developed for doped layer epitaxial growth, FET channels can be grown with thin n^+ contact layers on which Ohmic contact with adequate contact resistances have been achieved, gate metallization which can pitch off the channel and support a high drain bias have been demonstrated, and it has shown that both mesa etch and implant isolation can be used to define the active device area. Recently, an all implanted GaN junction FET, a Si_3N_4 gated GaN MISFET, and a $Ga_2O_3(Gd_2O_4)$ gated GaN MOSFET with reasonable performance were also reported. These types of devices potentially have advantage over MESFET, especially at high temperatures due to low reverse leakage currents.

So far, there are only few reports of development of GaN based bipolar transistors [74, 75]. Basically the device performance is limited by the difficulty in growth and

processing related to the buried p-type layer and the small minority carrier lifetime. It is still far from commercialization of these devices, but their developments will follow the material improvements in the new decade, and much impetus comes from defense applications where ultrawide bandwidth and linearity are desired.

Group III-V nitrides offer a valuable combination of electrical, optical and pizeoelectrical behavior, and enable the fabrication of LEDs, LDs, detectors, and transistors. In the past, the poor quality of the materials, the lack of p-type doping, and the absence of reliable processing procedures thwarted engineers and scientists from fabricating these useful devices. However, the 1990s have brought significant advances in the sophistication of growth techniques, the purity of the chemicals used for film deposition, the controlled introduction and activation of selected impurities, and progress in processing techniques. Most of the aforementioned obstacles have been sufficiently overcome, and the electronic and optical devices have been demonstrated and partially commercialized. In transistors, GaN can go where no other semiconductors have gone before. The future development in this area will definitely be fueled by the increasing demand for high temperature, high power applications. From materials science to device engineering, from laboratory research to commercial products, III-V nitride technologies have shown a late but exciting development.

While further improvements in the III-V nitride materials quality can be expected to enhance device operation, further device advances will also require improved processing technology. Owing to their wide bandgap nature and chemical stability, GaN and related materials present a host of device processing challenges, including poor p-type doping (by implantation), difficulty in achieving reliable low-resistance p-Ohmic contacts, high temperatures needed for implant activation, lack of efficient wet etch process, generally low dry etch rates and low selectivity over etching masks, and dry etch damage. These problems constitute a major obstacle to successful demonstration and commercialization of some GaN-based devices, such as bipolar transistors and power switches, whose performance are much more affected by the immature fabrication techniques. To fully exploit these device applications, a number of critical advances are necessary in the areas of implantation doping and isolation, high temperature thermal

processing, Ohmic contact to p-type material, dry etching process, and device passivation.

Considerable progress in the development of contacts to GaN has been made in the past several years. Nevertheless, it is necessary still to improve upon the electrical performance of these contacts, particularly to achieve low contact resistances to p-GaN, and to develop contacts with greater thermal stability, which is critical for high current density devices. It has proven challenging to obtain acceptable low specific contact resistances on p-GaN. Values $\leq 10^{-5}\Omega\text{cm}^2$ would be desirable in general, for electronics, but more typical numbers are$10^{-1} - 10^{-3}\Omega\text{cm}^2$. The high contact resistances can be attributed to several factors, including: (1) the absence of a metal with a sufficiently high work function (the bandgap of GaN is 3.4 eV, and the electron affinity is 4.1 eV, but metal work functions are typically ≤5 eV; (2) the relatively low hole concentrations in p-GaN due to the deep ionization level of the Mg acceptor (~170 meV); (3) the tendency for the preferential loss of nitrogen from the GaN surface during processing, which may produce surface conversion to n-type conductivity. In order to further lower the contact resistances to p-GaN, it will be necessary to further increase p-type conductivity or to lower the barrier height of the metal contacts, perhaps by growing a more readily contacted compositionally graded semiconductor alloy on the p-GaN. The thermal stability of the contacts is also noteworthy. Annealing at ~700^0 C resulted in interfacial reaction along with serious morphological degradation of the conventional Ti-based or Ni-based contacts. In the case of contact to p-GaN, the metallization will heat up as current flows across the interface due to the high series resistance, leading to metal migration down threading dislocations and eventual shorting of the devices. Thermally stable Schottky contacts are also required for power amplifiers and optoelectronics that operate at high temperatures, but the electrical characteristics of the metal/n-GaN diodes have been reported to suffer degradation upon exposure to temperatures as low as 300°C (Pd) , 400°C (Pt), 575°C (Au) and 600°C (Ni). Furthermore, there is a large scatter in the measured results of Schottky barrier height (SBH) and the Ohmic contact resistance, suggesting that our understanding of the interface reactions, surface preparation, and non-idealities associated with the metal/GaN contacts is far from complete.

GaN-based amplifiers and switches are attractive for high power applications in hostile environments. Reliable edge termination and passivation processes are critical to fully exploit these types of devices. There is not much work to date in this area. In addition, as discussed earlier, thermally stable doping, isolation, and metal contacts are all key issues for these special applications [76].

CHAPTER-3
PHYSICS OF MESFET

3.1 About MESFET

MESFET stands for Metal Oxide semiconductor Field Effect Transistor and it is similar to a JFET in terms of construction and terminology. In the MESFET a Schottky junction is used instead of p-n junction gate. It consists of a conducting channel positioned between a source and drain contact region as shown in the Fig.3.1, the carrier flow from source to drain is controlled by a schottky metal gate. By varying the depletion layer width underneath the metal contact the control of channel is obtained which modulates the thickness of the conducting channel and thereby the current. The MESFET in a majority carrier device and the key advantage of the MESFET is the higher mobility of the carriers scattering effect in the channel as compared to the MOSFET.

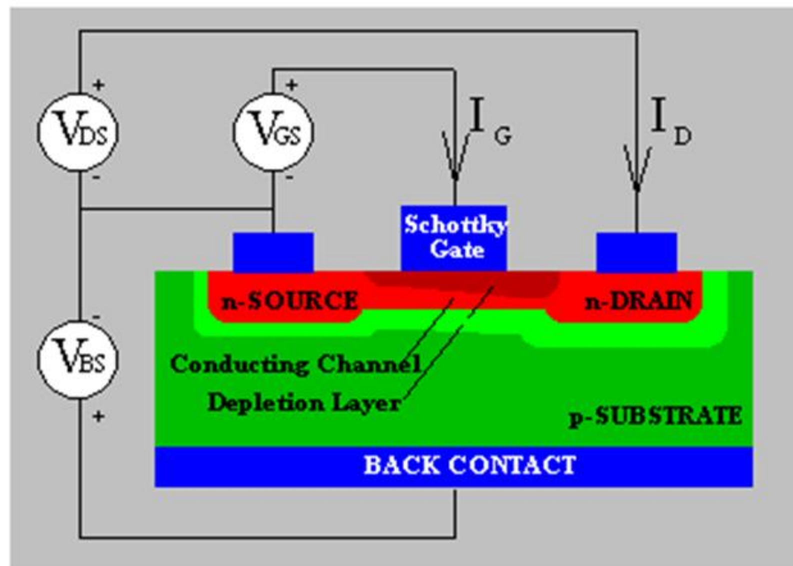

Fig. 3.1: Cross sectional view of a MESFET

In the MOSFET the carriers are located in the inversion layer, the MOSFET have a work function which extends into the oxide, surface mobility. The surface mobility is less than half of mobility of bulk material, when the depletion layer separates the carriers from the surface their mobility is close to that of bulk material.

3.2. Fabrication of MESFET

3.2.1. For High Current Operation

Recently, GaN electronic devices have been actively developed in the USA. Also in the USA, several venture companies selling and manufacturing GaN electronic devices have recently been established. Furthermore, Air Force and Naval Research have also been actively researching military applications. Other uses of GaN electronic devices are electric power switching devices such as inverters, converters, relay switching devices, and high -frequency devices [77].

First, the structurally simple MESFET for large current operation is fabricated. Fig. 3.2 is a schematic drawing of a GaN MESFET. A 50nm- thick GaN buffer layer was formed on the substrate using ammonia (NH_3) as the nitrogen source and a trymethylgallium (TMG) at a low temperature, such as 873^0 K. An undoped 2000 nm-thick GaN layer with high resistivity was grown on a GaN buffer layer at 1323 K to obtain a high-quality GaN active layer with a thickness of 200 nm. The GaN active layer with a carrier concentration of 2.0×10^{17} cm^{-3} and a mobility of 300 cm^2/Vsec at room temperature were used to fabricate the MESFET. A 100 nm thick Si-doped layer forms the contact layer. The Si concentration of the contact layer is 2×10^{19} $cm^{-3}$for ohmic contact .The GaN was etched by a dry-etching technique using an electron cyclotron resonance (ECR) plasma to make the FET. The etching gas was a mixture of CH_4 (5 sccm), Ar (7 sccm), and H_2 (15 sccm). The microwave input power was 250 W and the DC bias voltage was 250 V.The etching rate of Si-doped and undoped GaN layers was 14 nm/min. The etching depth of GaN was about 400 nm for isolation. Furthermore, the contact layer was etched to provide the recessed gate structure. The interval of the recessed structure was 20000 nm and the etched depth was 150 nm. After patterning using a photoresist combined with a SiO_2 mask, we formed a source and a drain using Al/Ti/Au, and a Schottky gate as Pt/Au on patterned GaN samples using the ECR sputter evaporation method. The distance between the source and the drain was 30000 nm. The gate length of the GaN MESFET was 2000 nm. The source, drain, and gate electrodes of 40 unit FETs were connected using Al/Au, to obtain high-current operation. SiO_2 was used to isolate source, drain, and gate electrodes [77].

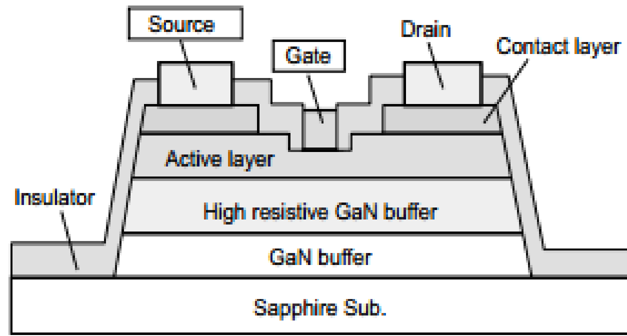

Fig. 3.2: Schematic drawing of a GaN MESFET

Fig. 3.3 shows the relation between the contact resistivity of ohmic electrode materials (Al/Ti/Au) and the Si concentration of the GaN contact layer. We obtained the ohmic contacts without thermal annealing. The contact resistivity was 1×10^{-6} Ω cm^2 at a Si concentration of $2\times10^{19}cm^{-3}$. It was thus confirmed that the contact resistivity decreased as Si concentration increased [77].

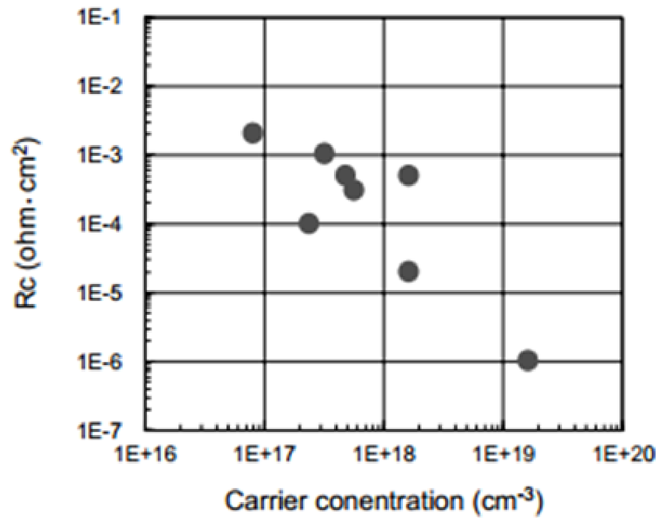

Fig. 3.3: Ohmic contact resistivity versus carrier concentration of the GaN contact layer

Fig. 3.4 shows the Schottky property between the gate and the source. The breakdown voltage was over 500 V and the maximum breakdown voltage was approximately 600 V.

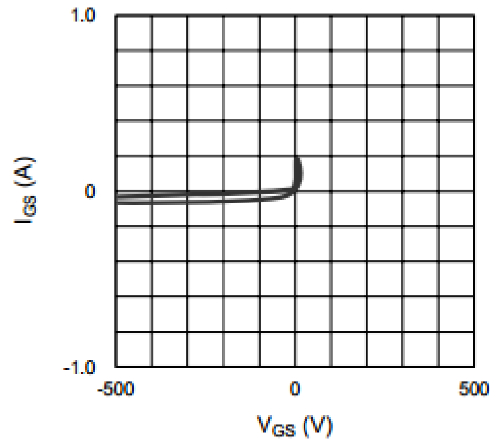

Fig. 3.4: Schottky property between the gate and source electrodes

The drain-source current (I_{ds}) as a function of the drain-source voltage (V_{ds}), and a FET was also obtained without cooling, as shown in Fig. 3.5. The gate voltage (V_{gs}) was changed from 0 V to -7 V in steps of -1 V. It was found that this FET can be operated above 5 A. The on-state resistance was about 2.7 Ω. The transconductance (g_m) was about 12 mS/mm. The pinch-off voltage was about -8 V [77].

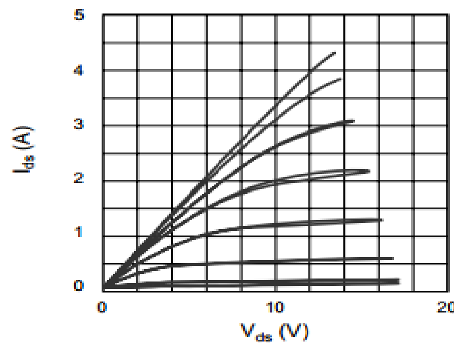

Fig. 3.5: Current –voltage characteristics ($I_{ds} - V_{ds}$) of a GaN MESFET with a gate width of 8 cm

The gate voltages were changed from 0V to 8V in steps of -1V. The sheet resistivity of a highly resistive undoped GaN layer was about 1×10^{-6} Ω/cm^2.To investigate whether or not electrode materials diffused into the GaN layer at 673 K, the interface of the GaN MESFET using secondary ion mass spectrometry (SIMS). We also observed, using a transmission electron microscope (TEM), that the interface of the

electrode materials and the GaN layer was not deformed. No degradation of the interfaces of Ti, Al, Au, and GaN layers was observed. The interfaces of the Pt, Au, and GaN layers were not deformed. Furthermore, it was confirmed that the isolating reaction of Sio_2 and electrode metal, such as Al, Ti, and Au, was not observed. Based on these results, it was confirmed that a GaN MESFET with the above-mentioned structure is effective for high-current devices. Furthermore, we fabricated a GaN MESFET with a gate width of 20 cm and a gate length of 2000 nm. The distance between source and drain was reduced to 15000 nm. This FET can be operated at above 10 A by cooling it with a fan. Also, the breakdown voltage of the gate and the source was over 500 V. Based on the above-mentioned results, it was confirmed that the GaN MESFET can be operated under conditions of high current and high breakdown voltage [77].

GaN-MESFET is grown on sapphire substrates using Molecular Beam epitaxy (MBE), the cross sectional sections of these structures are shown in Fig.3.6. All structures had a buffer layer consisting of a 20 nm AlN layer on a sapphire substrate, followed by a 3μm unintentionally doped GaN layer. The active layers were grown on the 3μm-thick GaN layer. The MESFET consisted of 100 nm thick, 1×10^{17} cm^{-3} Si-doped channel thinned from an originally 2μm and without a n^{++} capping layer. All FETs were fabricated with a source –drain spacing of 6μm. the gate length was 2μm and the width varied from 100μm to 200μm [78].

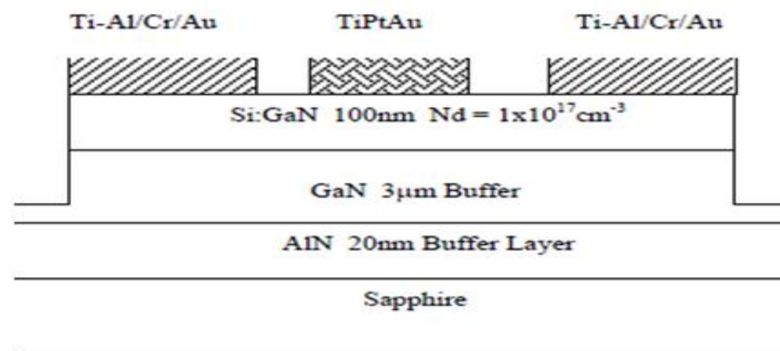

Fig.3.6: GaN-MESFET cross-section of Si-doped MESFET

The wafer was first covered with a 200nm-thick, sputtered, Ti layer as the mask prior to the photolithography. Processing steps were similar to that have been described for GaAs-based devices. The major difference in processing between the GaN-based

devices and GaAs-based devices is that the wet etching was ruled out in the former case. The trench etching for device isolation was carried out by reactive ion etching (RIE) using CI plasma. The final depth of the mesa is close to 2μm.The Ti mask is then removed in HF solution and contact windows were exposed. The wafer received plasma etching for 30sec in CF_4 and Ar plasma. Then, The Ti-Al ohmic contacts were deposited using e-beam evaporation for MESFET, TiPtAu gate contacts were deposited by sputtering. The annealing condition was optimized at 600^0 C for 5 min in forming gas ambient [78].

3.2.2. Fabrication Steps in MESFET's

The GaN MESFET fabrication process is summarized in Fig. 3.7 and incorporates two silicon ion implantations, one to form the n-channel region and a second to heavily doped n+ the source and drain regions in order to form low resistance contacts. For the fabrication process, a gold-germanium-nickel metallization is used to form the ohmic contacts for the source and drain regions and aluminum is deposited to form the Schottky gate and for thicker metal pads suitable for probing. E-beam evaporation is used for metal deposition and a metal liftoff process is used to define the metal layers. The processes used in device fabrication are photolithography, resist processing, dielectric deposition and etching, ion implantation, annealing, metal deposition, patterning and alloying. The fabrication process steps are: For the fabrication process, a gold-germanium-nickel metallization is used to form the ohmic contacts for the source and drain regions and aluminum is deposited to form the Schottky gate and for thicker metal pads suitable for probing. E-beam evaporation is used for metal deposition and a metal liftoff process is used to define the metal layers. The processes used in device fabrication are photolithography, resist processing, dielectric deposition and etching, ion implantation, annealing, metal deposition, patterning and alloying.

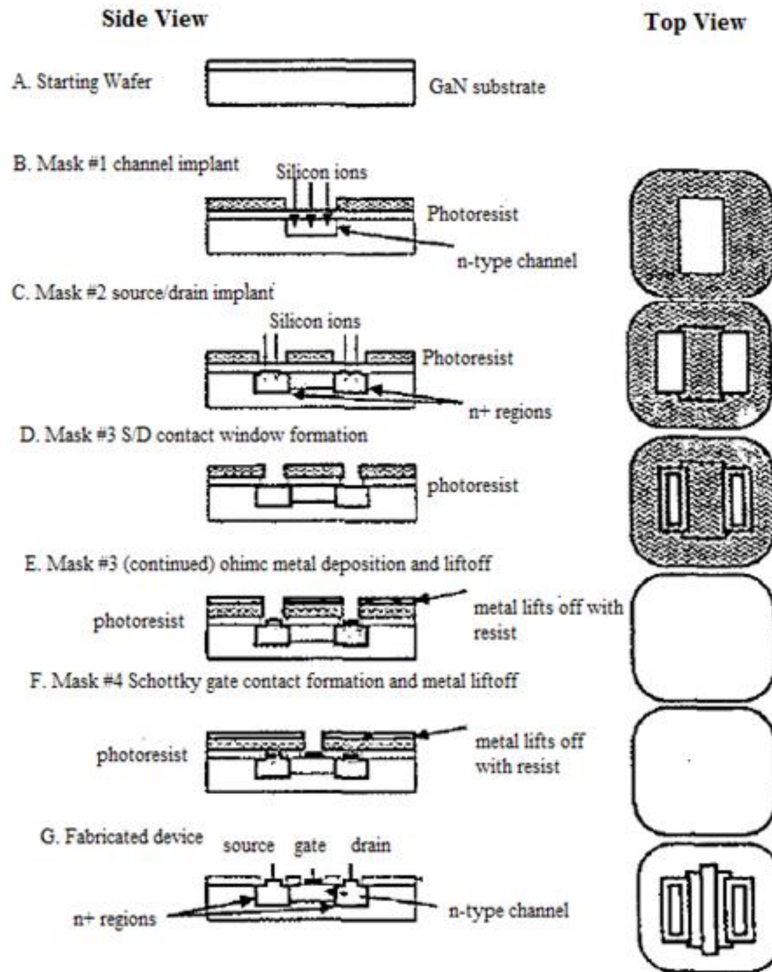

Fig. 3.7 Fabrication process of GaN MESFET

The fabrication process steps are:

- Initial wafer cleaning.
- Silicon nitride cap deposition by reactive sputtering.
- Resist patterning for channel implant using positive resist
- Silicon ion implantation of device channel regions
- Shallow etching of silicon nitride for alignment registration purposes in buffered HF solution and plasma etching.
- Resist stripping and ashing in oxygen plasma.
- Resist patterning for source/drain implant using positive resist.
- Silicon ion implantation of device source and drain regions.
- Resist stripping and ashing in oxygen plasma.

- Annealing of ion implants using rapid thermal annealing
- Resist patterning for ohmic contact formations
- Silicon nitride etching for ohmic contacts
- Deposition of AuGe/Ni metal for ohmic contacts to source and drain using e-beam evaporation and patterning by liftoff technique.
- Ohmic contact alloying by rapid thermal heating.
- Resist patterning for nitride etch for Schottky gate formation
- Silicon nitride etching for Schottky gate formation.
- Aluminum metal deposition for Schottky gate formation using e-beam lift off technique [78].

3.3 Operational Properties of GaN MESFET

The cross sectional structure of simulated wurtzite GaN MESFET. The substrate is the n-GaN with a background doping density of 3×10^{17} cm^{-3} and 0.1μm thick. The doping concentration of both source and drain is $2\times10^{19}cm^{-3}$.

The gold (Au) is assumed for the gate material with 0.1μm length, and the separation between source and drain is 0.4μm shown in the Fig. 3.8. The small dimensions of the device are chosen mainly to manage the computational demands of the Monte Carlo simulator [79].

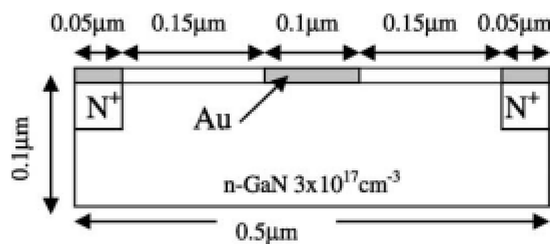

Fig. 3.8: The cross sectional structure of simulated GaN MESFET

The Fig. 3.9 shows the drain current (I_{DS}) the drain–source voltage V_{Ds} characteristics are obtained based on Monte Carlo simulations in the range of gate–source voltages from -6 to 0 V in 1 V step. At V_{DS} = 15 V and V_{GS} = 0 V; I_{DS} is equal to 5.03 A/cm, which is higher value [79].

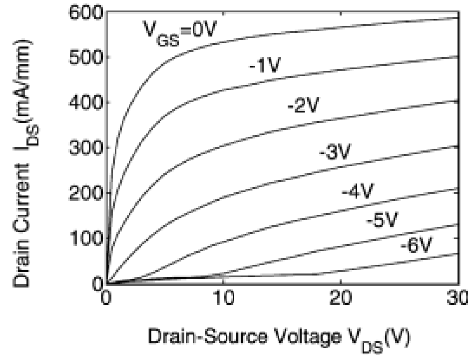

Fig. 3.9: GaN MESFET output characteristics

The characteristics of the transconductance G_m versus V_{GS} are also analyzed by Monte Carlo simulations. Fig. 3.10 shows transconductance as a function of gate–source voltage at V_{DS} = 15 V.

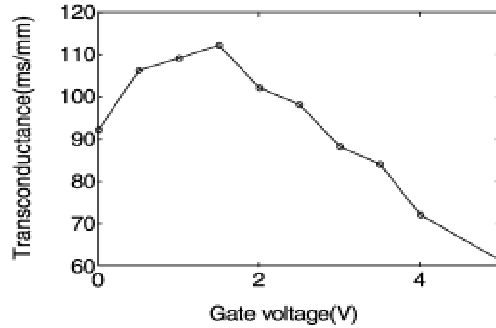

Fig. 3.10: Transconductance as a function of gate voltage at V_{DS}=15V

The $G_m - V_{Ds}$ curve exhibits bell shaped and the maximum G_m of 112 ms/mm at V_{DS} = 15V and V_{GS} =1.5V. The current gain cutoff frequency f_T is calculated from the following expression [79].

$$f_T = \frac{G_m}{2\pi C_g} \tag{1}$$

Where G_m the transconductance and C_g is the gate capacitance. Both G_m and C_g are a functions of V_{GS}. C_g versus V_{GS} curve was obtained by differentiating Q_g versus V_{gs} curve with respect to V_{GS}. The Fig. 3.11 shows the dependence of the current cutoff frequency f_T on the gate voltage at V_{DS} = 15 V; which got from Equation (1).

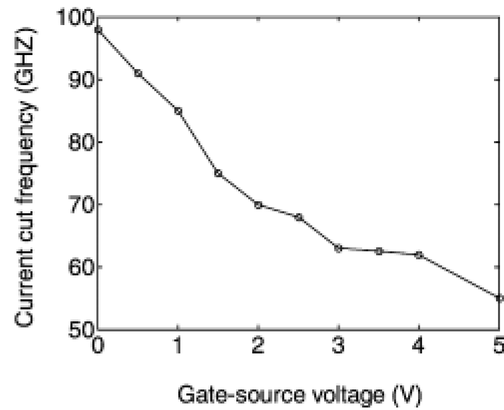

Fig. 3.11: Current cut frequency as a function of gate voltage at V_{DS}= 15V

The maximum value is about 98 GHz at V_{GS} = 0 V and I_{DS} = 1150 mA/mm. The high I_{DS} value and the high f_T value strongly suggest that wurtzite phase MESFETs have high potential as a high frequency and high-power device [79].

3.4 Substrate for GaN MESFET

Recently, there has been considerable interest in the growth of GaN and related alloys on Si substrates for the fabrication of light emitting diodes , photodetectors and high electron mobility AlGaN/GaN heterostructure because Si substrates have the advantages of low cost and large size. In addition to their low cost and large size, Si substrates have a thermal conductivity of 1.5W/ cm-K compared with the thermal conductivity of 0.35 W/cm-K for sapphire and 4.9W/cm-K for 6H-Sic [80]. Previous studies have shown that GaN-based materials on Si are of lesser quality than such materials grown on sapphire and on SiC, mainly due to the large lattice and thermal mismatches between GaN and Si .Taking account of its advantages, such as its use as a substrate for the heteroepitaxial growth of GaN-based materials, however, Si is expected to be an excellent candidate for high-power GaN-based devices. This deals with the characterization of GaN MESFETs on (111) - oriented Si substrates grown by metal organic chemical vapor deposition (MOCVD) using $Al_{0.27}$ $G_{0.73}$ N/AlN intermediate layers. Among the best technologies, this is the first demonstration of advantages of a GaN MESFET on Si [81].

The growth of GaN MESFETs on Sb-doped, 0.015**Ω**-cm resistivity n-type Si (111) substrates was carried out in a Nippon Sanso MOCVD system (SR-2000). The reactant species used were trimethylgallium (TMG), trimethylaluminum (TMA), and ammonia (NH_3) with H_2 as the carrier gas. Monosilane (SiH_4) diluted in H_2 (l0ppm) was used as the n-type dopant. The substrates were prepared by degreasing in solvents, followed by a 5min etch in H_2O_2: H_2 SO_2 (1:4) and an l min etch in HF: DIH_2O (1:10). A 80nm thick i-AlN nucleation layer was grown at 1100^0 C, followed by a 0.25μm thick i-$Al_{0.27}$ $G_{0.73}$ N layer at 1080°C, a 0.8μm-thick i-GaN layer at 1080^0 C and a 0.2μm thick n-GaN layer with Si doped to 2 x 10^{17} cm^{-3} at 1080°C. For the growth of i-AlN layer, the flow rates of the NH_3 and TMA were 51/min and 6.1μmol/min, respectively. The flow rates of the TMG and TMA were 13.9μmol/min and 6.lμmol/min, respectively, for the growth of the I- $Al_{0.27}$ $G_{0.73}$ N layer. For the growth of the GaN layers, the flow rates of the NH_3 and TMG were 5l/min and 20.8μmol/min, respectively. We have shown that the $Al_{0.27}$ $G_{0.73}$ N/AlN intermediate layers play an important role in obtaining a mirror-like surface morphology [82]. The GaN layer on Si exhibits a tension during cooling from the growth temperature to room temperature. The thickness of a GaN MESFET on Si is thinner than that of a MESFET on sapphire. This results from the suppression of crack formation in the epitaxial layer grown on Si. In this study the total grown layer thickness was designed to be 1.5μm in order to avoid the formation of cracks and to obtain a mirror-like surface morphology. The device isolation was accomplished by mesa dry etching down to the i-GaN layer by reactive ion etching (RIE) in a BCl_3, plasma at an RF power of 10W and a chamber pressure of 3Pa. Using a standard lift-off technique, the ohmic contacts to the drain and source regions were formed by the deposition of a Ti/Al (25/150nm) bi-layer, which was subsequently alloyed at 600^0 C for 60s. The specific contact resistance of the source-drain ohmic was measured to be 3 x10^{-3} **Ω**-cm^2 using a transmission line model measurement. The Schottky gate metallization consisted of a Pt/ Ti/Au (10/40/100nm) multilayer. The devices had a gate length L_g of 2.5μm, a gate width W_g of 15μm, and the source-to-drain distance of 10μm [83].

Double crystal X-ray diffraction (DCXD) and photoluminescence (PL) and van-der Pauw Hall measurements were performed on the 0.8μm thick GaN layers on Si and sapphire. Secondary-ion mass spectroscopy (SIMS) measurements were also performed

with Cs^+ primary ion bombardment. The detection limit of Si in the GaN layer was 5 x 10^{15}atoms/cm^3. The GaN layer grown on Si exhibited a mirror-like surface morphology and the large crack-free areas using the $Al_{0.27}$ $G_{0.73}$ N/AlN intermediate layers. The full-width at half maximum (FWHM) of the (0004) GaN diffraction peak of the 0.8μm thick n-GaN layer on Si was 600arcsec, which is larger than the typical value of 387arcsec measured on 0.8μm thick n-GaN on sapphire. The FWHMs near the band-edge line width at 300K were 86.8meV for the GaN layer on Si and 65.3meV for the GaN layer on sapphire. The near band-edge emissions were observed at 3.39 and 3.43eV for the n-GaN layers on Si and sapphire, respectively. The peak shift is due to the lattice deformation caused by the difference in the thermal expansion coefficients between GaN and Si. However, the single peak from the near band-edge emission indicates the uniform stress in the GaN layer on Si. Deep level emission (yellow luminescence) was observed around at 550nm**,** which was similar to that of the GaN layer on sapphire. The Hall mobilities were 150 200cm^2 /Vs and 200-250cm^2 /Vs for the n-GaN layers with an electron carrier concentration of 3 x 10^{17} cm^{-3} grown on Si and sapphire, respectively [83].

The drain-source current against drain-source voltage (I_{DS} -V_{DS}) characteristic of the GaN MESFET on Si is shown in Fig. 3.12 The gate-source bias V_{GS} is from +1.5 to -10.5V.

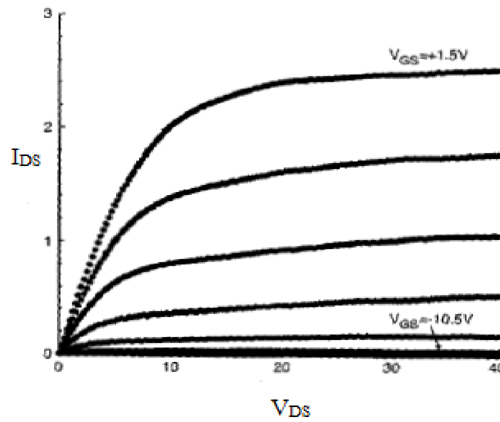

Fig. 3.12: I_{DS}– V_{DS} characteristic at different V_{GS} for GaN MESFET grown on Si

The extrinsic transconductance g_m and the drain-source current I_{DS} were measured to be 25mS/mm and 169mA/mm, respectively, for the device with L_g /W_g = 2.5/1.5μm. The variation of extrinsic transconductance g_m and the drain source I_{DS} as a function of

the applied gate bias V_{GS} is shown in Fig. 3.13 .The maximum extrinsic transconductance g_{mmax} was measured to be 25mS/mm at V_{GS} = 0.4V and V_{DS}, = 14V**.** The g_m–V_{GS} characteristic exhibits a well-behaved feature, which indicates that the condition does not exist beneath the channel layer. Complete pinch off was observed for the GaN MESFET on Si because the isolation leakage current at 20V was as low as 60-100nA for the 5µm gap.

We have reported that the GaAs MESFET on Si showed a poor pinch-off characteristic due to the conduction beneath the channel layer. However, the GaN MESFET with complete pinch-off can be fabricated on Si. The complete pinch-off characteristic is attributed to the high-resistivity of the undoped GaN, $Al_{0.27}$ $G_{0.73}$ N and AlN layers beneath the n-GaN channel layer. Fig. 3.14 shows SIMS profiles of the GaN MESFET on the $Al_{0.27}$ $G_{0.73}$ N/AlN/Si. The increase in Si concentration has been reported at the AIN/Si interface due to either auto doping of Si from the Si substrate or the pipe diffusion from the defective AIN/Si interface, which was similar to the growth of GaAs/Si. As shown in Fig.3.14**,** however, a pile-up or increase in the Si concentration was not observed in the GaN MESFET on Si using the $Al_{0.27}$ $G_{0.73}$ N/AlN intermediate layers.

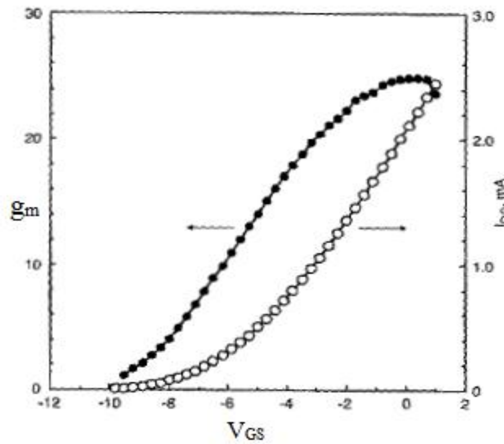

Fig. 3.13: $g_m$and I_{DS} against applied V_{GS} for GaN MESFET on Si

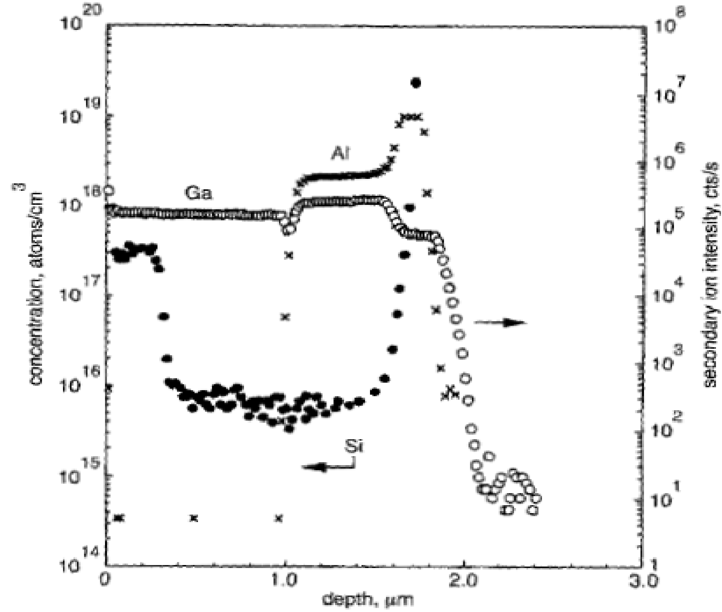

Fig. 3.14: SIMS profiles of GaN MESFET grown on Si using $Al_{0.27}$ $G_{0.73}$ N/AlN intermediate layers

The surface morphology and the Si concentration in the i- GaN layer depended on the growth conditions and the thickness of the $Al_{0.27}$ $G_{0.73}$ N/AlN intermediate layers on Si. Another important feature of the GaN MESFET on Si is that drain-source current reduction as a result of the self-heating effect is not observed. The drain-source current in the FETs grown on sapphire exhibited a much larger negative slope compared to that for the devices grown on Sic .The presence of the negative slope is related to the device self-heating because the thermal conductivity of sapphire is more than an order of magnitude smaller than that for SiC. The self-heating effect was observed at high voltages and high currents for the FETs grown on sapphire [83].

3.5 Microwave Performance of GaN MESFET'S

This interest stems primarily from the lower thermal generation rates and higher breakdowns fields inherent in wide-band gap materials. GaN also has the required properties for these applications and can be incorporated into heterojunction device structures [84]. The DC characteristics of GaN MESFETs with a 4um gate length have been recently reported, the device fabrication and microwave performance of 0.7um gate length GaN MESFETS where the active channel was grown on a highly resistive GaN layer.

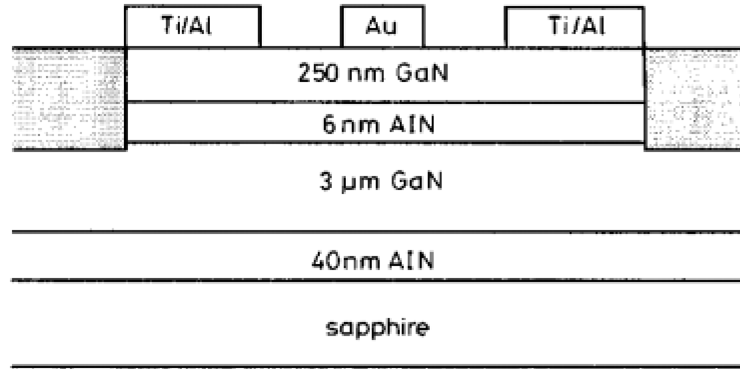

Fig. 3.15: Device cross section, the shaded area represents the proton implanted region

The GaN epitaxial layers used in this study were unintentionally doped and grown on basal plane sapphire substrates by metal organic vapour phase epitaxial. The Fig. 3.15 a 40nm thick AlN buffer layer was grown at substrate temperature of 450^0C, followed by a 3 m thick undoped highly resistive GaN layer grown at 1050^0 C. A thick AlN layer was then grown, followed by the growth of the 0.25μm thick channel. From Hall–effect measurements at 300k on samples patterned with a clover-leaf geometry and at a magnetic field of 0.2T, the electron mobility and carrier concentration of the active channel layer were measured to be 400 cm^2/(Vs) and $2.7 \times 10^{17} cm^{-3}$, respectively. C-V measurements indicated that most of the carriers in the active channel are located near the GaN/AlN interface. The mechanism responsible for this behavior is currently under investigation. MESFET'S were fabricated with a source-drain spacing of 5 μm and gate lengths of 0.7 to 0.2 μm. The total gate width is 150μm.The metallization patterns were designed to be compatible with on-wafer microwave probes. All metallisations are defined by photoresist lift-off. Ti/Al alloyed at 500^0C was used to form the source and drain ohmic contacts. The devices were isolated by using multiple-energy proton implantation designed to penetrate the 0.2μm channel thickness. The Schottky-barrier gate was formed with 300nm of Au [85].

The Fig. 3.16 below shows the DC drain characteristics for GaN MESFET with gate length of 1.4μm and width of 150um for a gate source diode reverse bias of 35V, the gate leakage current was 100μA and the maximum transconductance is 20mS/mm. The characteristics depend on the rate at which the I-V curves were measured. A 25% higher g_m was measured using a curve tracer that swept V_{DS} at 120Hz. This dependence

on measurement rate is indicative of trapping effects. The nearly constant g_m as a function of gate bias, as well as the fairly low g_m, is attributed to the fact that most of the carriers as near the upper GaN/AlN interface, as in a step-doped structure. The gate voltage was applied in -2V steps [85].

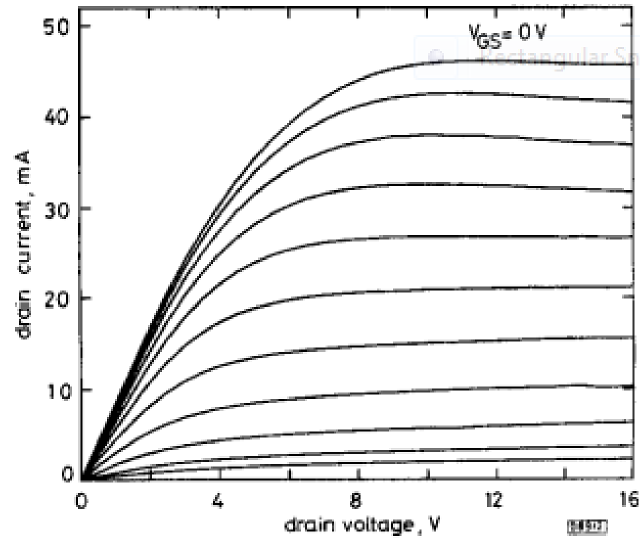

Fig. 3.16: Drain characteristics for GaN MESFET with gate length of 1.4μm and width of 150μm

As a function of frequency and bias on-wafer probing the S-parameters of these devices were measured. The Fig. 3.17 shows the short circuit current gain $|h_{21}|$ and mason unilateral gain U for device with gate length of 0.7μm and the values of f_{max} and f_T are 8 and 17 GHz.To maximize the gain values the bias point was chosen, the usual 6dB/octave curve fitting yields f_{max} and f_T values of 8 and 17GHz, respectively. The initial results on GaN are competitive with those obtained with SiC MESFET in terms of frequency performance [85].

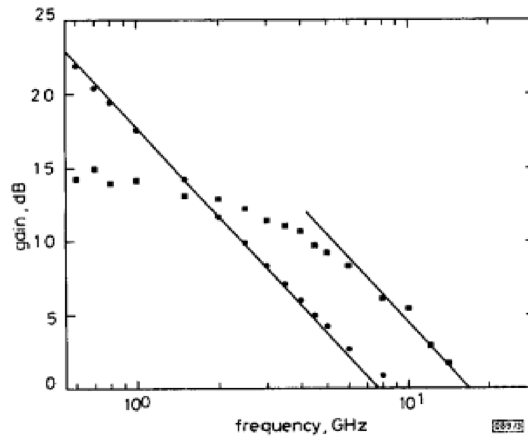

Fig. 3.17: Short circuit current gain $|h_{21}|$ and Mason unilateral gain U for devices with 0.7μm gate length

A small-signal equivalent circuit for these devices was developed by matching measured and calculated S-parameters and the topology is commonly used for FETs. An excellent match between calculated and measured results was achieved, indicating a well-behaved transistor. The GaN MESFET has small transconductance and large drain and source resistances. The drain and source resistances are made up in roughly equal parts by the contact and access resistances. With the higher carrier concentrations and improved contact technology, both of these values can be lowered. The Fig. 3.18 below shows the GaN MESFET equivalent circuit for device with 0.7μm gate length, V_{DS}=17V, V_{gs}=-12V, I_{DS} = 24MA, width= 150μm [85].

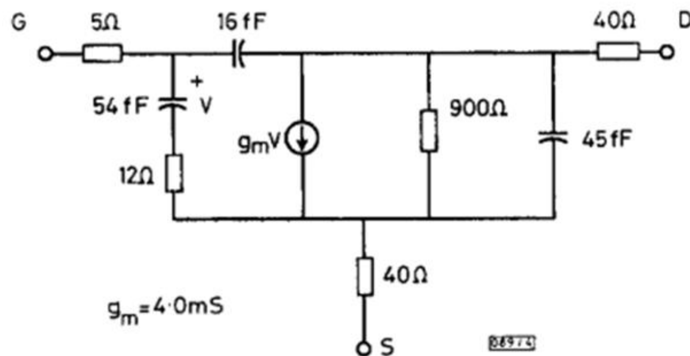

Fig. 3.18: GaN MESFET equivalent circuit for device with 0.7 gate length

The design and technology improvements has been improved the MESFET structure should perform with f_T in the 20 to 40 GHz range. These values would require a

shorter gate length and modified channel doping as well as some improvements in the contact technology [85].

3.6 Extraction of R_s, R_d and R_g by STATZ model

The Statz model is a popular nonlinear MESFET model that is available in most large-signal circuit simulation packages used by microwave engineers. The model can be divided into two shells an inner shell represents the intrinsic MESFET device, while the outer shell represents the device parasitic. The important step in parameter extraction strategy for the Statz is extracting the parasitic resistances separately before the other model parameters because it reduces the number of element values that require a final optimization. This enhances speed and accuracy of the extraction process.

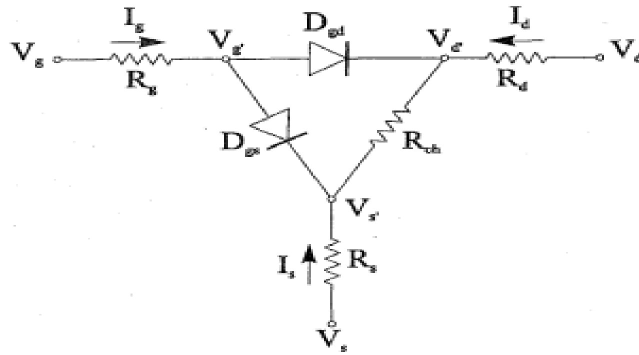

Fig.3.19: DC equivalent circuit model of Statz MESFET for ColdFET operation

The Fig. 3.19 shows a dc equivalent circuit model of a Statz MESFET for ColdFET operation ,this model is valid for only ColdFET operation of the MESFET, which means that the drain-source voltage is equal to zero or very small. The model consists of source, drain and gate, channel resistance using two different dc measurements, three unknown resistances R_s, R_d, R_g is generated. In a first measurements setup in Fig. 3.20, a current I_g is forced through the gate, while at the same time the drain is left open and the source is grounded. This current must be large enough to result in a substantial voltage drop across the gate and source resistance. The voltages at the gate and the drain terminal are measured simultaneously [86].

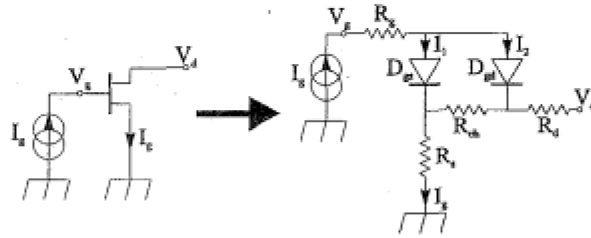

Fig. 3.20: First dc measurement setup and equivalent circuit

In second measurement setup is shown in Fig. 3.21, again a current is forced through the gate, but now a second current source sinks half of this current out of the drain. The source current is driven fully symmetrical, no current will flow through the channel resistance, or that the intrinsic drain-source voltage is forced to zero by the second current source [86].

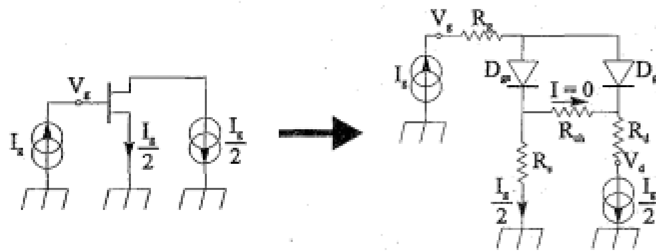

Fig. 3.21: Second dc measurement setup and equivalent circuit

The voltage at the drain is proportional to the difference between the source and the drain resistances. From the voltages measured at the drain and the gate, and Kirchhoff's voltage law, the following two additional relations between the unknown parasitic resistances are obtained. I_{sat} and η are two parameters that also have to be determined for use in the complete Statz MESFET model, with two parameters we have all the necessary information to solve three equations for three unknown parasitic resistances [86]. By using Shockley's, I_1 and I_2 through the two Schottky diodes is given by the following equation.

$$I_1 = I_{Sat} \cdot \left\{ \exp\left[\frac{V_g - \left(R_s + R_g\right) \cdot I_g}{\eta \, . V_t} \right] - 1 \right\} \tag{2}$$

$$I_2 = I_{sat} \cdot \left\{ \exp\left[\frac{V_g - R_g \cdot I_g - V_d}{\eta \,.\, V_t}\right] - 1 \right\}$$

(3)

$I_1 + I_2 = I_g$, (1) and (2) can be solved to obtain the following relation between $R_s + R_g$ is given as

$$R_s + R_g = \frac{V_g - \eta \cdot V_t \cdot \ln\left\{\left(2 + \frac{I_g}{I_{sat}}\right) \cdot \left[1 + \exp\left(\frac{R_s \cdot I_g - V_d}{\eta \,.\, V_t}\right)\right] \;\hat{}(-1)\right\}}{I_g}$$

(4)

$$R_d + \frac{2 \cdot V_d}{I_g} = R_s$$

(5)

$$R_g + \frac{R_s}{2} = \frac{V_g - \eta \,.\, V_t . \ln\left(1 + \frac{I_g}{I_{sat}}\right)}{I_g}$$

(6)

The diode parameters also have to be determined for use in the complete Statz MESFET model. This can be done using the same setup with I_{sat} and η to solve the three equations (4), (5) and (6) for the three unknown parasitic resistances. The solution is not straight forward. Normally care should be taken in calculating the parasitic resistances of small devices from direct dc I/V measurements, because junction heating at high current densities can affect the accuracy of the extracted resistance values. Still, this problem is inherent to any extraction method that is based on S–parameter or dc measurements of a device with strong forward bias [86].

MESFET operation in ohmic region or linear region is shown in the Fig.3.22, in this region V_{DS} is assumed small i.e. $|V_{GS}| > |V_{DS}|$ [87].

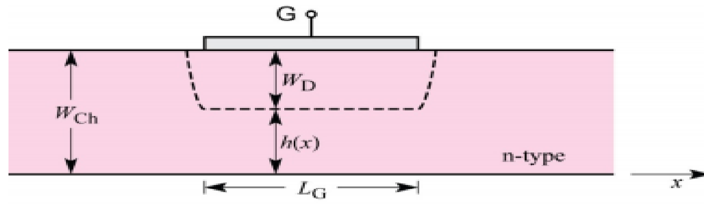

Fig.3.22: The MESFET operation in linear regime

The depletion layer thickness under the gate is given by,

$$W_D = \sqrt{\frac{2\,\epsilon}{e\,N_D}(-V_{GS})} \tag{7}$$

W_{ch} is a total channel height, in pinch off condition $W_D = W_{ch}$ and in pinch off voltage

$$V_{PO} = \frac{e\,N_D}{2\epsilon}\,W_{ch}^2 \tag{8}$$

Resistive of channel,

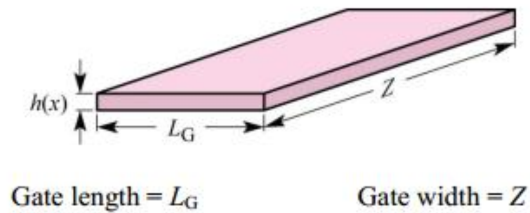

Fig. 3.23: The conductive channel

The resistance of Channel,

$$R = \rho\,\frac{L_G}{A} \tag{9}$$

At $V_{GS} = -V_{PO}$, R is ∞

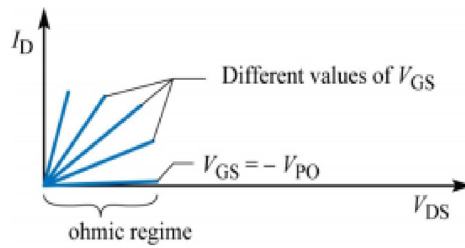

Fig. 3.24: The I-V characteristics of variable resistor controlled by the gate voltage

In the "linear regime", the FET behaves like a variable resistor controlled by the gate voltage.

$$I_D = -e\ n\ v\ h(x)\ Z \tag{10}$$

Whereas

$$h(x) = W_{ch} - W_D(x) \tag{11}$$

n = high concentration

Pinch off at drain end of the channel,

$$V_{PO} = V_{DS} - V_{GS} \tag{12}$$

At pinch off, $I_D = I_{D,sat}$ = saturation current this is independent of V_{DS} shown in Fig 3.25.

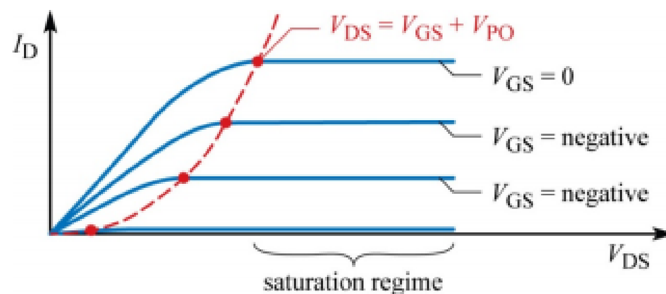

Fig.3.25: The output characteristics of FET in Saturation regime

The amplification of an FET is equal to Transconductance the dimensions of amplification is Ω^{-1} and dimensions of conductance is Siemens. The source resistance is

detrimental because it reduces the transconductance of the FET. The transconductance of FET is given as [87].

$$g_m = \left(\frac{1}{g_m} + R_S\right)^{-1} \tag{13}$$

CHAPTER-4

NUMERICAL CALUCATIONS

The parasitic resistance occurs when the three terminals such as source, drain and gate of MESFET are closer to each other. The present technology of short channel FET required the intensive study on parasitic parameters. These resistances can be calculated analytically from three equations, by assuming the $I_g = I_{g1} + I_{g2}$, the solutions for R_s, R_g, R_d are associated with contacts on devices.

Source resistance: Parasitic resistance at source is given by,

$$R_s = \frac{2\eta V_t}{I_g} \ln\left(0.5\, w_3 - 0.5\sqrt{w_3^2 - 4w_3}\right) + \frac{\eta\, V_t}{I_g} w_2 \tag{14}$$

Where w_2 and w_3 are,

$$w_2 = \frac{2}{\eta\, V_t}\left(V_{g2} - V_{g1}\right) + 2\ln 0.5 \tag{15}$$

$$w_3 = \exp\left(\frac{V_{d2}}{\eta\, V_t}\right) - w_2 \tag{16}$$

The function $w_3^2 - 4w_2$ in the square root has to equal to or larger than zero.

Drain resistance: Parasitic resistance at drain is given by,

$$R_d = R_s - \frac{2V_{d1}}{I_{g1}} \tag{17}$$

Gate resistance: Parasitic resistance at gate is given by,

$$R_g = \frac{V_{g1} - \eta V_t \ln\left(1 + \frac{I_{g1}}{2I_s}\right)}{I_{g1}} - \frac{R_s}{2} \tag{18}$$

CHAPTER-5

RESULT AND DISCUSSIONS

The analytical model has been developed based on the device physics. This model is developed to evaluate the characteristics of parasitic resistance such as drain, gate, and source under different voltage condition at standard saturation current, ideality factor, thermal voltage. Extraction of parasitic resistance is most important factor because it degrades the performance of both digital and analog microwave FET's.

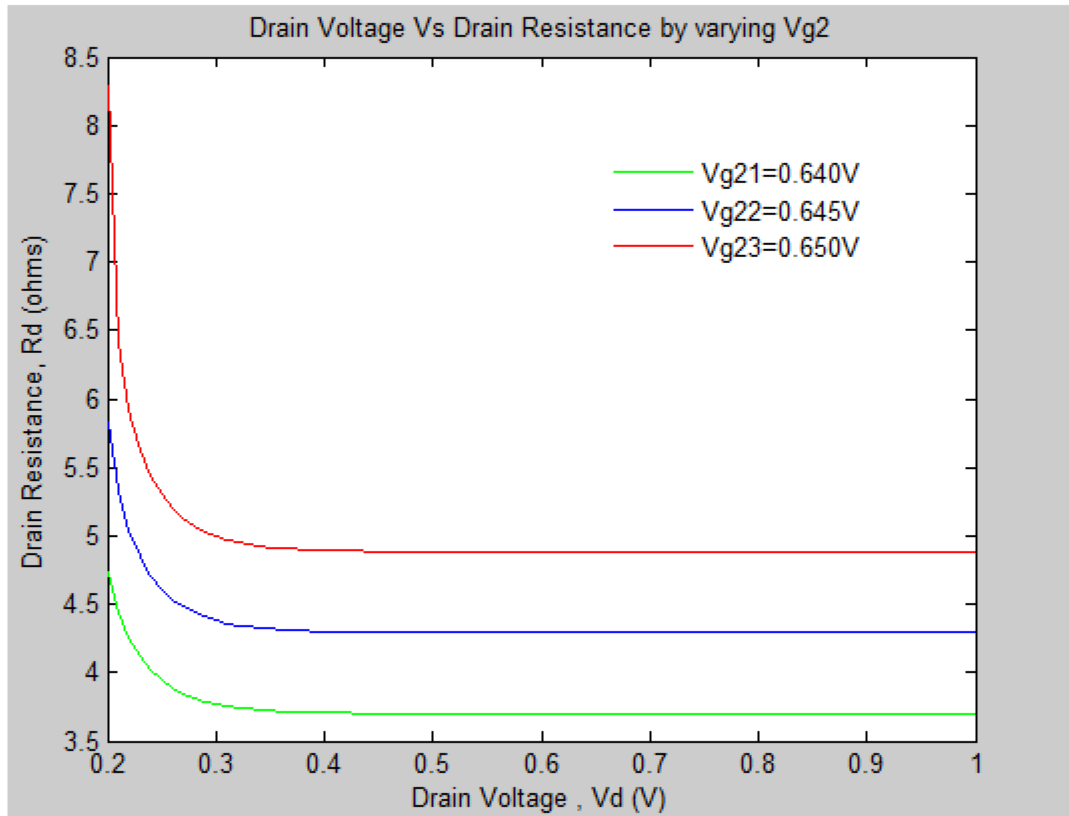

Fig.5.1: Plot of Drain Voltage $V_{d2}(V_d)$ vs Drain Resistance R_d varying Gate Voltage V_{g2}

The Fig. 5.1 shows a plot of drain voltage V_{d2} versus drain resistance R_d for different gate voltage V_{g2} of 0.640V, 0.645V, 0.650V and this plot had been drawn by using the equation (17). The drain resistance exponentially decreases between the drain voltages from 0.2V to 0.4V, whereas the drain resistance becomes saturated beyond 0.4V

to 1V. I-V plot shows a clear evident of changes of transconductance, the device can behave the linearity and non- linearity due to drain bias change.

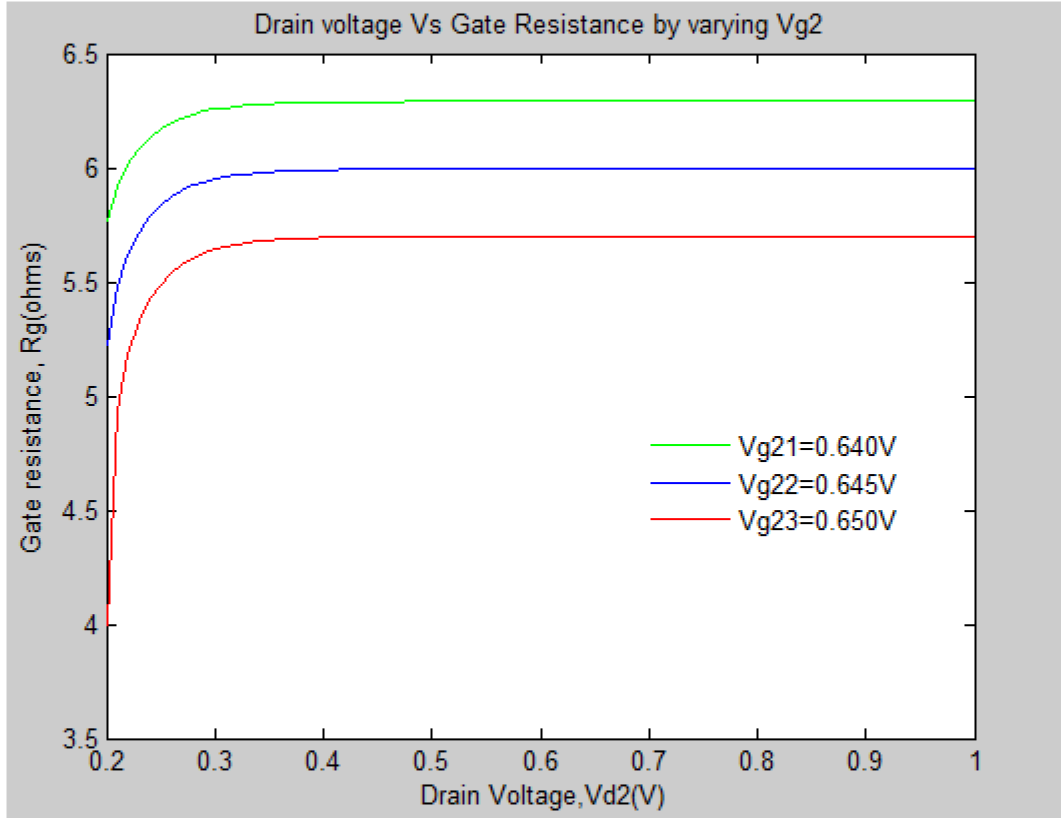

Fig. 5.2: Plot of Drain Voltage V_{d2} Versus Gate resistance R_g varying gate voltage V_{g2}

The Fig. 5.2 presents a plot of drain voltage V_{d2} versus gate resistance R_g for different gate voltage of 0.640V, 0.645V and 0.650V and the plot has been obtained by using the equation (18). The gate resistance R_g exponentially increases at the drain voltage of 0.2 -0.3V for gate voltages of 0.640V, 0.645V and 0.650V and the gate resistance value reaches to steady state constant value from 0.35V to 1.0V for same gate voltages. The gate resistances increase from the drain voltage from 0.2V to 0.3V, because of the excess carrier generation. The gate resistances become saturation, when the excess carriers reach to steady state value. This nature of the I-V plot shows clear indication of linearity and non-linearity properties of MESFET devices.

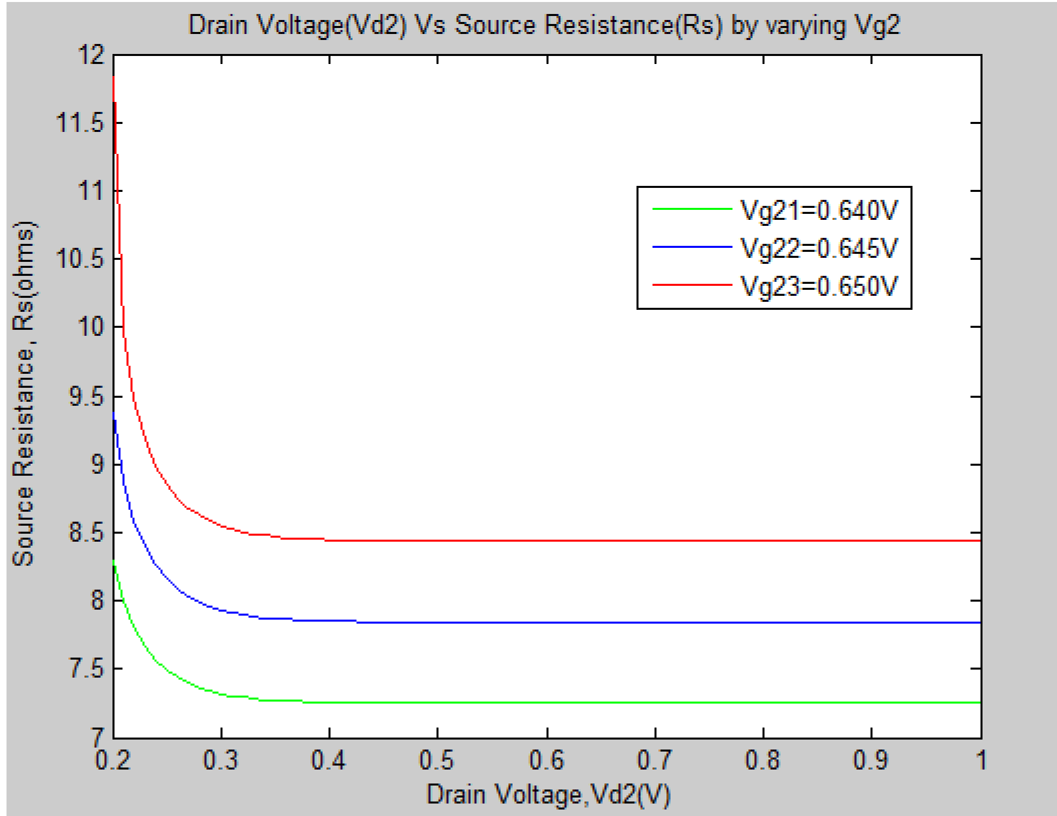

Fig. 5.3 Plot of Drain Voltage V_{d2} Versus Source resistance R_S varying gate voltage V_{g2}

The Fig. 5.3 shows a plot of drain voltage V_{d2} versus source resistance R_s for different gate Voltage V_{g2} of 0.640V, 0.645V and 0.650V and this plot has been drawn by using the equation (14). The source resistance exponentially decreases between the drain voltages from 0.2 to 0.3V, whereas the source resistance becomes saturated beyond 0.4V to 1V for different gate voltage. The knee source resistance between the drain voltage of 0.2V and 0.3V is a clear evident of change of transconductance, the device can behave the linearity and non-linearity due to drain biasing change. This study shows a significant effect on extrinsic parameter, which is due to the physical geometry of MESFET device. This extrinsic parameter clearly indicates their effect on linearity and non-linearity behavior of the devices and this will be helpful for optimization of device fabrication and physical parameters.

CHAPTER-6

CONCLUSION

The study of analytical determination of parasitic resistances is presented here to understand the characteristics of parasitic resistances and conductance. The extraction of parasitic resistances can be calculated analytically by using Matlab software is presented and this makes the calculations more simple and reliable. Therefore newton's iteration method is not required. For different voltage values variation, parasitic resistance of drain and source are exponentially decreases and gate resistance are exponentially increased has been studied and it is clear evident of change of transconductance, the device can behave the linearity and non-linearity due to the drain bias drain .This model is good alternative to other parasitic resistance extraction methods. Finally, this method is very sensitive to the measurement of noise. The extrinsic parameter study is important to understand the physical dimension design of active areas in MESFET and their interference in the contribution to high frequency performance.

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APPENDIX-A

η = Ideality factor

I_{sat}= Saturation Current

I_g= gate currents (I_{g1}, I_{g2})

R_s = Source resistance

R_d = Drain resistance

R_g = Gate resistance

V_t = Thermal voltage

V_g= Gate voltages (V_{g1}, V_{g2})

V_d = Drain voltages (V_{d1}, V_{d2})

w = the width of depletion region, w_2 and w_3 are used in equation (7)

W_{ch} = Channel width

R= The Resistance of channel

n =high concentration.

g_m= Transconductance

V_{PO}= Pinch off at the drain end of the channel

APPENDIX-B

MATLAB Code

Code for Drain Voltage V_d versus Drain Resistance R_d , by varying Gate Voltage V_g

```
%********** *** At Gate voltage Vg21 = 0.640V***************%

eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg21=0.640;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg21-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
 B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs = A*B+C;
Rd1 = Rs-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
 Rg=((Vg1-E)/Ig1)-(Rs/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
```

```
display(C);
display(Rs);
display(Rd1);
display(D);
display(E);
display(Rg);
title('Drain  Voltage  Vs Drain Resistance')
xlabel('Drain Voltage ,Vd2(V)');
ylabel(' Drain Resistance,Rd1(ohms)');

%********** At gate voltage Vg22 = 0.645V***********%

eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg22=0.645;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg22-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs = A*B+C;
Rd2 = Rs-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg=((Vg1-E)/Ig1)-(Rs/2);
display(W2);
```

```
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs);
display(Rd2);
display(D);
display(E);
display(Rg);
title( 'Drain Voltage  Vs Drain Resistance')
xlabel(' Drain voltage ,Vd2 (V)');
ylabel('Drain resistance,Rd2 (ohms)');

%*************** At gate voltage Vg23= 0.650V ****************%

eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg23=0.650;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg23-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A= (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs = A*B+C;
```

```
Rd3 = Rs-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg=((Vg1-E)/Ig1)-(Rs/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs);
display(Rd3);
display(D);
display(E);
display(Rg);
plot(Vd2,Rd1,'g',Vd2,Rd2,'b',Vd2,Rd3,'r');
xlabel('Drain Voltage,Vd(V)');
ylabel('Drain Resistance, Rd(ohms)');
title( 'Drain Voltage Vs Drain Resistance ')
xlabel('Drain Voltage , Vd (V)');
ylabel('Drain Resistance, Rd (ohms)');
```

Code for Drain Voltage V_d versus Gate Resistance R_g , by varying Gate Voltage V_g

```
%******** At gate voltages Vg21 = 0.640V**********%
eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg21=0.640;
Is=8.3*10^-7;
Ig1=0.0169;
```

```
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg21-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs = A*B+C;
Rd = Rs-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg1=((Vg1-E)/Ig1)-(Rs/2);
display (W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs);
display(Rd);
display(D);
display(E);
display(Rg1);
title('Drain VoltageVs Gate Resistance')
xlabel('Drain Voltage,Vd2(V)');
ylabel('Gate Resistance,Rg1(ohms)')

 %******** At gate voltage Vg22=0.645V********%
eta=1.6;
Vt=0.0259;
```

```
Ig=0.0169;
Vg1=0.55;
Vg22=0.645;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg22-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs = A*B+C;
Rd = Rs-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg2=((Vg1-E)/Ig1)-(Rs/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs);
display(Rd);
display(D);
display(E);
display(Rg2);
title('Drain voltage Vs  Gate Resistance')
xlabel('Drain voltage,Vd2(V)');
```

```
ylabel('Gate Resistance,Rg2(ohms)');

%******** At gate voltage Vg23 = 0.650V *********%
eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg23=0.650;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg23-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs = A*B+C;
Rd = Rs-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg3=((Vg1-E)/Ig1)-(Rs/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs);
display(Rd);
```

```
display(D);
display(E);
display(Rg3);
plot(Vd2,Rg1,'g',Vd2,Rg2,'b',Vd2,Rg3,'r');
Xlabel(' Drain Voltage,Vd2(V)');
Ylabel('Gate Resistance,Rg3(ohms)');
title('Drain voltage Vs Gate Resistance')
xlabel(' Drain Voltage,Vd2(V)');
ylabel('Gate resistance, Rg(ohms)');
```

Code for Drain Voltage V_d versus Source Resistance R_S, by varying Gate Voltage V_g

```
%**********At gate voltage Vg21=0.640V***********%
eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg21=0.640;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg21-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs1 = A*B+C;
Rd1 = Rs1-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
```

```
Rg=((Vg1-E)/Ig1)-(Rs1/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs1);
display(Rd1);
display(D);
display(E);
display(Rg);
title('Drain Voltage(Vd2) Vs Source Resistance(Rs)')
xlabel('Drain Voltage,Vd2(V)');
ylabel('Source Resistance,Rs1(ohms)');

%**********At gate voltage Vg22=0.645V************%
eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg22=0.645;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
W2 = (2/(eta*Vt))*(Vg22-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
```

```
C = (eta*Vt*W2)/Ig;
Rs2 = A*B+C;
Rd2 = Rs2-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg=((Vg1-E)/Ig1)-(Rs2/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs2);
display(Rd2);
display(D);
display(E);
display(Rg);
title('Drain Voltage2 Vs  Source Resistance')
xlabel('Drain Voltage,Vd2(V)');
ylabel('Source Resistance,Rs2(ohms)');

%*********At gate voltage Vg23=0.650************%
eta=1.6;
Vt=0.0259;
Ig=0.0169;
Vg1=0.55;
Vg23=0.650;
Is=8.3*10^-7;
Ig1=0.0169;
Vd2=0.20:0.01:1.00;
Vd1=0.03;
```

```
W2 = (2/(eta*Vt))*(Vg23-Vg1)+2*log(0.5);
W3 = exp((Vd2/(eta*Vt))-W2);
A = (2*eta*Vt)/Ig;
F= sqrt((W3.*W3)-(4.*W3));
B = log((0.5*W3)-(0.5*F));
C = (eta*Vt*W2)/Ig;
Rs3 = A*B+C;
Rd = Rs3-((2*Vd1)/Ig1);
D = (Ig1/(2*Is));
E = eta*Vt*log(1+D);
Rg=((Vg1-E)/Ig1)-(Rs3/2);
display(W2);
display(W3);
display(A);
display(F);
display(B);
display(C);
display(Rs3);
display(Rd);
display(D);
display(E);
display(Rg);
plot(Vd2,Rs1,'g',Vd2,Rs2,'b',Vd2,Rs3,'r');
xlabel('Drain Voltage,Vd2(V)');
ylabel('Source Resistance,Rs3(ohms)')
title('Drain Voltage(Vd2) Vs Source Resistance(Rs) ')
xlabel(' Drain Voltage,Vd2(V)');
ylabel(' Source Resistance, Rs(ohms)');
```