CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

OPERATING CHARACTERISTICS OF UTILITY INTERACTIVE INVERTERS USED IN PHOTOVOLTAIC SYSTEMS

A graduate project submitted in partial fulfillment of the requirements
For the degree of Master of Science in Electrical Engineering

By

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DEDICATION

This graduate project is dedicated to my family, both immediate and extended. Without their support my accomplishments would mean nothing. To all of the professors at California State University, Northridge who provided their knowledge, wisdom and expertise not only in their respective fields but also in regards to life. To my wife Nikki, to whom I owe my life to; without her unending support throughout these past couple of years, I would not be writing this sentence. Finally, to my son, whom I expect to see very soon, may you aspire to and achieve all the dreams that fill your mind.

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ABSTRACT

OPERATING CHARACTERISTICS OF UTILITY INTERACTIVE INVERTERS

USED IN PHOTOVOLTAIC SYSTEMS

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Master of Science in Electrical Engineering

The fundamental operating characteristics of the utility interactive, or grid connected, inverter is explored. The foundation of photovoltaic and power electronics is established, along with the concept of waveform inversion leading to the understanding of the inner workings of the utility interactive inverter. Various topologies of the inverter design are presented, along with discussions regarding switching devices, of which it is determined that currently the IGBT semiconductor devices are more applicable. The concept of utility synchronization is explored along with methods of accomplishing synchronization, such as Fourier filters, adaptive filtering, in-quadrature signal generation, phase locked loops, etc. Anti-Islanding methods are discussed, as pertaining to IEEE 1547 along with maximum power point tracking algorithms, of which it is determined that the perturb and observe method along with the incremental conductance method provide the most efficiency. Finally, the concepts are combined together to simulate an H-type full-bridge inverter topology with a second order generalized integrator (SOGI) frequency locked loop (FLL) with gain optimization and a unipolar pulse-width modulated control scheme coupled with a maximum power point tracking (MPPT) control block and algorithm driving a DC-DC step down converter. Simulations verify the concepts discussed and establish a concise text regarding a complete utility interactive inverter system.

INTRODUCTION

For hundreds of years, the use of fossil fuels have significantly shaped our lives, from the generation of electricity to the internal combustion engine that powers the automobiles we drive every day. Fossil fuels have brought about tremendous changes in the world as evident by the Industrial Revolution, which provided advancements in manufacturing, agriculture, and technology to name a few. These advancements have had a profoundly positive impact on human society as more job opportunities were available than ever before and a global economic infrastructure began to take shape as a result of mass production and transportation capabilities. However as technology has progressed, so has our understanding of the negative consequences from the use of fossil fuels.

According to a US Environmental Protection Agency (EPA) report released in 2011, almost 95% of the greenhouse gases that were generated in the United States in 2009 were due to the combustion of fossil fuels [1]. The results of this and many other similar studies have raised our awareness of the detrimental impact that the combustion of fossil fuels have on our environment and our health. This has provided a shift in our way of thinking, as now we assess the results of our actions and how they will affect our environment. In recent years, legislation has been passed to further our advancement and use of technologies utilizing renewable energy sources, such as wind, heat and sunlight.

As we now strive to become an environmentally friendly society, more and more companies and institutions are developing new technologies, and improving existing technologies, to take advantage of renewable energy sources. One such technology is the use of solar panels to generate electricity. Solar panels are able to accept sunlight and convert that energy into electricity, thus providing a viable energy source devoid of the harmful effects from the combustion of fossil fuels.

The production of electricity from the use of solar cells is nothing new. In fact, in 1839 French physicist A.E. Becquerel was the first to discover the photovoltaic effect while studying the effect of light on electrolytic cells. Little did he know that his discovery would eventually propel the human race into a new technological frontier and provide the means to power satellites and vehicles sent into orbit to explore the depths of our solar system and universe. However, as revolutionary as his discovery was, it was not until 1954 at Bell Laboratories when the first modern photovoltaic cell was developed. From that point on we have seen solar cells be utilized in anything from small electronics, such as calculators, to large scale solar panel installations capable of generating upwards of a few hundred megawatts (MW) of electricity. In fact, at the time of this writing, California State University Northridge has installed solar array systems in two areas of the campus with a total system size of 872 kW DC. Also, since its inception in March

2005, the solar array has generated over 10 megawatt-hours (MWh) of energy, enough energy to power over 206,000 homes for one day.

The use of solar panels for the generation of electricity is not limited only to large organizations such as energy companies or educational institutions. Due to advancements in technology and the public's awareness of the availability of such technologies, many home owners have installed solar panels on the roofs of their homes to generate their own electricity and thus reduce their energy costs and reduce the amount of fossil fuels consumed by power plants. Some governments even offer incentives and rebates for home owners who install such panels on their homes.

As a result, the quantity of solar panel installations throughout the world has tremendously increased in recent years. This has in turn caused many startup companies to emerge in order to provide the hardware and installation services of solar panel systems. As we see a proliferation of solar panel installations, the engineering community must be able to provide the technology that will accommodate the needs of the different types of consumers of these photovoltaic systems.

For example, a residential installation of a solar panel system would have to allow for both a stand-alone system and one that is going to be grid connected, which will be able to feed any unused energy back into the system. This will also hold true for commercial installations, however, these installations must be able to provide 3-phase power, as opposed to single phase power found in residential installations. These and other issues such as anti-islanding, synchronization, etc. will be touched upon along with a general introduction to photovoltaic systems and their properties.

However, no matter the type of system to be designed and installed, one piece of hardware is essential to the proper operation of the photovoltaic system, the inverter. The inverter is one of the most important components of the system and its proper operation is crucial to the efficiency and feasibility of the solar panel installation. Its most fundamental operation is to transform the direct current (DC) generated by the solar cells into alternating current (AC) that is used in ALL residential and commercial buildings as its electrical power source, which we will discuss in further detail.

We will focus on all aspects of the inverter as it applies to grid connected/utility interactive applications. Basic photovoltaic theory will be introduced to set a foundation in regards to the spirit of this text, along with general engineering concepts that will be needed for a complete understanding. Power electronics, in relation to the inverter, will be heavily relied upon and topics related to photovoltaic systems, such as Maximum Power Point Tracking (MPPT), utility synchronization and anti-islanding techniques will

be explored. The motivation behind this project is to provide a unified source of information regarding photovoltaic theory and its application in utility interactive inverter technology.

PHOTOVOLTAIC THEORY

Introduction

The photovoltaic effect, as stated previously, was discovered in the 19th century; and since then, advancements in science and technology have enabled us to successfully harvest solar energy from our sun and convert it into electrical energy capable of powering the appliances and devices we use on a daily basis. The mass production of semiconductors, using elements such as silicon, has no doubt contributed to the proliferation of solar cells in the market, considering that the semiconductor material is the fundamental component of the cell and photovoltaic theory. As such, to further explore the subject of photovoltaics, we must first establish an adequate understanding of the science involved.

Sunlight is a form of electromagnetic radiation (EMR), that is, energy with both an electric and magnetic field component that travels in a wave-shaped pattern through space. The basic unit of EMR, and thus sunlight, is a mass-less, charge-less elementary particle called the photon. Since EMR has been proven to travel in a wave-like pattern, so must the photon. Also, all wave-like patterns have an associated wavelength, λ, and the photon is no exception. Since the photon is mass-less, its energy is dependent only upon its wavelength, which can be shown as

$$(1) \quad E_\lambda = \frac{hc}{\lambda}$$

where h is Planck's constant ($6.62606957 \times 10^{-34}$ J·s or $4.135667516 \times 10^{-15}$ Ev·s), c is the speed of light/photon (299792458 m/s) and λ is the wavelength of the photon. For example, the energy of a photon with a wavelength of 700nm (visible light of the color red) is approximately 1.39×10^{-31} J·s or 1.77 Ev·s. The importance of Equation (1) is realized in the fact that only photons with energy greater than the semiconductor band gap (E_G) will contribute to the energy conversion process. This energy must be enough to form an electron-hole pair in the semiconductor material. As such, the spectral nature of sunlight is an important consideration in the design of efficient solar cells. We will explore the semiconductor band gap further in the text.

The creation of multiple electron-hole pairs in the semiconductor generates an electrical current between n-type and p-type materials, due to the simple fact that electrons and holes are carriers of electrical current. To compare this process to a familiar electrical process and facilitate a general understanding, the semiconductor can be thought of as a diode that allows the passage of electrical current through its terminals in a particular

direction, after it has absorbed the energy of sunlight and converted into an electrical current. Figure 1 shows the structure of a conventional solar cell and also demonstrates the energy conversion process.

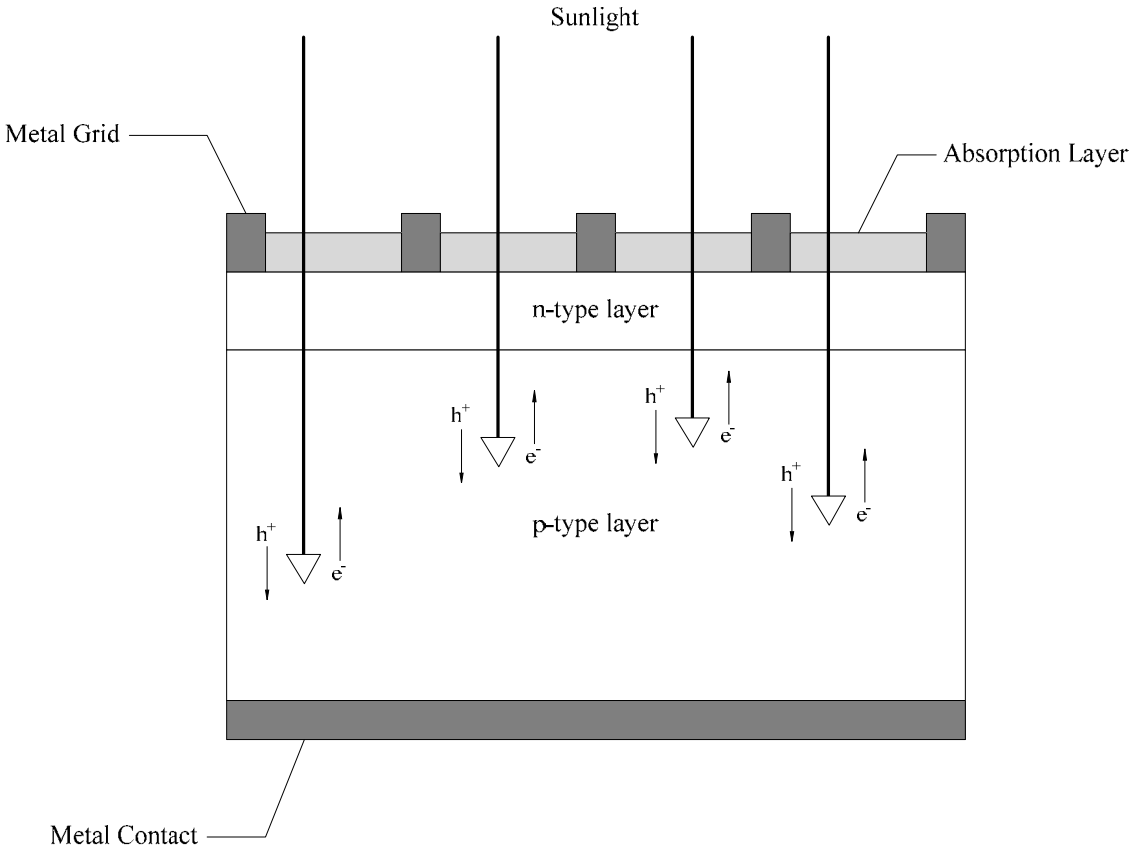


Figure 1 A conventional solar cell. Creation of electron-hole pairs, e^- and h^+. Generated current flows between the metal grid and metal contact, which are opposite in polarity due to the migration of electrons and holes

Since the energy conversion process in the solar cell is highly reliant upon the energy available in sunlight, we must analyze the spectral irradiance of sunlight. The surface temperature of the sun is measured to be 5762 K and its radiation spectrum is closely approximated to that of a black-body radiator, a physical body that absorbs all wavelengths of incident electromagnetic radiation. Also, the emission of radiation from the sun, along with all black-body radiators, is isotropic, that is, it radiates uniformly in all directions. However, due to the fact that the Earth is such a great distance away from the sun (almost 150 million kilometers), only those photons emitted directly in the direction of the Earth will contribute to the solar spectrum as observed from the Earth. Since the atmosphere affects the spectral content and intensity of the radiation reaching Earth's surface from the sun, we must be able to measure this effect. This measurement is known as the Air Mass number and can be calculated by the following equation

$$(2) \quad Air\ Mass = \frac{1}{\cos\theta}$$

where θ is the angle of incidence (θ = 0 when the sun is directly overhead). An Air Mass number of 0 (AM0) is the spectral distribution just above the Earth's atmosphere. AM1.5 is a widely used standard used to compare solar cell performance that is normalized to a total power density of 1 Kw/m^2. The Air Mass number can be further defined in terms of whether or not the measured spectrum includes the diffuse component, such as when we observe the spectral content of sunlight from here on Earth due to the reflection and scattering in the atmosphere and surrounding landscape. For example, an Air Mass number of AM1.5d signifies that the measured spectrum does not include the diffuse component and is therefore direct, whereas AM1.5g signifies a global measurement that includes the diffuse component.

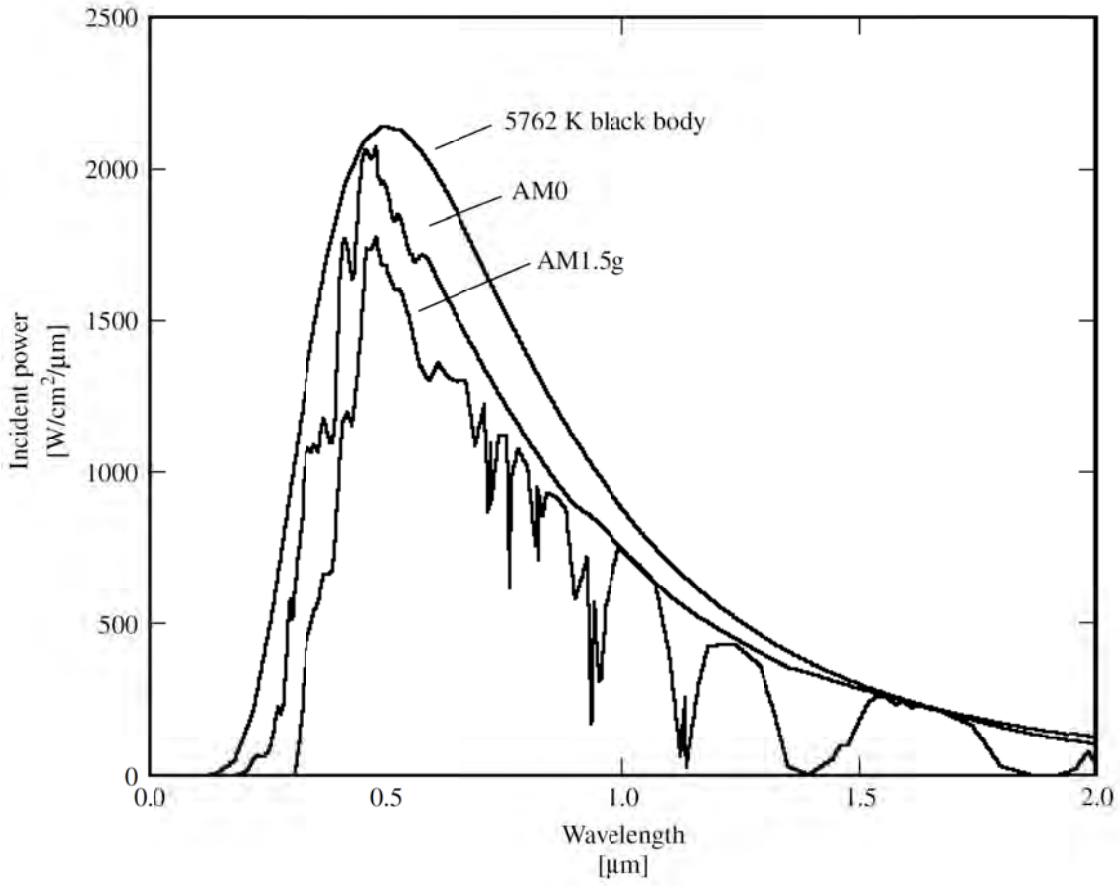


Figure 2 The radiation spectrum for a black-body at 5762 K, an AM0 spectrum, and an AM1.5 global spectrum [2]

As we can see in Figure 2, a 100 cm^2 surface area (the area of a typical solar cell used on a solar array panel) of sunlight on the Earth's surface can have an incident power up to

approximately 175 kW at approximately the 500 nm wavelength. However, we are well aware that a real-world solar cell will not produce power anywhere near the amount we observe in Figure 2. As such, we must explore the underlying operation of solar cells and to do so, we must understand some fundamental properties of semiconductors which will lead us to define the most basic attributes of the solar cell: the open-circuit voltage, V_{OC}; the short-circuit current, I_{SC}; the fill factor, FF; the conversion efficiency, η; and the collection efficiency, η_c.

Semiconductors

The discovery of semiconductors have allowed for some of the greatest technological advances in history. As shown earlier, the characteristics of semiconductors are ideal for their use in solar cells. The most common semiconductor material used in the fabrication of solar cells is silicon (Si), whether it be crystalline, polycrystalline, or amorphous. Although there are other materials such as GaAs, GaInP, and CdTe that can also be used, silicon has been the most common choice due to the fact that its absorption characteristics are a good match to our solar spectrum [2]. We will only provide the essential concepts of semiconductors as related to this paper. A more in depth analysis of semiconductors can be explored through sources [2, 5, 6], or others, if further explanation of the introductory material is required.

It was stated earlier that in order for the energy conversion process in semiconductor materials to occur, absorbed photons must have an energy greater than the semiconductor's band gap (E_G). The material's band gap is essential to the solar energy conversion process. The best way to understand the energy conversion process, and consequently the band gap, is to analyze how electrons behave and essentially what it takes to get those electrons excited. Electrons carry a negative charge, and when a large number of electrons move in the same direction, they form an electric current. Borrowing from quantum mechanics, electrons in an atom can be thought of as being somewhere in an array of possible "states" – which include their energy level, momentum and spin – with different probabilities of being in a given state. Two electrons cannot be in the same state at the same time; at least one of the aforementioned variables must be different. Some particular states are possible, and some are forbidden by the laws of quantum mechanics. Sets of possible states form regions that are called bands. Set of states that are not possible form regions between those bands, and these are called band gaps. In order to create electrical current in the semiconductor material, enough energy is needed to excite the electrons to move between the bands, and thus, through the band gap. Figure 3 illustrates this concept by plotting the energy E versus the crystal momentum p. Materials with a fairly large band gap are referred to as *insulators*. The

large band gap between the valence and conductions bands of insulators prevent electrons from reaching

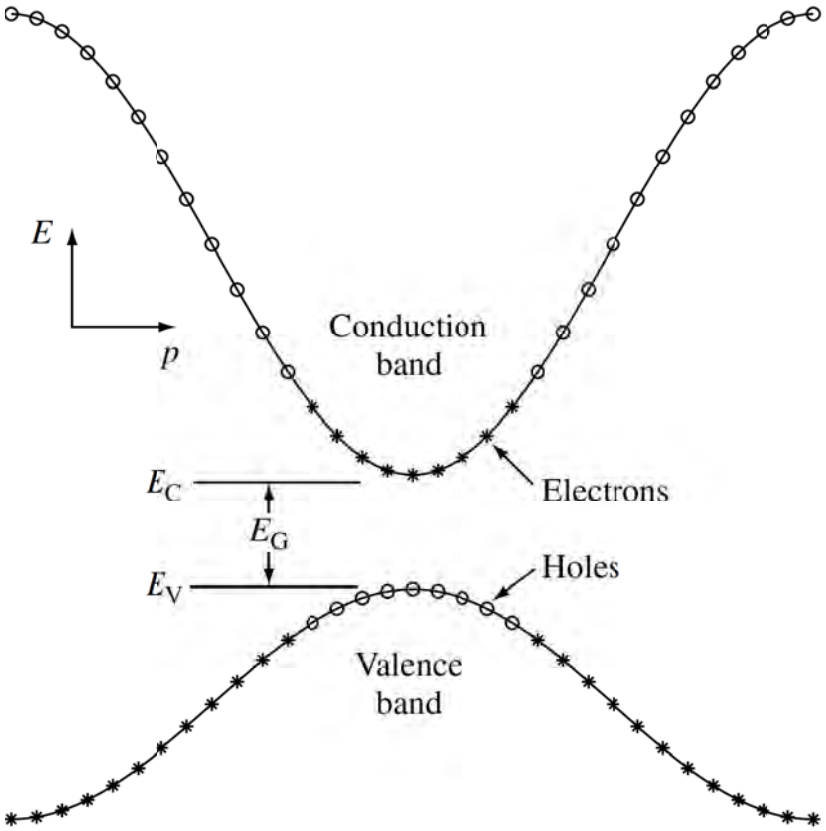


Figure 3 A simplified energy band diagram at $T > 0$ K for a direct band gap (E_G) semiconductor [2]

the conductions at ordinary temperatures, such as what we experience here on Earth. *Conductors*, on the other hand, have overlapping bands with no band gap, which means that their electrons are essentially free to move from the valence band to the conduction band. As one can already imagine, semiconductors can act as both insulators and conductors directly due to their band gap. At lower energy levels, semiconductors will not conduct electricity, whereas at higher energy levels, the semiconductor behaves like a conductor in its electrical characteristics.

As we are well aware, different materials have different characteristics, and semiconductors are no exception. Semiconductors have two different types of band gaps: *direct band gaps*, as seen in Figure 3, and *indirect band gaps*. The difference between the two is actually quite simple. When the minimum of the conduction band and the maximum of the valence band occur at the same value of the crystal momentum, as shown in Figure 3, the material is considered a *direct band gap* semiconductor. When they do not align, then the semiconductor is said to be an *indirect band gap* semiconductor. Si is an indirect band gap semiconductor, whereas CdTe or GaAs, for example, are direct band gap semiconductors. One can deduce from Figure 3 that direct

band gap materials are a much better candidate for solar cell fabrication compared to indirect band gap materials as they will absorb light better due to the amount of energy needed to move electrons between bands. However, Si, an indirect band gap semiconductor, is the most common material used to make solar cells. This may be attributed to the availability and cost of production of Si compared to other semiconductor materials. As stated previously, a more in-depth analysis can be attained through sources [2, 5, 6] and others.

Figure 4 depicts the structure of a simple solar cell to assist in attaining the fundamental properties of a solar cell pertaining to photovoltaic energy production: the short-circuit current, open circuit voltage and the fill factor.

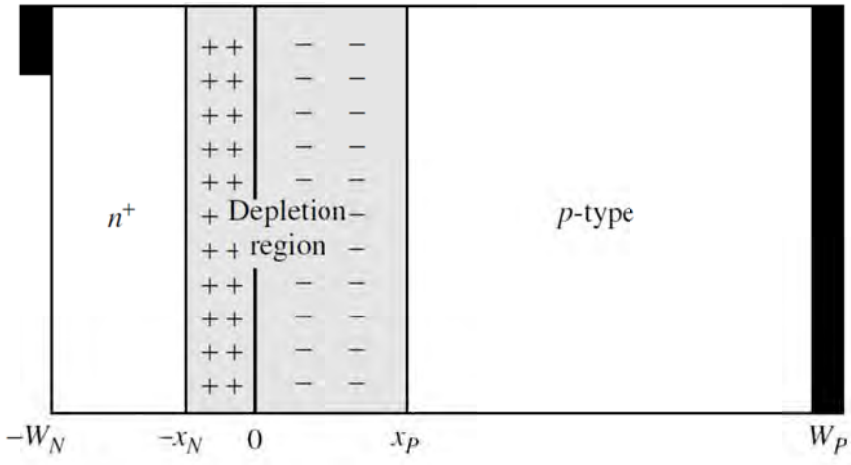


Figure 4 Simple solar cell structure used to analyze the operation of a solar cell. Free carriers have diffused across the junction (x = 0) leaving a space-charge or depletion region practically devoid of any free or mobile charges. The fixed charges in the depletion region are due to ionized donors on the n-side and ionized acceptors on the p-side [2]

During the solar energy conversion process, electrical current flows through the solar cell's terminals at $x = W_P$ and $x = -W_N$. Without exhausting the derivation, a solar cell's short-circuit current can be defined as

$$(3) \quad I_{SC} = I_{SCN} + I_{SCD} + I_{SCP}$$

where I_{SC} is the short-circuit current and is the summation of the short-circuit current from each of the three regions: the *n*-type region (I_{SCN}), the depletion region (I_{SCD}), and the *p*-type region (I_{SCP}). By observing Figure 4, this conclusion can be made rather easily, however, a full mathematical derivation of equation (3) is outside the scope of this paper and can be found in [2].

We can furthermore represent the solar cell as an electrical circuit model, as shown below in Figure 5.

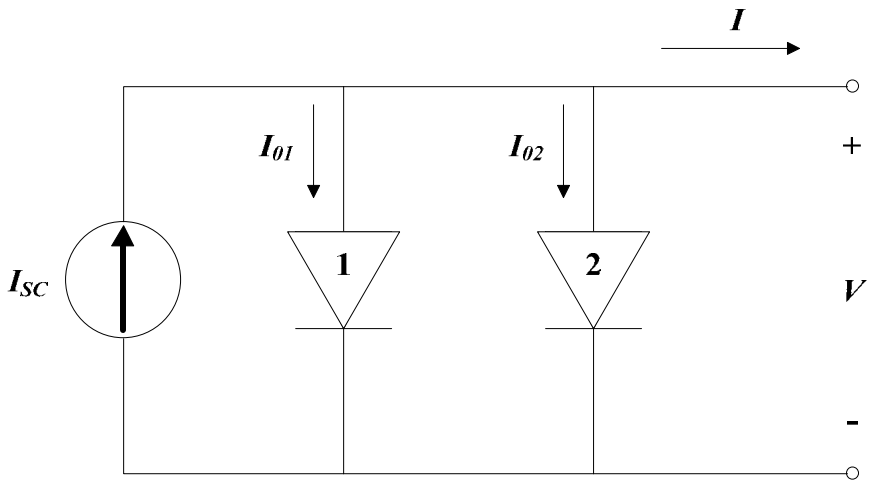


Figure 5 A simple solar cell circuit model. Diode 1 represents recombination in the quasi-neutral region, while diode 2 represents the recombination in the depletion region

Please note that for ease of discussion, we have not included parasitic series and shunt resistances inherent in real-world solar cells. As such, this is considered an idealized model of a typical solar cell. Using elementary circuit analysis and derivations shown in [2], we can represent the circuit model in Figure 5 with the following equation:

$$(4) \quad I = I_{SC} - I_{01}\left(e^{qV/kT} - 1\right) - I_{02}\left(e^{qV/2kT} - 1\right)$$

where I_{01} is the dark saturation current due to recombination in the quasi-neutral regions, I_{02} is the dark saturation current due to recombination in the depletion (space-charge) region, q is the magnitude of the charge of an elementary electron, k is Boltzmann's constant, and T is the temperature in Kelvin [2]. A common and reasonable assumption for a good silicon solar cell is the elimination of diode 2, the dark saturation current due to the depletion region. This model, along with derivations made in [2], allows us to plot the current-voltage characteristic of a given silicon solar cell in Figure 6.

This plot illustrates the important characteristics of the solar cell: the short-circuit current, the open-circuit voltage, and the fill factor. When the applied voltage, V, is small, the diode current is negligible and current can be approximated to the short-circuit current, I_{SC} (set $V = 0$ in equation (4)). Conversely, when the applied voltage is high enough that the recombination current (diode current) becomes significant, the solar cell current, I_{SC}, quickly drops to zero.

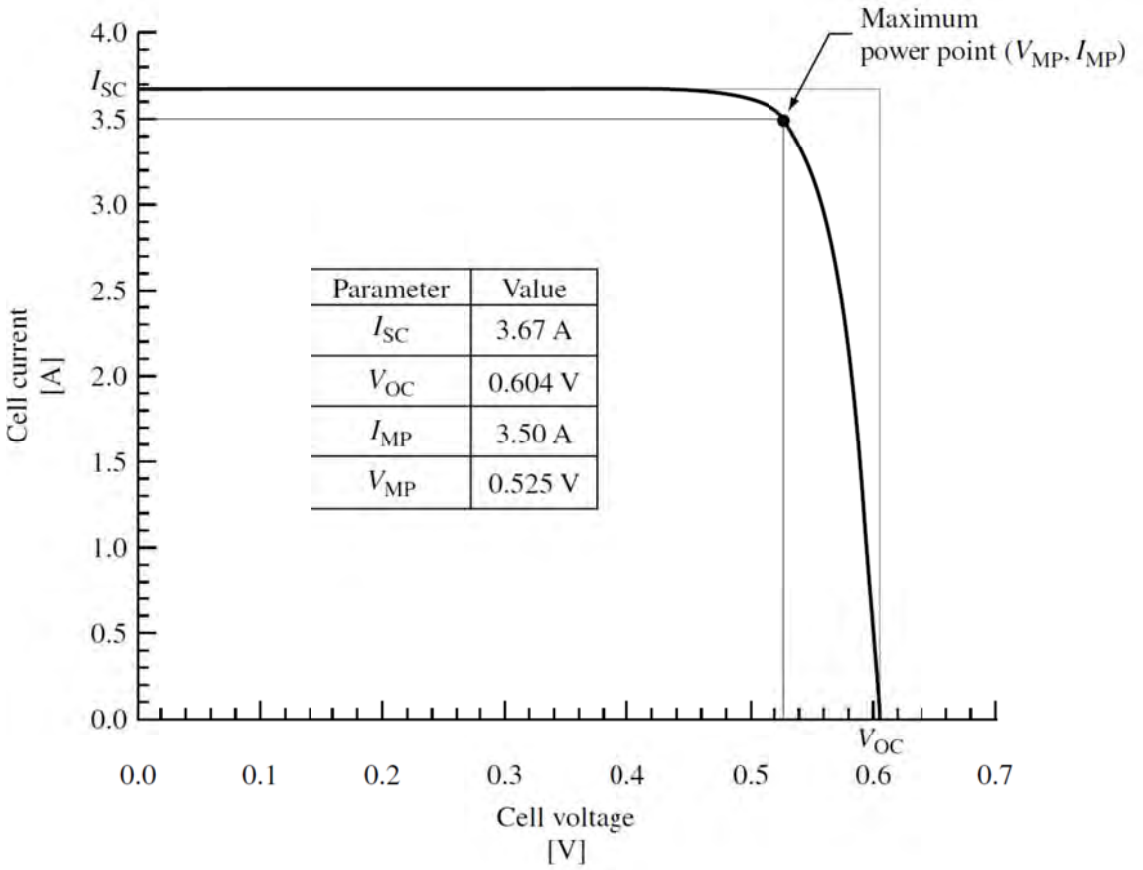


Figure 6 Current-voltage characteristic of a typical silicon solar cell [2]

In an open-circuit condition (I = 0), all of the light-generated current, I_{SC}, is flowing entirely through diode 1, and thus, the open-circuit voltage, V_{OC}, can be written as

$$(5) \quad V_{OC} = \frac{kT}{q} ln \frac{I_{SC} + I_{01}}{I_{01}} \approx \frac{kT}{q} ln \frac{I_{SC}}{I_{01}}$$

where $I_{SC} >> I_{01}$. Please turn your attention to the "knee point" of the curve shown in Figure 6. This point is where the power produced by the solar cell is at a maximum. This is referred to as the *maximum power point*, $P_{MP} = V_{MP}I_{MP}$. We will discuss in depth the use and calculation of the maximum power point in regard to inverters later in the text. Of particular interest is the rectangle whose area, given by P_{MP}, is the largest rectangle for any point on the *I-V* curve shown in Figure 6. The maximum power point is found by solving the following equation:

$$(6) \quad \left.\frac{\partial P}{\partial V}\right|_{V=V_{MP}} = \left.\frac{\partial (IV)}{\partial V}\right|_{V=V_{MP}} = \left.\left[I + V\frac{\partial I}{\partial V}\right]\right|_{V=V_{MP}} = 0$$

The current at the maximum power point, I_{MP}, is then found by evaluating equation (4) at $V = V_{MP}$.

The fill factor, *FF*, is a measure of the "squareness" of the *I*-*V* characteristic curve in Figure 6, is always less than one, and can be defined as

$$(7) \quad FF = \frac{P_{MP}}{V_{OC} I_{SC}} = \frac{V_{MP} I_{MP}}{V_{OC} I_{SC}}$$

This ratio ultimately defines the actual maximum obtainable power of the solar cell. The fill factor is one of the most significant parameters in evaluating the energy yield of a solar cell, besides the efficiency.

The efficiency, η, of a photovoltaic cell is defined as

$$(8) \quad \eta = \frac{P_{MP}}{P_{in}} = \frac{FF V_{OC} I_{SC}}{P_{in}}$$

where, P_{in} is the *incident power* determined by the properties of the light spectrum incident upon the photovoltaic cell. Information regarding the experimental determination of said properties can be found in [2].

The last attribute of the photovoltaic cell we will discuss is the collection efficiency, η_C. A solar cell's collection efficiency is a measure of how well the cell is able to convert energy received from photons into electrical current. The collection efficiency can be defined in two ways: the external efficiency, η_C^{ext}, defined relative to both optical and recombination losses, and the internal efficiency, η_C^{int}, defined with respect to recombination losses only. The external collection efficiency can be calculated with the following equation

$$(9) \quad \eta_C^{ext} = \frac{I_{SC}}{I_{ph}}$$

where

$$(10) \quad I_{ph} = qA \int_{\lambda<\lambda_G} f(\lambda) d\lambda$$

is the maximum possible photocurrent that would result if all photons with $E > E_G$ ($\lambda < \lambda_G = hc/E_G$) created electron-hole pairs that were collected. *A* is defined as the area of the

solar cell and $f(\lambda)$ is defined as the photon flux shown in [2]. The internal collection efficiency can be calculated with the following equation

$$\eta_C^{int} = \frac{I_{SC}}{I_{gen}} \quad (11)$$

where

$$I_{gen} = qA(1-s)\int_{\lambda<\lambda_G}[1-r(\lambda)]f(\lambda)\left(1-e^{-\alpha(W_N+W_P)}\right)d\lambda \quad (12)$$

is the light generated current, s is defined as the grid-shadowing factor, $r(\lambda)$ is defined as the reflectance, α is defined as the reflection coefficient, W_N is defined as the width of the n region, and W_P is defined as the width of the p region [2]. This would represent the short-circuit current if every photon that is absorbed by the solar cell is collected and contributes to the short-circuit current. It should be noted that the average solar cell is only 10% efficient.

The characteristics discussed above are just the fundamental properties of photovoltaic theory and are presented to provide the required material necessary for proper comprehension of the subject. There is more information that may need to be explored for accurate system design, however, that would be beyond the scope of this paper. Please refer to [2] for further in-depth information regarding cell manufacturing, theoretical limits of photovoltaic conversion, semiconductor composition and other important topics regarding photovoltaic theory.

A Complete Photovoltaic System

Departing momentarily from theory, let us take a more practical approach in understanding the photovoltaic system as a whole, as it pertains to our daily lives. We now have some knowledge pertaining to the solar cell and its major characteristics. Our next task is to apply this knowledge and benefit from the results.

Let us consider a single family home containing 4 family members. In the United States, the average energy consumption is 12000 kWh/person/year. However, this includes all the energy required at work, school and the energy required to produce goods purchased by each person. Therefore, if we assume that, on average, the energy consumption per-capita at home is one-third of the average energy consumption, we can conclude that energy consumption at the home is 4000 kWh/person/year. Dividing by 365 days a year and multiplying by 4 members of the single family we have approximately 44 kWh/day

of energy consumption. We must now determine the size of the photovoltaic array to be installed, along with an adequately sized inverter to convert the DC generated by the solar panel(s) into AC used throughout the home. Other considerations such as conductor sizing, circuit protection, etc. will be omitted in this paper but must be considered at the time of system design.

According to [3], solar irradiance has been measured to be 1.3608 kW/m^2 and thus the daily value of solar energy per square meter in terms of kilowatt hours is approximately 32.66 kWh/m^2. Given the fact that the average photovoltaic cell is only 10% efficient, this value becomes 3.266 kWh/m^2/day. Therefore, for an average single family home consisting of 4 members, the size of the required photovoltaic array would approximately be 13.5 m^2 (145 ft^2), which the average household roof can more than accommodate for.

Now to calculate the size of the inverter required, we must take into account that on average, present day inverters are 90% - 95% efficient, because some of the power is lost as heat during the conversion process. Therefore, if we divide 44 kWh/day by 24 h/day we will have approximately 1.83 kW, and taking into account a 90% efficiency rating of the inverter, we must install an inverter rated at least 2 kW.

Typically, the input voltages of inverters are between 140 VDC and 450 VDC, with 500 VDC being the maximum input voltage allowable. The output voltage of our panel(s) will vary throughout the day, each day, and will also vary with temperature. We must ensure that the total open-circuit voltage of the installed panels does not exceed the maximum allowable input voltage of the inverter.

Advances in technology and the photovoltaic cell fabrication process have led to the production of cells that are able to provide a much higher output in power than compared to the example shown in Figure 6, sometimes providing twice the maximum power point current under standard test conditions, STC (1 kW/m^2, 25°C, AM 1.5) [4]. Let us consider a typical 156mm x 156mm (6.14 in x 6.14 in) monocrystalline silicon cell used in many photovoltaic panels today. Each cell has the following specifications as shown in Table 1.

We can construct a solar module capable of producing 200 W by connecting together 50 monocrystalline silicon cells, whose specifications are shown in Table 1.

There are two ways to connect solar cells, as there are two ways to connect any electrical components together, in series or in parallel, as shown in Figure 7. Connecting cells in series effectively adds the output voltage of each cell, and in the same way, connecting cells in parallel adds the output current of each cell.

Parameter	Value
Maximum Power Rating (P_{MAX})	4 W
Open Circuit Voltage (V_{OC})	0.616 V
Short Circuit Current (I_{SC})	8.60 A
Maximum Power Voltage (V_{MP})	0.496 V
Maximum Power Current (I_{MP})	8.07 A

Table 1 Specifications of a typical 156mm x 156mm monocrystalline silicon cell at STC (1 Kw/m^2, 25°C, AM 1.5)

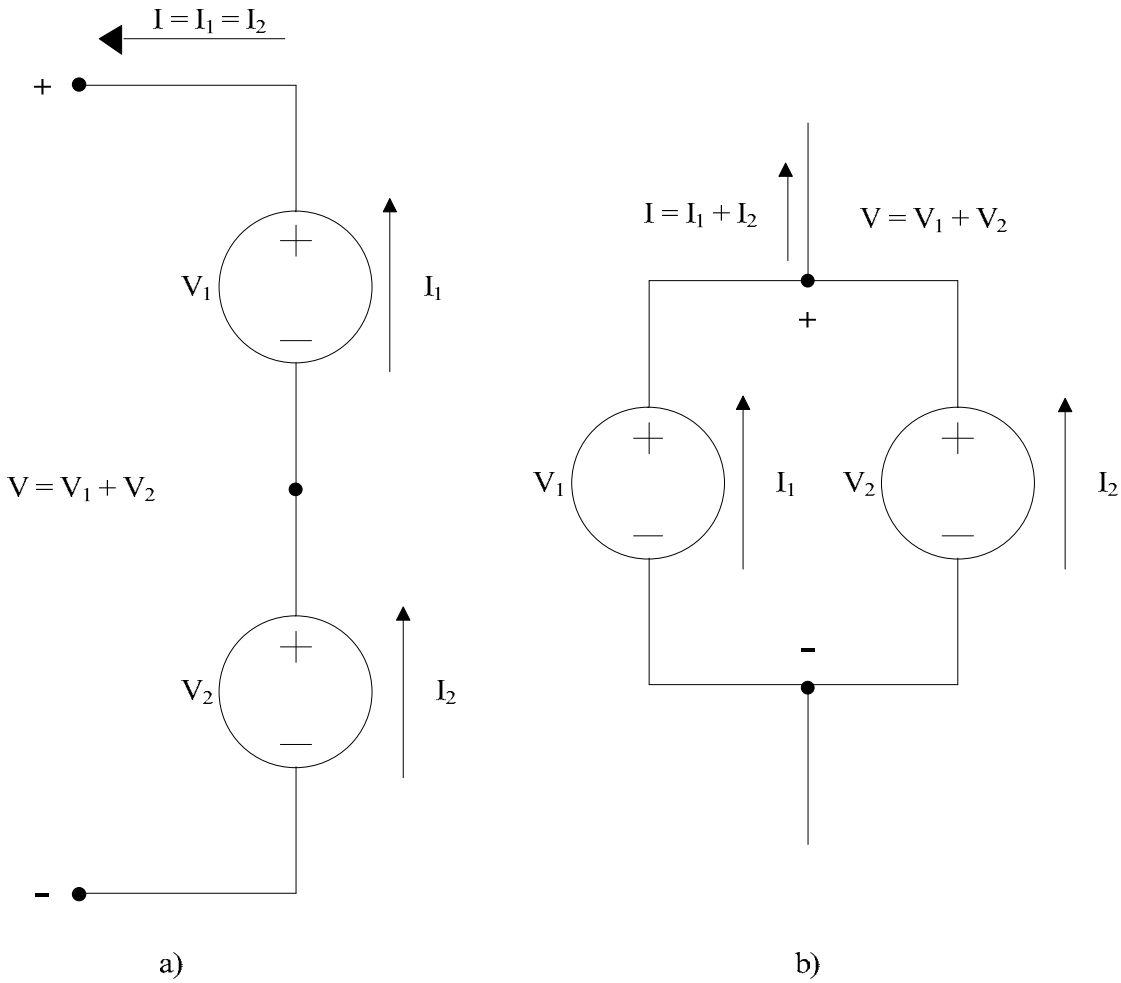


Figure 7 Solar Cell Connection a) Series Connection of Solar Cells b) Parallel Connection of Solar Cells

For simplicity, and to follow the convention of most photovoltaic module manufacturers today, let us construct a solar module by connecting 50 individual photovoltaic cells in series, as shown in Figure 8.

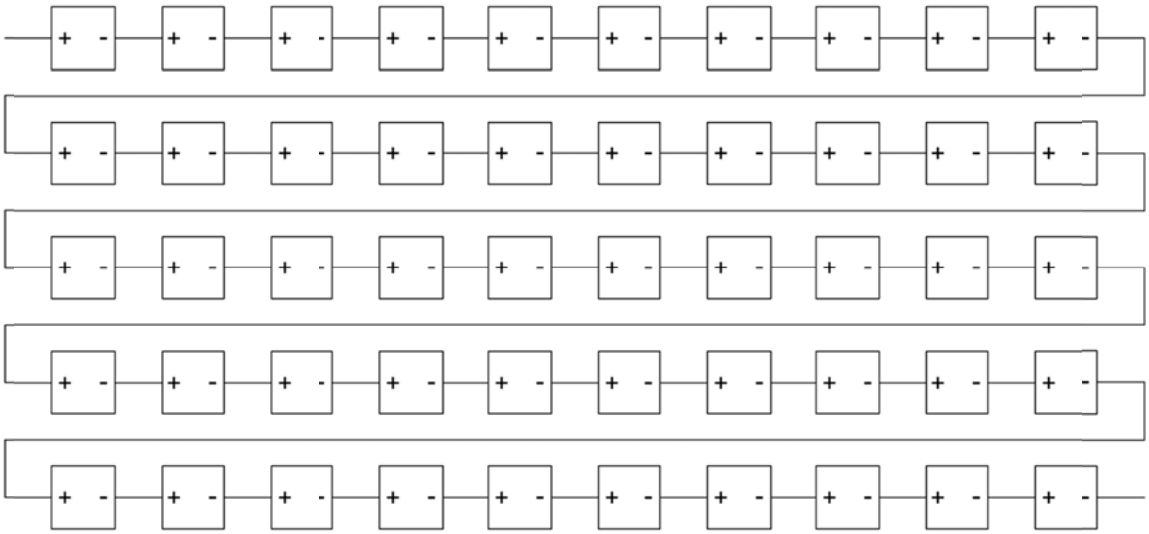


Figure 8 Electrical representation of a photovoltaic module with 50 series connected solar cells

As such, the module in our example will have the following specifications shown in Table 2 below. The dimensions of this module are 1.658 x .834 x .046m (5.44 x 2.74 x .151 ft), which corresponds to a surface area of 1.383 m^2 (14.89 ft^2).

Parameter	Value
Maximum Power Rating (P_{MAX})	200 W
Open Circuit Voltage (V_{OC})	30.8 V
Short Circuit Current (I_{SC})	8.6 A
Maximum Power Voltage (V_{MP})	24.8 V
Maximum Power Current (I_{MP})	8.07 A

Table 2 Specifications of a typical 50 cell photovoltaic module at STC (1 kW/m^2, 25°C, AM 1.5) [7]

To provide the average household of 4 with 1.83 kW of power, we will need to connect 10 of these photovoltaic modules in series, to create a photovoltaic array with the ratings shown in Table 3.

Parameter	Value
Maximum Power Rating (P_{MAX})	2 kW
Open Circuit Voltage (V_{OC})	308 V
Short Circuit Current (I_{SC})	8.6 A
Maximum Power Voltage (V_{MP})	248 V
Maximum Power Current (I_{MP})	8.07 A

Table 3 Ratings of a 10-module series array using modules with specifications shown in Table 2

This array will provide power for the 4 person household in our example and will only use 13.83 m^2 (148.9 ft^2) of the roof's surface area. This is strikingly close to the 13.5 m^2 (145 ft^2) we calculated earlier, the difference of which can be attributed to extra materials required in the fabrication process of a typical photovoltaic module. We can now construct a simple diagram for the photovoltaic system we designed for an average household of 4 people, as shown in Figure 9.

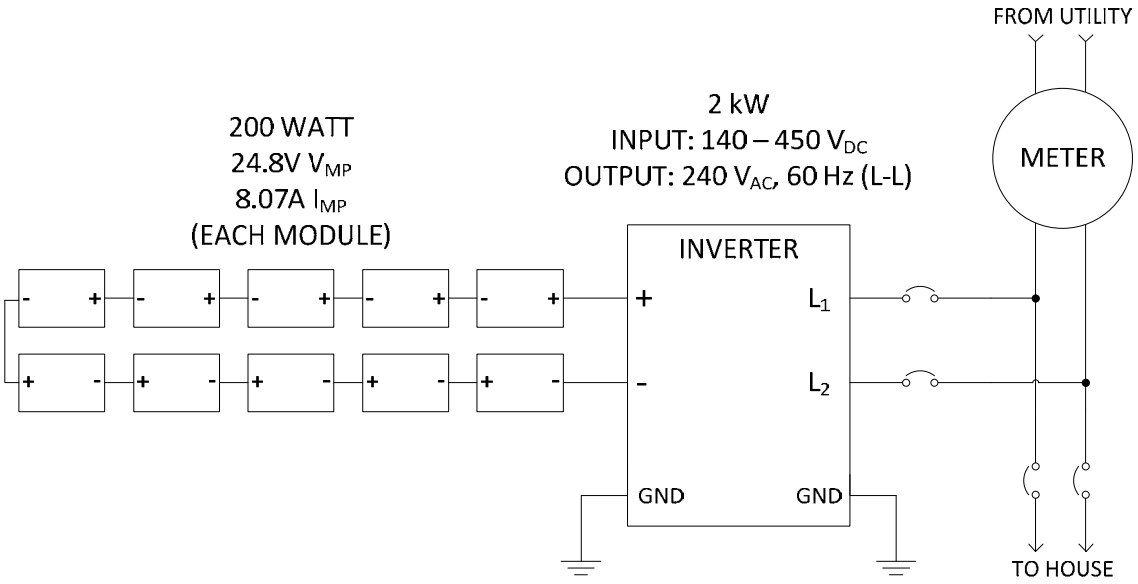


Figure 9 A simple 2 kW photovoltaic system for a typical 4 person household

As stated earlier, the reader may wish to explore in more detail in regard to photovoltaic theory and design by utilizing the sources referenced in this paper. We conclude our discussion of photovoltaics and turn to the heart of this paper, the inverter, beginning with applicable power electronics theory.

POWER ELECTRONICS THEORY – AS IT RELATES TO THE INVERTER

Introduction

Without a minimal knowledge of power electronics theory and concepts, the task of properly identifying and understanding the operating characteristics of an inverter would be insurmountable. Power electronics can be thought of, in a general sense, as a means to supply the proper voltages and currents to a load by way of processing and controlling electric energy through a mixture of power system and electronic components. To visualize this statement, Figure 10 illustrates a block diagram of an elementary power electronic system.

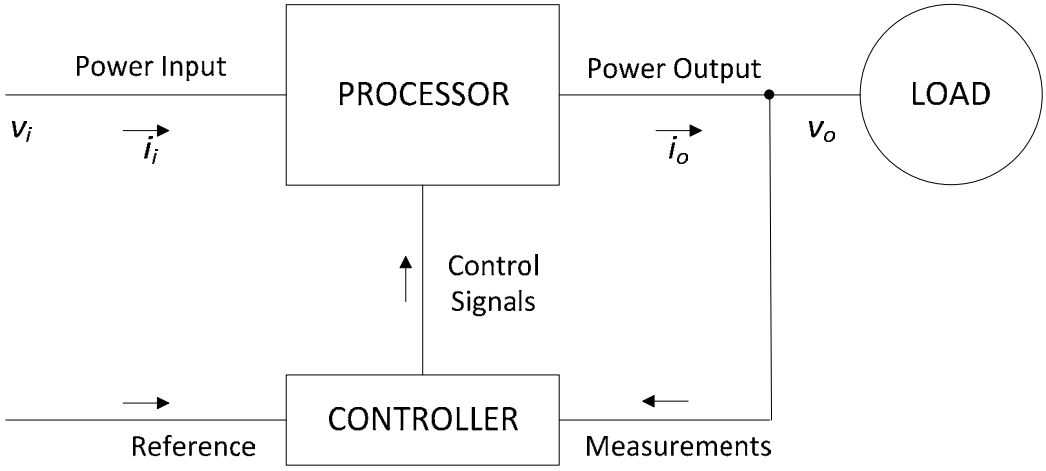


Figure 10 Block Diagram of an elementary power electronic system

We can easily see that the Processor in Figure 10 accepts an incoming power signal (which may be single or three phase) and produces a suitable output power signal for the Load based on information it receives from the Controller. For example, consider that our load accepts only a DC input and the only available input source available to us is an AC source. By following the block diagram in Figure 10, the Processor could be comprised of a high-frequency transformer, rectifier circuits and filtering circuits to convert the sinusoidal AC source to a DC source suitable for the Load. By the same token, the Controller could be comprised of a microcontroller which measures the output voltages of the rectifier circuit and filtering capacitor, compares it to a reference voltage and outputs a control signal to a MOSFET that controls the output of the transformer. This is just a simple example of the application of power electronics theory.

In recent years, major advancements in the fields of microelectronics and semiconductor fabrication have allowed for more robust system design, faster processing speeds, higher

voltage and current capabilities and faster semiconductor switching speeds. This allows for broader application of power electronics from simple household rectifying transformers to utility interactive inverters and beyond.

Steady State Concepts and Fourier Analysis

Before we dive into inverter theory, let us review some fundamental concepts required for an adequate understanding. Power electronics involves circuits that contain devices, such as diodes and switches, which constantly alternate between their respective on and off states. How can one determine if these circuits are in a state of transient response or in steady state? The steady state of a circuit is the condition in which the circuit waveforms begin to repeat within a time period of *T* seconds. For example, Figure 11 below shows a circuit waveform in which the initial state of the circuit is of a transient nature which then settles into a steady state form, much like the response of a circuit containing reactive components changing from an off state to an on state.

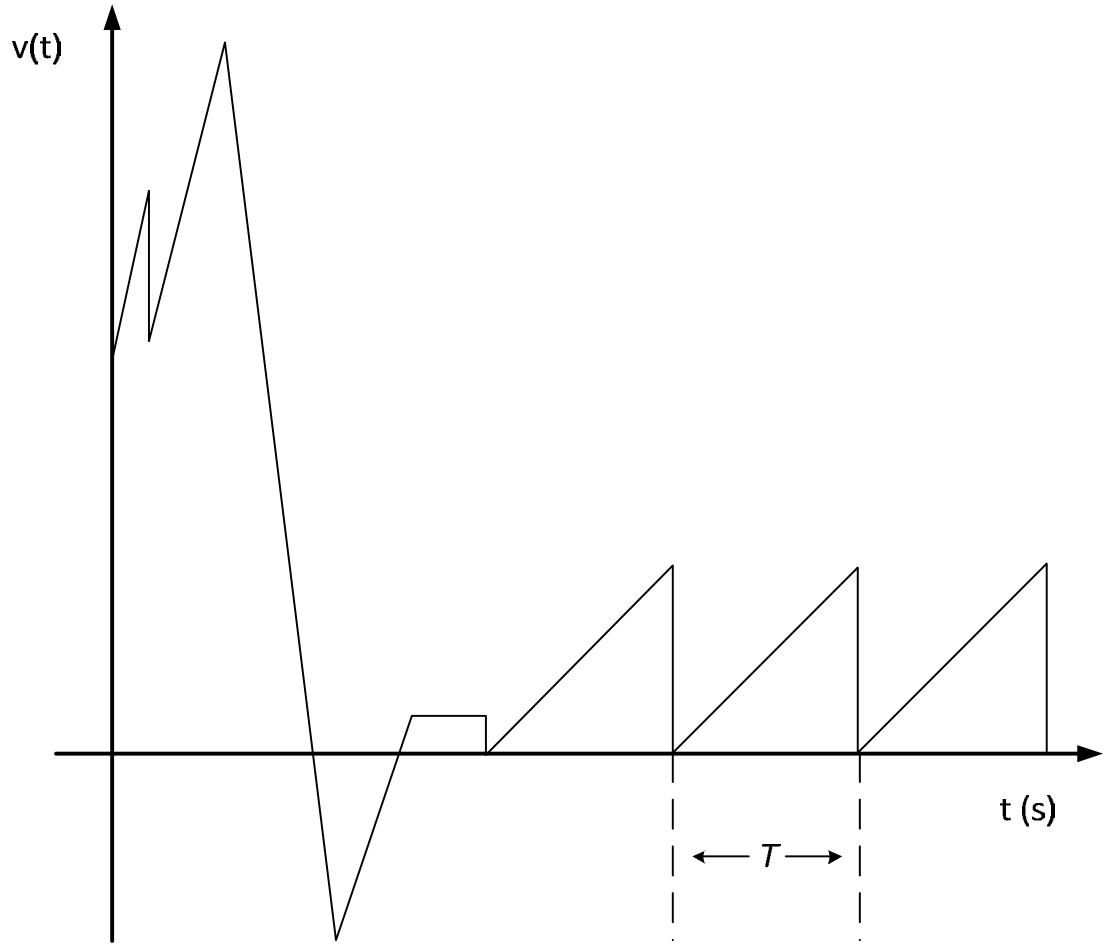


Figure 11 Example of a waveform with transient and steady state responses

Now consider that we must calculate the power generated/dissipated from a given circuit or part of a given circuit. The instantaneous power flow of any given circuit can be calculated as

$$p(t) = vi \tag{13}$$

where *v* and *i* are the time varying waveforms of voltage and current respectively. This does not give us usable information about the power of the circuit because it is different for each point in time. However, if *v* and *i* repeat with a time period *T* in steady state, then we can calculate the average power, which is a more useful piece of information than the instantaneous power. The average power can be calculated as

$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^T vi\ dt \tag{14}$$

If the circuit in question consists of a purely resistive load, then $v = Ri$ and can be substituted in equation (14) to yield

$$P_{av} = R\frac{1}{T}\int_0^T i^2 dt \tag{15}$$

Let us now consider the RMS value *I* of the current, rather than the instantaneous, and express the average power as

$$P_{av} = RI^2 \tag{16}$$

By comparing equations (15) and (16), we obtain

$$RI^2 = R\frac{1}{T}\int_0^T i^2 dt$$

And solving for the RMS current *I* yields,

$$I = \sqrt{\frac{1}{T}\int_0^T i^2 dt} \tag{17}$$

Examining equation (17) reveals to us the origin of RMS, as in Root Means Square. This is a general result and can be applied to all waveforms. Utilizing the same method, the RMS voltage *V* is determined to be

$$(18) \quad V = \sqrt{\frac{1}{T}\int_0^T v^2 dt}$$

By analysis, if *v* and *i* are a constant DC voltage and current, these equations would still remain valid except that the average and RMS values would be equal. Also, if the waveforms of *v* and *i* are purely sinusoidal, such as in an AC circuit, then we can calculate the RMS voltage and current to be

$$(19) \quad V = \frac{v}{\sqrt{2}} \quad I = \frac{i}{\sqrt{2}}$$

where *v* and *i* are the peak values of the instantaneous voltage and current waveforms respectively.

In power electronics, however, the more prevalent waveform is the nonsinusoidal waveform. This is due to the fact that most of the waveforms in power electronics are synthesized by using pieces and segments of an input waveform or waveforms. These waveforms are almost always highly distorted but are always analyzed in the steady state. As discussed earlier, the steady state waveform repeats with a time period *T* after an initial transient period has passed. As such, once the circuit is in steady state and the period *T* can be determined, the frequency of the waveform, *f*, can be calculated as

$$(20) \quad f = \frac{\omega}{2\pi} = \frac{1}{T}$$

where ω is known as the angular frequency in rad/s. The frequency *f* , in Hz, is known as the fundamental frequency and is usually denoted by a subscript 1. There are circuits, however, where components with unwanted frequencies may exist as a result of switching signals operating at a frequency other than the fundamental frequency, or they may be multiples, or harmonics of the fundamental frequency. These are best shown in Figure 12.

We can see that the general shape of the waveform is that of a square wave depicted by the dotted line. However, in order to obtain the square wave shape, a triangle waveform

was modified to produce the square wave and the resulting unwanted components generated by the switching devices can easily be seen.

It is important to calculate these components so as to determine the total distortion present in a particular circuit. Fourier analysis is used to calculate these components.

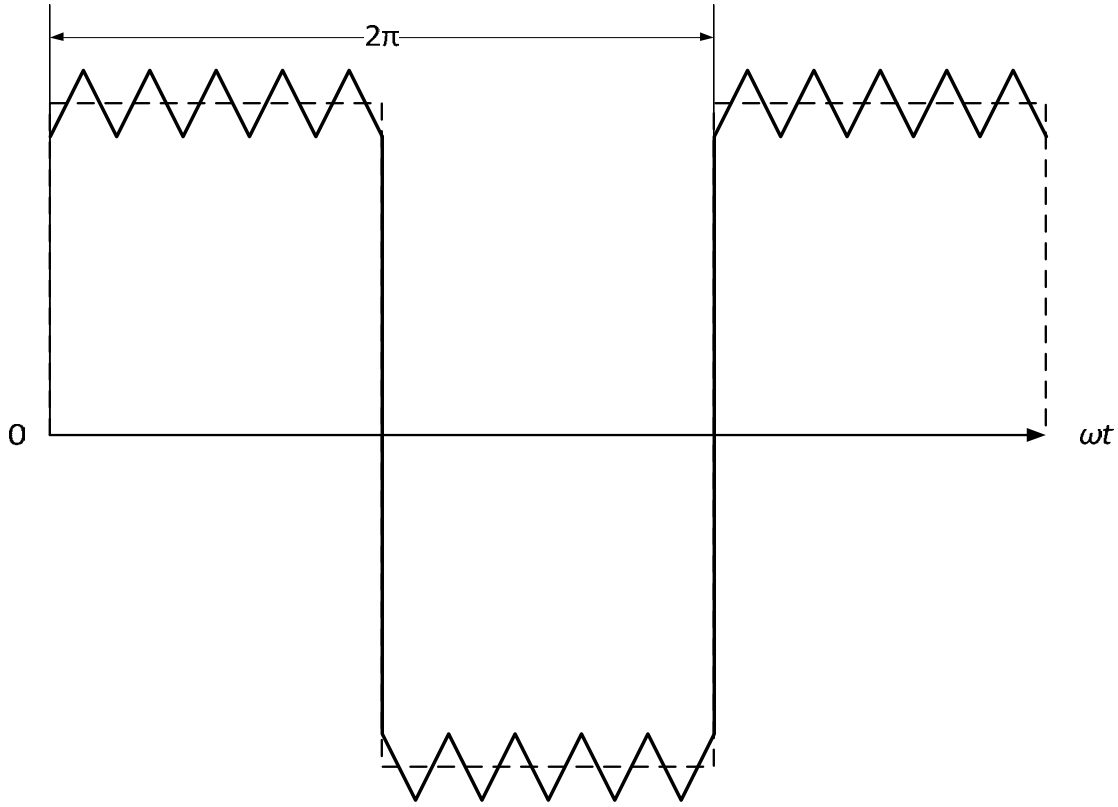


Figure 12 Example of a nonsinusoidal waveform with multiple frequency components

In general, a nonsinusoidal waveform *f(t)* repeating with an angular frequency ω can be expressed using a Fourier Infinite Series as shown below

$$(21) \quad f(t) = F_0 + \sum_{h=1}^{\infty} f_h(t) = \frac{1}{2}a_0 + \sum_{h=1}^{\infty}\{a_h \cos(h\omega t) + b_h \sin(h\omega t)\}$$

where

$$(22) \quad F_0 = \frac{1}{2}a_0 = \frac{1}{2\pi}\int_0^{2\pi} f(t)d(\omega t) = \frac{1}{T}\int_0^{T} f(t)dt$$

$$(23) \quad a_h = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(h\omega t)\, d(\omega t)$$

and

$$(24) \quad b_h = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(h\omega t)\, d(\omega t)$$

We can clearly see through these equations that a waveform in steady state is the sum of its Fourier components [8]. For example, a distorted waveform such as the one shown in Figure 12 can be synthesized by adding triangular waveforms at multiple pre-calculated frequencies to form the general shape of a square wave. By the same token, we can quantify the amount of distortion present in any periodic waveform by means of an index called the total harmonic distortion, or THD.

Leaving the derivation to the reader, the THD, usually shown in terms of percentage, is defined as

$$(25) \quad \%THD = 100 \times \frac{F_{dis}}{F_{s1}}$$

$$= 100 \times \frac{\sqrt{{F_s}^2 - {F_{s1}}^2}}{F_{s1}}$$

$$= 100 \times \sqrt{\sum_{h\neq 1}\left(\frac{F_{sh}}{F_{s1}}\right)^2}$$

The terms in equation (25) are all in RMS and are based under a simplifying assumption of a purely sinusoidal waveform F_{s1} at the fundamental frequency. The total waveform, F_s, is the square root of the sum of the square of F_{s1} and the sum of squares of all the waveforms containing multiples, or harmonics, of the fundamental waveform F_{sh}, where $h \neq 1$. The distorted waveform, F_{dis}, can be expressed as $\left[{F_s}^2 - {F_{s1}}^2\right]^{1/2}$.

Fourier analysis is fundamental in understanding concepts related to power electronics such as waveform shaping and calculation of total harmonic distortion (THD). It is left to the reader to further explore such topics for a more thorough understanding of Fourier analysis and its applications.

Semiconductor Switches

The concept of switching and the use of semiconductor switches are essential to the theory, design and use of power electronic circuits. These switches allow engineers to modify voltage and current signals and route them to appropriate loads or sub-circuits. Before beginning our discussion on switches, let us briefly take into account the fundamental element of switching losses. Switching losses arise from the momentary surge in power resulting from the closing or opening of a switch. This is better described through an illustration in Figure 13.

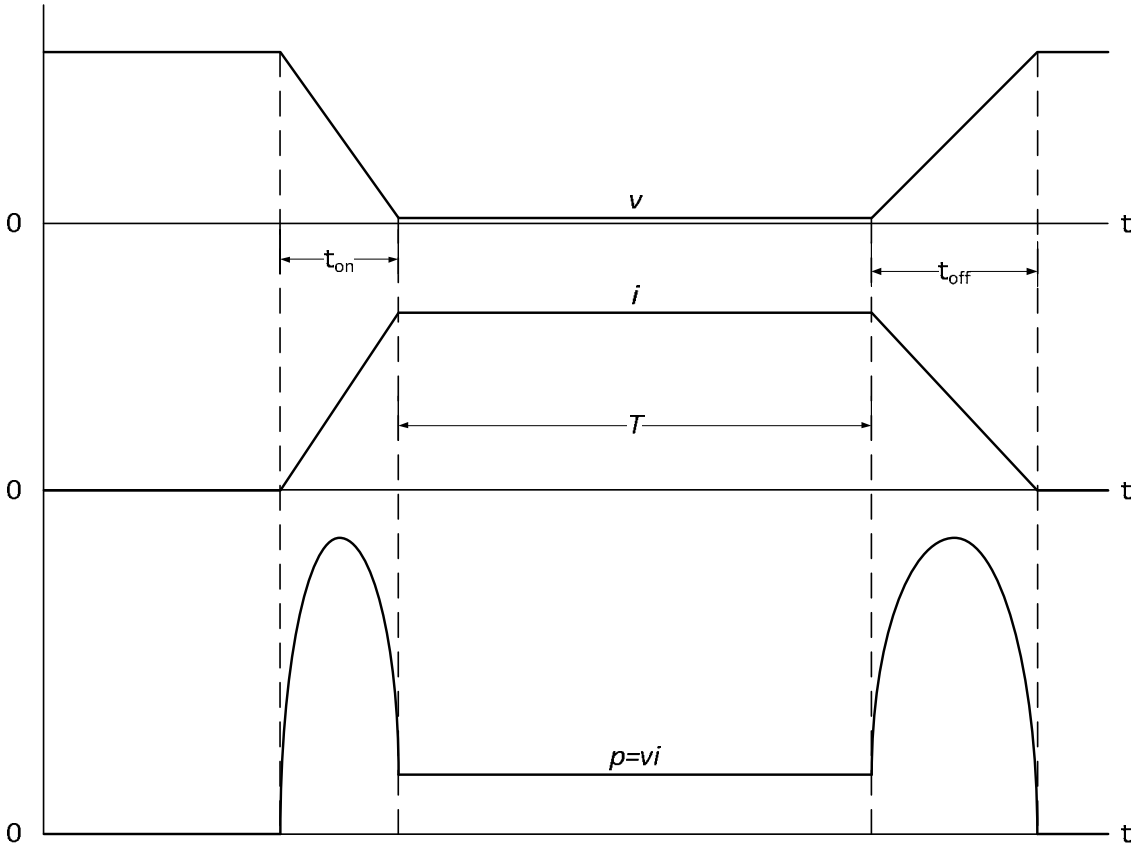


Figure 13 Voltage, Current and Power Loss waveforms of a semiconductor switch

The operation of a switch contains three states: turn-on, conduction and turn-off. When a switch is closed and is in the turn-on state, the voltage across its terminal drops from a large value down to almost zero within a time period t_{on}. Respectively, the current rises sharply from no current to its full current value during that same time interval. This results in a temporary spike in power during the turn-on state as seen in Figure 13. After the turn-on period has elapsed, the switch is in its steady state known as the conduction state, shown by *T* in Figure 13. When the switch is opened and is in the turn-off state, the

voltage across the switch begins to rise sharply within a time period t_{off}. And as such, the current drops sharply to zero during that same time period. This turn-off state, as seen in Figure 13, also generates a temporary spike in power. The average value of the sum of these spikes is known as *switching losses* and can be calculated by

$$(26) \quad P_{SW} = \left(\int_0^{t_{on}} p \, dt + \int_0^{t_{off}} p \, dt \right) f_{SW}$$

where f_{SW} is the frequency at which the switch operates. The total power loss of a switch is the sum of the power loss during the conduction state and the power loss due to switching and can be shown by

$$(27) \quad P_{total} = P_C + P_{SW}$$

Calculation of these losses is essential in determining the overall efficiency of the circuit and allows engineers to determine the correct devices needed.

One of the most important switching devices related to power electronics and inverter design is the power diode. Power diodes are considered to be an uncontrolled semiconductor switch, in that it operates without, and independent of, a control signal. The semiconductor structure and circuit symbol of a power diode are shown in Figure 14.

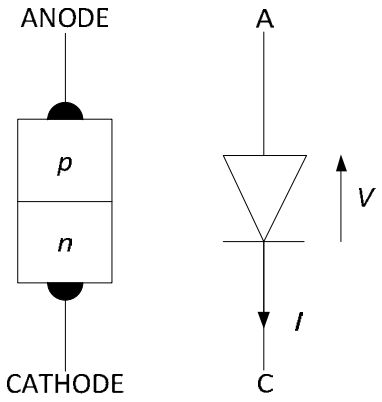


Figure 14 The semiconductor structure and circuit symbol of a typical power diode

The current in a diode can only flow from anode to cathode under forward bias conditions, that is, the voltage from cathode to anode must be positive and within a certain range. Current in the reverse direction is blocked when this voltage is not positive. The voltage-current characteristic of a power diode is shown in Figure 15.

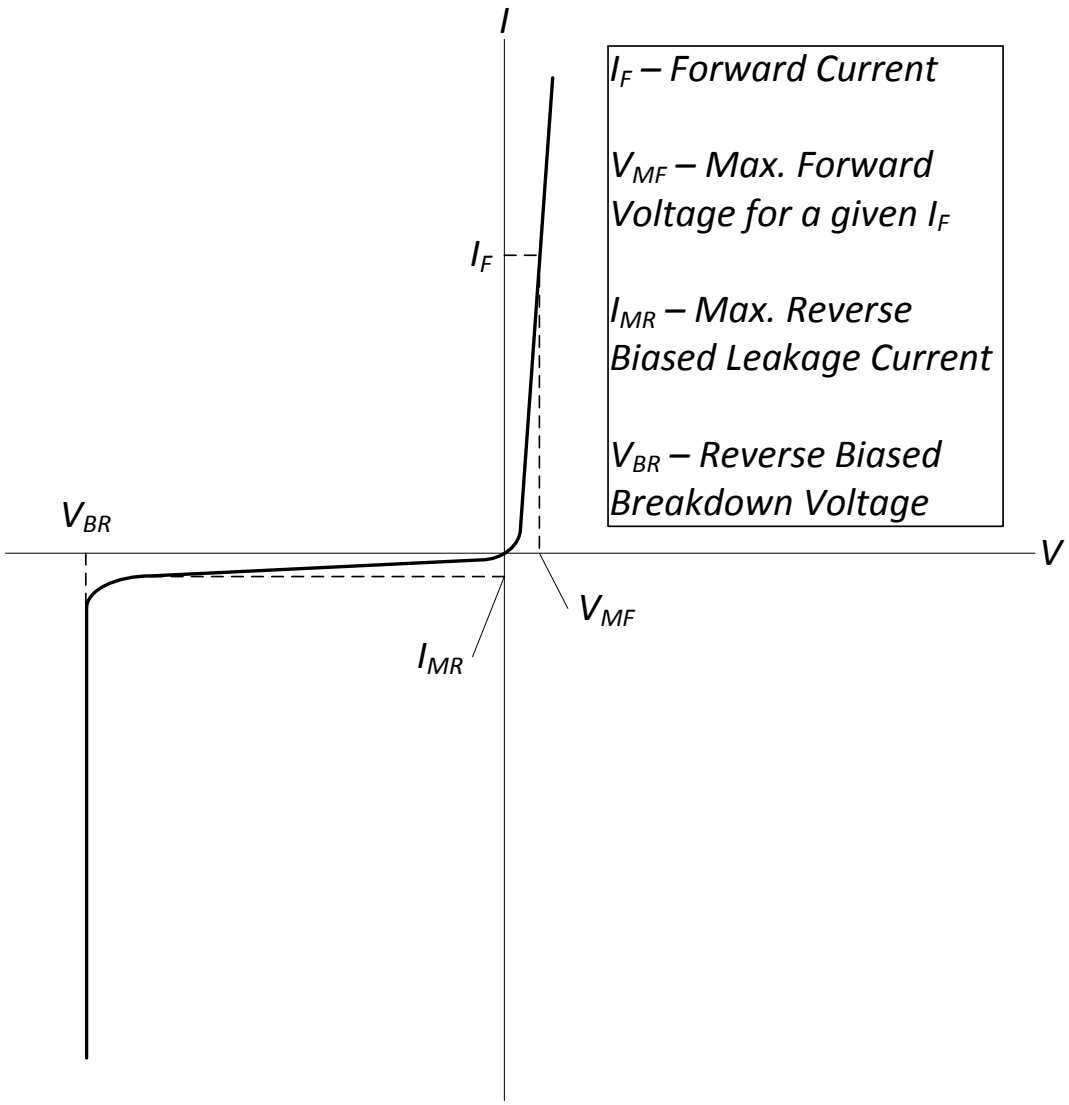


Figure 15 Voltage-Current characteristics of a typical power diode (Different scales are used for positive and negative half-axes)

Other important characteristics of the diode such as *reverse recovery time* are left for the reader to explore. We will also forgo a discussion on semi-controlled switches, such as the thyristor family of semiconductor devices (SCRs, Triacs) and instead focus on three types of fully controlled semiconductor switches predominantly used in modern inverter systems, Power BJTs, Power MOSFETs and IGBTs. This is not to say that these three are the only devices categorized as fully controlled switches, however, they are the most prevalent in inverter systems and most applicable in terms of the scope of this project.

The *bipolar junction transistor* (BJT) is a three terminal semiconductor device. An npn BJT is shown in Figure 16. The collector (C) to emitter (E) path serves as the switch,

conducting or interrupting the main current, while the base (B) is the control electrode which “opens” or “closes” the switch.

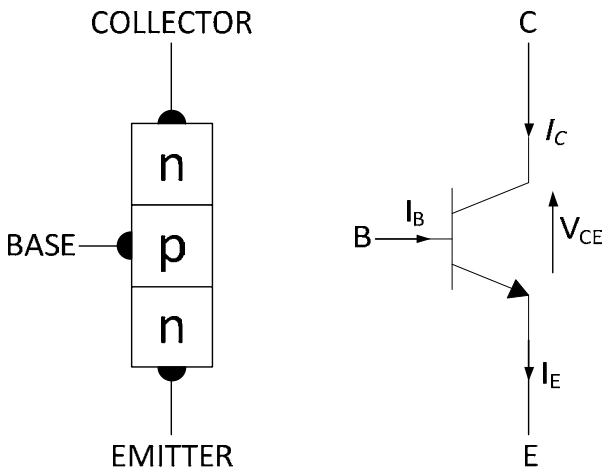


Figure 16 The semiconductor structure and circuit symbol of a typical power BJT

In contrast to the thyristor family of devices not discussed in this paper, the collector current, I_C, of the BJT can be controlled continuously by the base current, I_B, as follows

$$(28) \quad I_C = \beta I_B$$

where β is the *DC current gain* of the transistor. This is more commonly known as a current-controlled switch and requires additional circuitry to properly bias and operate. In general, BJTs offer very low conduction losses, however, the disadvantages outweigh the advantages by a considerable margin. The voltage-current characteristics of a typical BJT are shown in Figure 17. It is important to note that in order for conduction losses to be kept to a minimum, the base current in the on-state must be high enough for the operating point to lie on, or close to, the hard saturation line associated with the lowest voltage drop across the BJT, thus resulting in the lowest power loss. Also, the BJT cannot block negative collector-emitter voltages. As such, if used in an AC-input converter, such as an inverter, the BJT must be protected from reverse breakdown with a diode connected in series with the collector. In addition, the BJT is susceptible to what is known as a *second breakdown*. The second breakdown is different from the more commonly known reverse avalanche breakdown (first breakdown) in that it occurs when both the collector-emitter voltage and collector current are high, during turn-on or turn-off states. Local hotspots appear in the semiconductor due to crystal faults, or doping

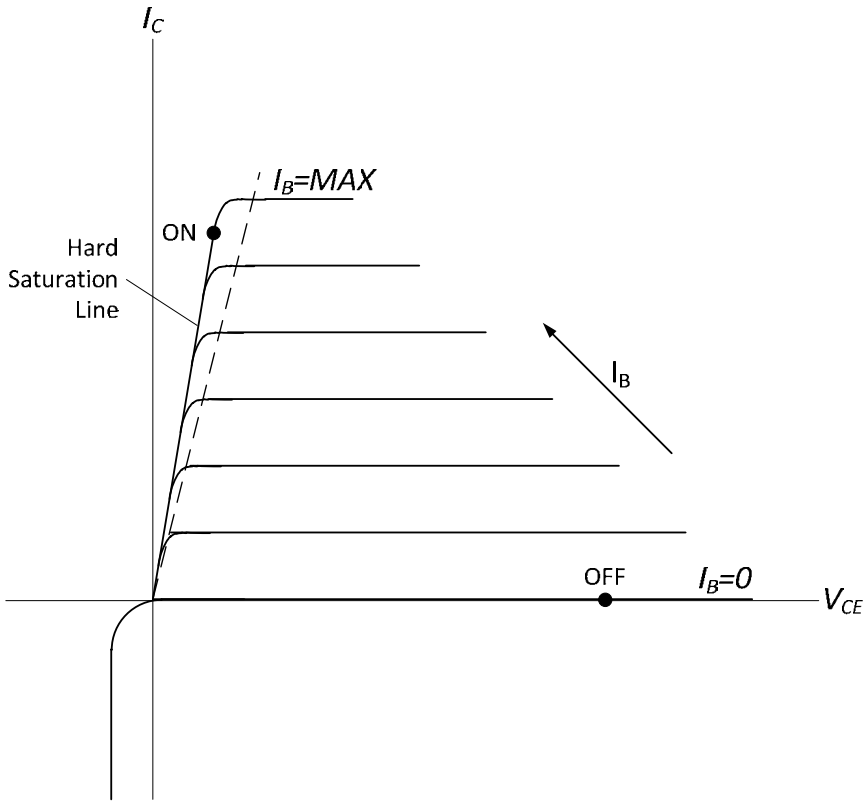


Figure 17 Voltage-Current characteristics of a typical power BJT

fluctuations, and high power losses. Throughout operation time, the temperature of these hotspots will rise ever higher and cause irreparable damage to the semiconductor. Another disadvantage of the BJT is its low current gain. As a result, multiple transistors must be used to provide a sufficient and usable current in power electronic converters. In recent years, power BJTs have been losing their market share to insulated-gate bipolar-transistors (IGBT), described later in the text. Voltage-controlled IGBTs possess all the advantages of BJTs, such as high current capability, without the weaknesses, such as second breakdown or current-controlled switching.

The power MOSFET (metal-oxide semiconductor field-effect transistor), shown in Figure 18, is best known for its high switching speed and simpler control circuitry. Also, MOSFETs have a negative temperature coefficient, which allows for paralleling transistors for increased current-handling capability along with uniform current density within the device, preventing second breakdown from occurring, as in BJTs. In addition,

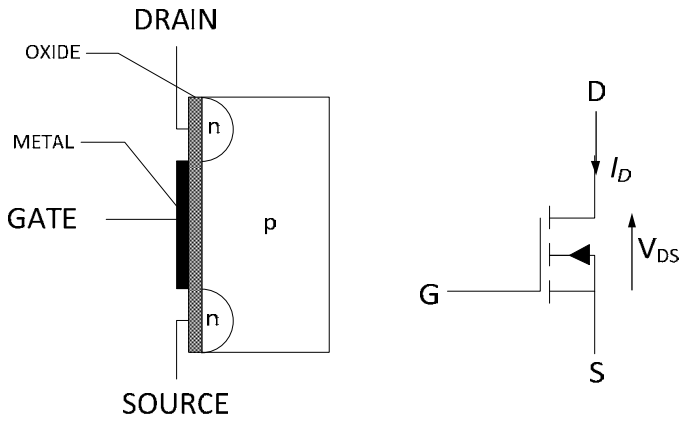


Figure 18 The semiconductor structure and circuit symbol of a typical power MOSFET

the short turn-on and turn-off times of the MOSFET result in low switching losses, even at the high switching frequencies used with MOSFETs. Similar to BJTs, MOSFETs cannot be exposed to negative drain-source voltages unless protected by a diode connected in series with the transistor. The main drawback of MOSFETs, however, is the inability to carry large currents. The characteristics of the MOSFET, as seen in Figure 19, are strikingly similar to those of the BJT.

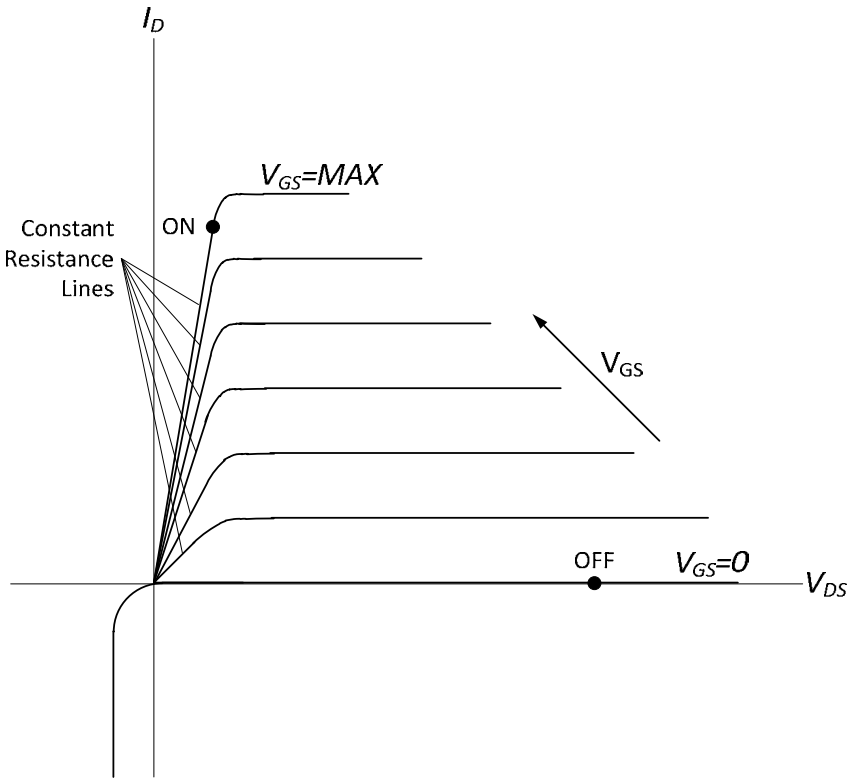


Figure 19 Voltage-Current characteristics of a typical power MOSFET

However, it should be noted that there is no hard saturation line as is present in BJTs. So the question arises, how can we incorporate the high current-handling capability of BJTs at higher switching frequencies of MOSFETs without the drawbacks of either device? The solution is the insulated gate bipolar transistor, shown in Figure 20.

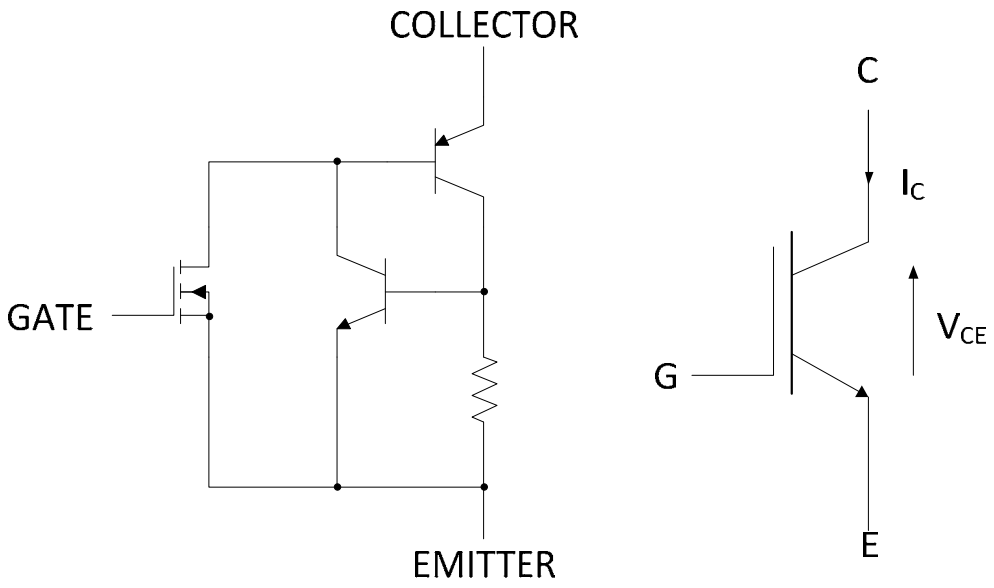


Figure 20 The equivalent circuit and circuit symbol of a typical IGBT

As can be seen, IGBTs are hybrid semiconductor devices, combining the advantages of MOSFET and BJT technologies. Like MOSFETs, they are voltage controlled but have lower conduction losses and higher voltage and current ratings. The voltage-current characteristics of a typical IGBT are shown in Figure 21. There are generally two types of IGBTs, the asymmetrical and symmetrical type. The majority of IGBTs available on the market are of the asymmetrical type, that is, they do not have reverse voltage blocking capability. Symmetrical IGBTs can block reverse voltages as high as the rated forward-blocked voltage. This is a great advantage of these devices provide, however, it comes at the cost of slightly higher conduction losses when compared to their asymmetrical counterpart.

The on-state voltage drop of IGBTs is comparable to BJTs but superior to power MOSFETs. Similar to MOSFETs, IGBTs are turned on by a gate-emitter voltage around 20 V and turned off by zero voltage. Also, IGBTs can be switched with frequencies undetectable by the human ear (exceeding 20 kHz). Lastly, the maximum voltage and current ratings currently available are 6.5 kV and 2.4 kA respectively. It is because of these advantages that IGBTs are the preferred semiconductor power switch for use in modern power electronics equipment, including utility interactive inverters.

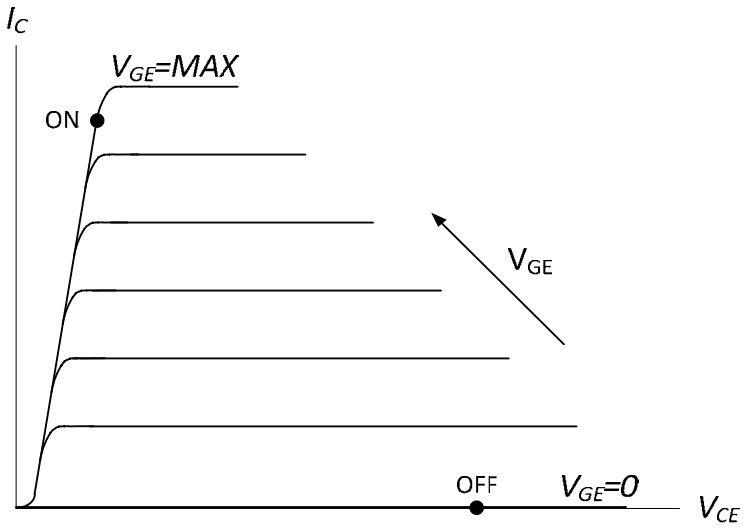


Figure 21 Voltage-Current characteristics of a typical IGBT

The Basic Inverter

We must now develop an understanding of waveform inversion and begin to apply it in our pursuit of identifying the crucial operating requirements of the utility interactive inverter. The concept of waveform inversion is rather elementary; given a particular waveform as an input, modify that waveform into a signal that is appropriate for the load in question. For our purposes, the load in question is the 60 Hz AC waveform of the utility's electrical supply and the input waveform that needs modifying is a DC signal from a photovoltaic module. Let us begin with the most basic topology of a DC to AC inverter circuit shown in Figure 22. This topology is better known as the H-Bridge, or

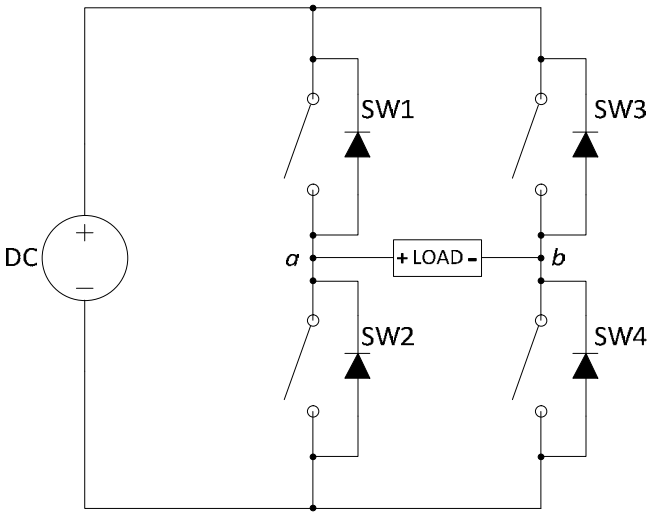


Figure 22 Fundamental inverter circuit using McMurray's H-Bridge topology

Full-bridge, inverter circuit first patented by William McMurray in 1965 for the General Electric Company [9].

This simplified version of the H-bridge utilizes four (4) semiconductor switches (shown here as mechanical switches for simplicity), two on each leg (diodes are placed across the terminals of each switch to prevent a short circuit condition in the event that all switches are in the closed position. Each end of the load is tied to one of the legs between two switches. Let us assume that the load is purely resistive and that it requires an AC waveform to operate. By closing switches SW1 and SW4 in Figure 22, a positive voltage, at the value of the DC source, is created from point *b* to *a*, which results in a current flowing through the load from point *a* to *b*. Now if we open switches SW1 and SW4 and close switches SW2 and SW3, a positive voltage, at the value of the DC source, is now created from point *a* to *b*, which causes the current to flow from point *b* to *a*. This results in a negative voltage and current seen at the load. Both conditions are illustrated in Figure 23.

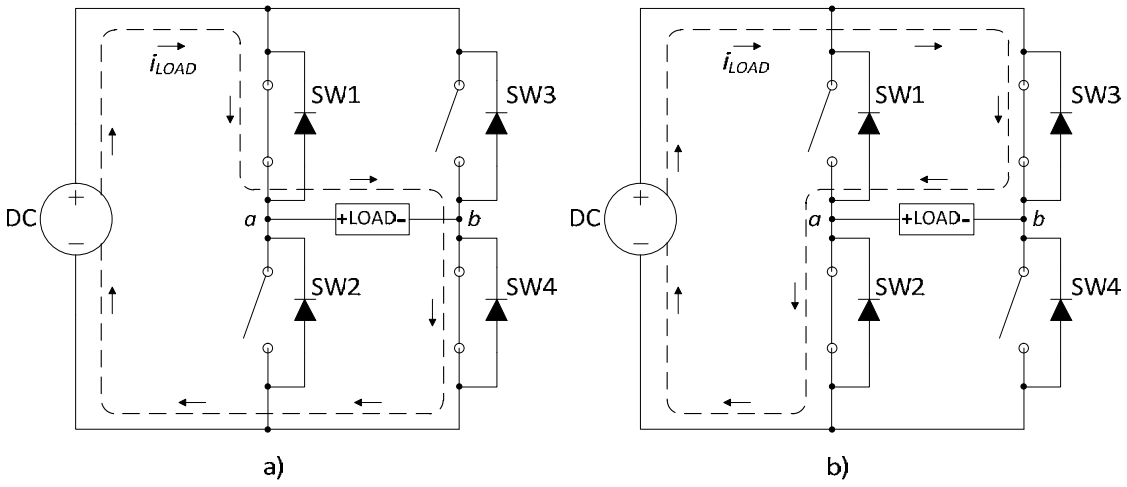


Figure 23 H-Bridge inverter a) positive current at load, b) negative current flow at load

By alternating this switching pattern every 0.00833 seconds, we will create an AC waveform at the load with a frequency of 60 Hz, as seen in Figure 24. Although this waveform is a square wave, it is nevertheless an AC waveform. Notice the absence of the waveforms of switches SW2 and SW4 as they only provide a path to ground, thus their respective voltages will be zero throughout the inversion process.

As discussed earlier, when dealing with waveform shaping, especially in utility interactive inverter design, care must be taken to minimize the THD of the output waveform. In the case of our basic inverter, the output we obtained was a square wave, much too different from the sinusoidal waveform we see at the utility. Using Fourier

analysis, it can be shown that a square wave is obtained through the summation of harmonic components of a sine wave. By utilizing this knowledge along with equation (25), let us calculate the %THD of the square wave we obtained from our basic inverter.

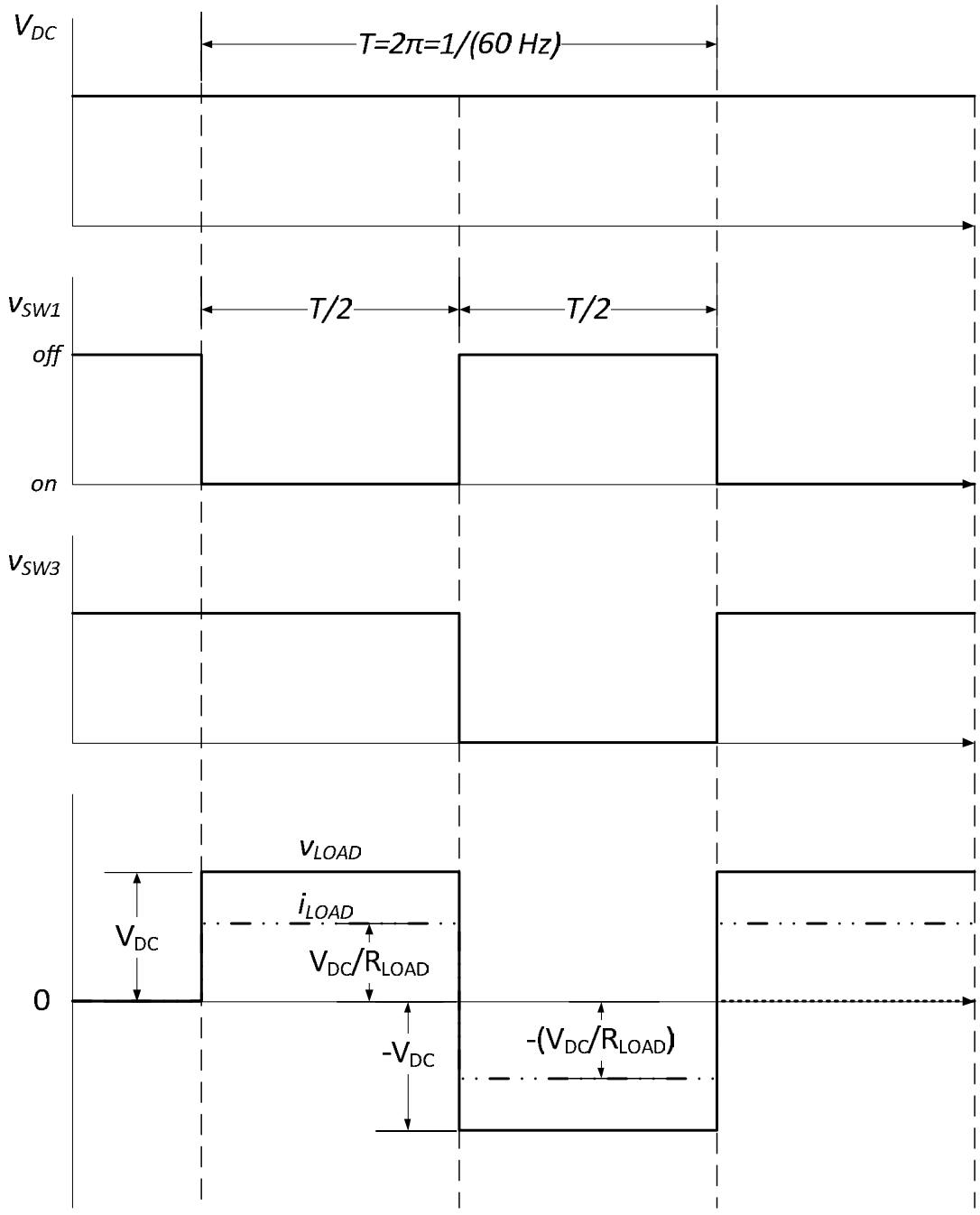


Figure 24 Voltage and Current waveforms of circuit in Figure 23

In Figure 24, we see that our output waveform has a fundamental frequency of 60 Hz. We can calculate the RMS value of the voltage using equation (18) as follows

$$(29) \quad V_{RMS} = \sqrt{\frac{1}{T}\int_0^T v^2 dt} = \sqrt{\frac{1}{\pi}\int_0^\pi {V_{DC}}^2 dt} = \sqrt{\frac{{V_{DC}}^2}{\pi}\int_0^\pi dt}$$

$$(29)\text{ cont.} \quad V_{RMS} = \sqrt{\frac{{V_{DC}}^2}{\pi}\pi} = \sqrt{{V_{DC}}^2} = V_{DC}$$

The RMS value of the voltage waveform's fundamental component can be found to be

$$(30) \quad V_1 = \frac{4V_{DC}}{\pi\sqrt{2}}$$

By plugging in equations (29) and (30) into the second form of equation (25), we obtain

$$(31) \quad \%THD = \frac{\sqrt{{V_{RMS}}^2 - {V_1}^2}}{V_1} \times 100 = \frac{\sqrt{{V_{DC}}^2 - \left(\frac{4V_{DC}}{\pi\sqrt{2}}\right)^2}}{\frac{4V_{DC}}{\pi\sqrt{2}}} \times 100$$

$$\%THD = \frac{\sqrt{{V_{DC}}^2\left(1 - \frac{8}{\pi^2}\right)}}{\frac{4V_{DC}}{\pi\sqrt{2}}} \times 100 = \frac{\pi\sqrt{2}\sqrt{\left(1 - \frac{8}{\pi^2}\right)}}{4} \times 100$$

$$\%THD = 48.34\%$$

As we can see from our result, and it is no surprise, that the total harmonic distortion in our output waveform is significantly high. The same result will be obtained if solving for the output current waveform i_{LOAD}. We must explore some different control techniques to hopefully generate a waveform which has an acceptable level of distortion.

Inverter Control Schemes – Single Phase

To continue with our basic inverter, let us try and minimize the THD for this circuit. Let us define a general square wave, as shown in Figure 25, with an arbitrary value, t_1, which directly affects the duty cycle of the inverter. The RMS value of this square wave can be

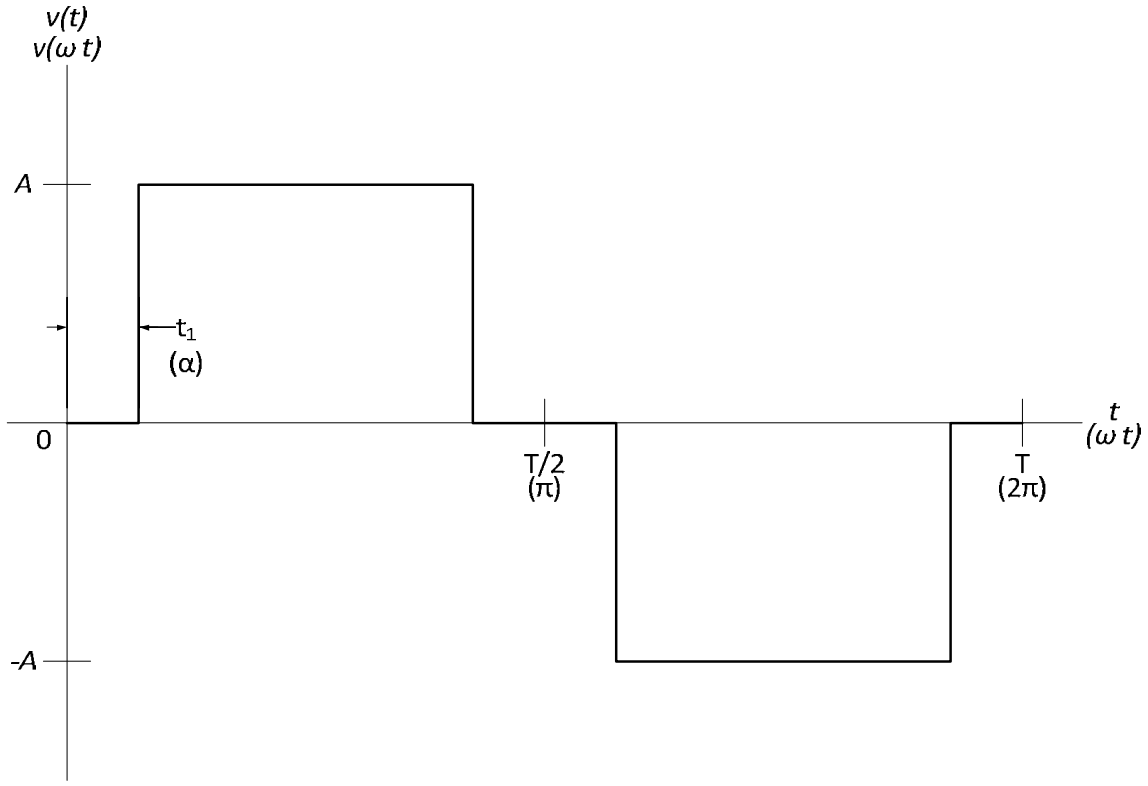


Figure 25 General square wave function with duty cycle variable t_1

found by using equation (32) below

$$(32) \quad V_{RMS} = \sqrt{\frac{1}{T}\int_0^T f^2 dt} = A\sqrt{\frac{1}{T}\left(\int_{t_1}^{\frac{T}{2}-t_1} dt + \int_{\frac{T}{2}+t_1}^{T-t_1} dt\right)}$$

$$= A\sqrt{\frac{1}{T}(T-4t_1)} = A\sqrt{1-\frac{4t_1}{T}}$$

Taking into account that $T = \frac{2\pi}{\omega}$ and $t_1 = \frac{\alpha}{\omega}$, and plugging into equation (32) we have

$$(33) \quad V_{RMS} = A\sqrt{1-\frac{4\left(\frac{\alpha}{\omega}\right)}{\frac{2\pi}{\omega}}} = A\sqrt{\frac{\pi-2\alpha}{\pi}}$$

The RMS value of the fundamental component of the square wave can be found using equation (24) and the laws of symmetry applicable to the Fourier series, shown in equation (22).

$$(34) \quad V_h = \frac{2}{\pi}\int_0^{\pi} f(t)\sin(h\omega t)\, d(\omega t)$$

$$= \frac{2A}{\pi}\int_0^{\pi} \sin(h\omega t)\, d(\omega t)$$

$$= \frac{2A}{\pi h}(-\cos(\omega t)|_{\omega t=0}^{\pi})$$

$$V_h = \frac{4A}{\pi h}\cos(\alpha) \quad h = 1,3,5 \ldots odd, \alpha = \omega t$$

To be able to use equation 34 in our attempt to minimize THD, we must obtain the RMS value of the first fundamental as shown below

$$(35) \quad V_{1,RMS} = \frac{4A}{\sqrt{2}\pi}\cos(\alpha)$$

We can now plug in equations (33) and (35) into equation (25) and obtain a general equation for the THD as shown below

$$(36) \quad THD_V = \frac{\sqrt{{V_{RMS}}^2 - {V_{1,RMS}}^2}}{V_{1,RMS}}$$

$$= \sqrt{\frac{\pi(\pi - 2\alpha)}{8\cos^2(\alpha)} - 1}$$

Now that we have a generalized equation for the THD, an attempt to minimize it is rather elementary and can be accomplished by setting its derivative to zero and obtaining

$$(37) \quad \tan(\alpha) = \frac{1}{\pi - 2\alpha}$$

Solving equation (37) for α, we obtain only one plausible solution of 0.45235 rad (23.22°), which is supposed to give us the minimum value of THD for a square wave. Plugging our result into equation (36) we obtain a %THD of 29.3%, an improvement of 40%. This method has significantly reduced the THD of the square wave, however, in order for us to be able to utilize an inverter in a utility interactive environment, we must limit our THD as much as possible. The important thing to note is to achieve, as much as possible, a sinusoidal current waveform. A pulse width modulated control scheme has shown to provide output waveforms close to sinusoidal form.

Pulse Width Modulation (PWM) is a very popular technique used in power electronics, mainly due to the fact that the harmonics in the current waveform are kept low as compared to other techniques, such as the square wave operation shown earlier. PWM involves the use of two signals, a *carrier* signal which operates at a switching frequency of f_s, and a *modulation* signal operating at the desired output frequency f_1. Usually a triangular waveform is utilized as the carrier, and f_s is usually in the range of a few hundred Hz to 20 kHz, and maybe higher depending on the type of semiconductor switches being used. The modulation, or control signal is a sine wave at 60 Hz in our case. These are illustrated in Figure 26.

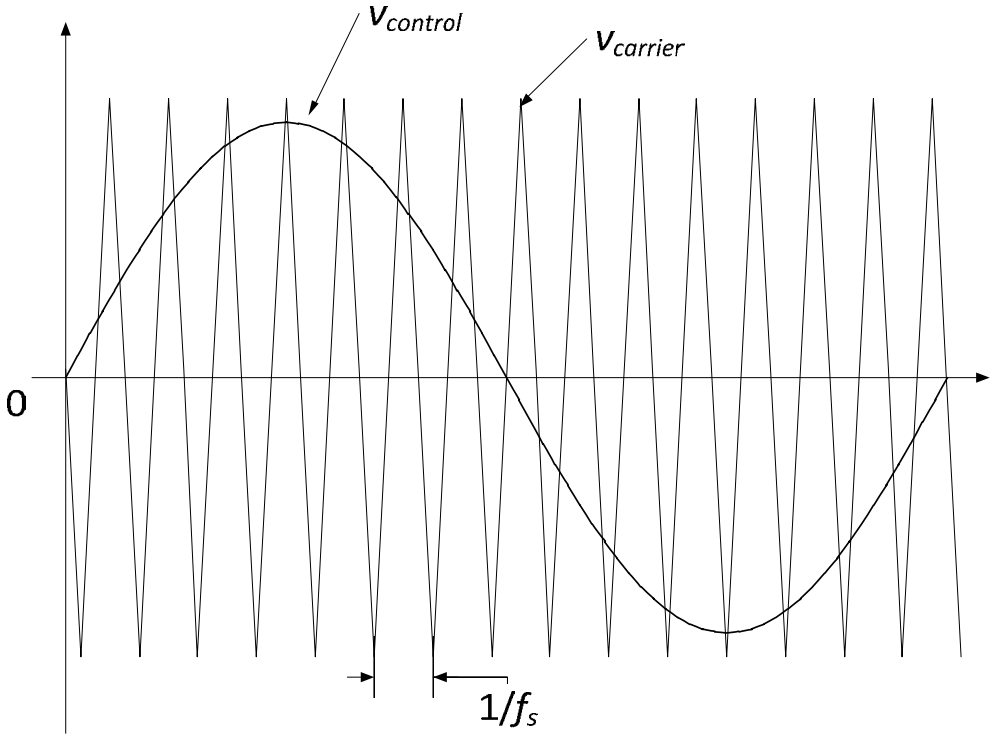


Figure 26 PWM with bipolar voltage switching, showing control and carrier signals

To control the switches shown in the circuit of Figure 22, the control signal, $v_{control}$, is compared to the carrier signal, $v_{carrier}$ and the output of the comparison is the logic signal applied to the semiconductor switches. The switching logic is as follows:

$v_{control} > v_{carrier}$, SW1 & SW4 are ON, SW2 & SW3 are OFF
$v_{control} < v_{carrier}$, SW1 & SW4 are OFF, SW2 & SW3 are ON

This results in the following voltage waveform at the load of Figure 22:

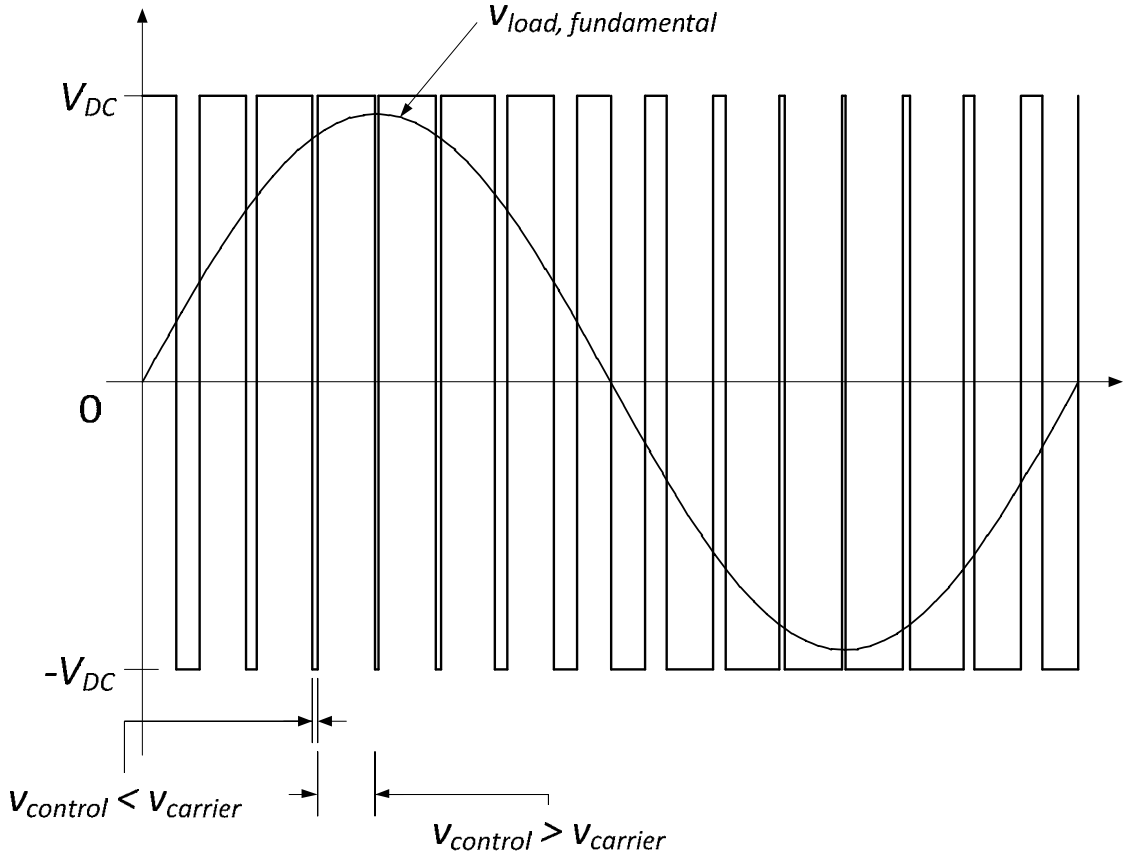


Figure 27 Bipolar PWM voltage waveform at the load of circuit in Figure 22

Let us also define the following ratios for reference

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{carrier}} \quad (38)$$

and

$$m_f = \frac{f_s}{f_1} \quad (39)$$

where m_a is the amplitude modulation ratio and m_f is the frequency modulation ratio. $\hat{V}_{control}$ is the peak amplitude of the control (modulation) signal and $\hat{V}_{carrier}$ is the amplitude of the triangular carrier signal and is generally kept constant.

This type of PWM is termed bipolar switching because the voltage swing of the waveform alternates from positive to negative, hence the word bipolar. Due to the fact that the voltage change in a bipolar PWM switching scheme varies so drastically with respect to time, the current on the DC side of the circuit develops significant ripples. This can be mitigated, however, using a unipolar PWM switching scheme. The term unipolar implies that the PWM control signal for each switching state does not alternate in sign, however, switches from positive to zero and negative to zero, as shown in Figures 28 and 29.

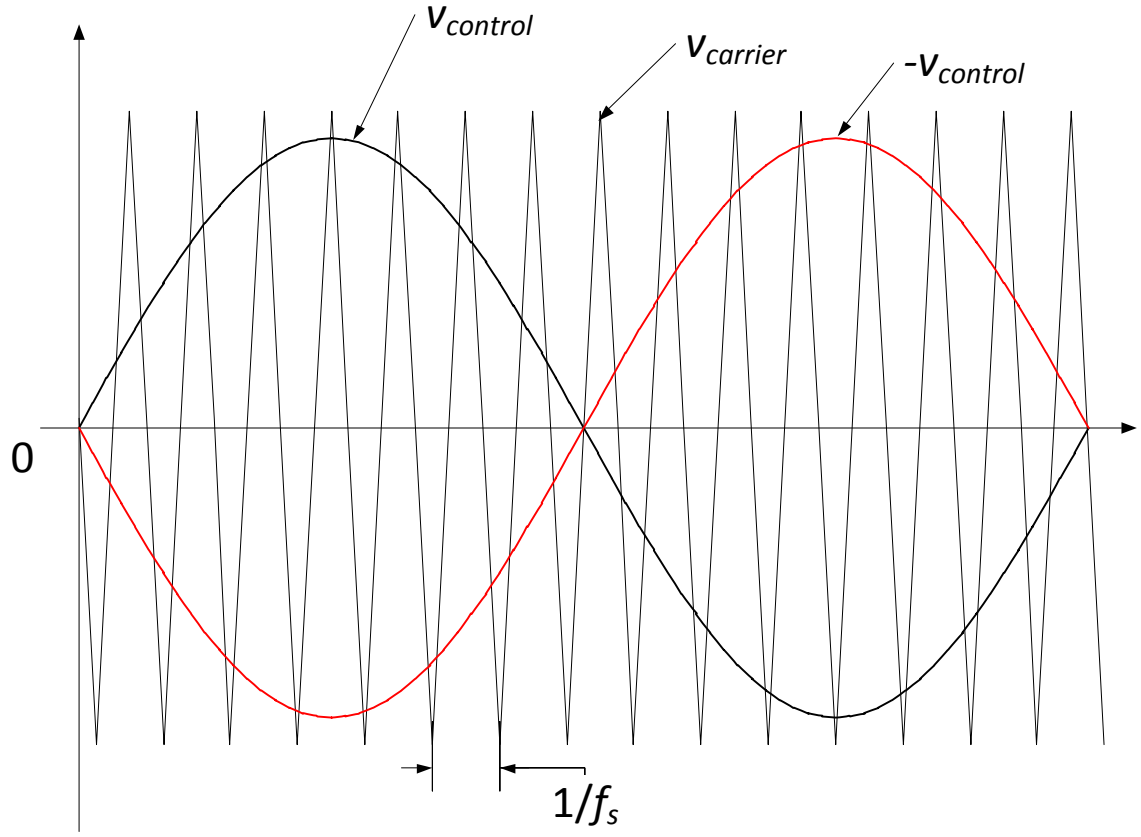


Figure 28 PWM with unipolar switching, showing control and carrier signals

The unipolar PWM switching scheme is accomplished by making an additional comparison of the negative of the control signal to the carrier signal. Also, each pair of switches is controlled independently, rather than just taking the complement of comparison and feeding into the opposite set of switches. The control logic for operating the switches are

$$v_{control} > v_{carrier}, \text{ SW1 ON \& SW2 OFF}$$
$$v_{control} < v_{carrier}, \text{ SW1 OFF \& SW2 ON}$$
$$(-v_{control}) > v_{carrier}, \text{ SW3 ON \& SW4 OFF}$$
$$(-v_{control}) < v_{carrier}, \text{ SW3 OFF \& SW4 ON}$$

By analyzing Figure 28, we can conclude that four possible states exist in unipolar PWM switching. They are described by

$$v_{control} > v_{carrier} \ \& \ (-v_{control}) > v_{carrier}, \text{ SW1 ON-SW2 OFF \& SW3 ON-SW4 OFF}$$
$$v_{control} < v_{carrier} \ \& \ (-v_{control}) < v_{carrier}, \text{ SW1 OFF-SW2 ON \& SW3 OFF-SW4 ON}$$
$$v_{control} > v_{carrier} \ \& \ (-v_{control}) < v_{carrier}, \text{ SW1 ON-SW2 OFF \& SW3 OFF-SW4 ON}$$
$$(-v_{control}) < v_{carrier} \ \& \ (-v_{control}) > v_{carrier}, \text{ SW1 OF-SW2 ON \& SW3 ON-SW4 OFF}$$

and thus, the resultant voltage waveform seen at the load is illustrated in Figure 29.

One of the advantages of a unipolar switching scheme is the reduced ripple on the DC side current as stated before. Another advantage is that the number of pulses generated has doubled for the same switching frequency as used in bipolar switching. This, in effect, is the same as doubling the sampling frequency of an AD converter, which consequently results in a much more precise output waveform. As such, the output current waveform will contain fewer harmonics.

Inverter Control Schemes – Three Phase

The inverter control methods described so far also apply in three phase inverter systems, like the general one shown in Figure 30. Obviously more components are required in a three phase inverter system, along with more control signals. If we wish to operate our three phase inverter utilizing a square wave scheme, at least three control signals are required (we are not taking into account the inversion of a signal to designate the complement state, i.e. switch 2's control signal is the complement of switch 1's control signal). In addition, the pulses for each leg must be timed so that phase difference between each phase is 120°. Also, all switches operate at a duty ratio of 50%, which means that at any instant of time, three switches are on. The voltage waveforms are shown in Figure 31.

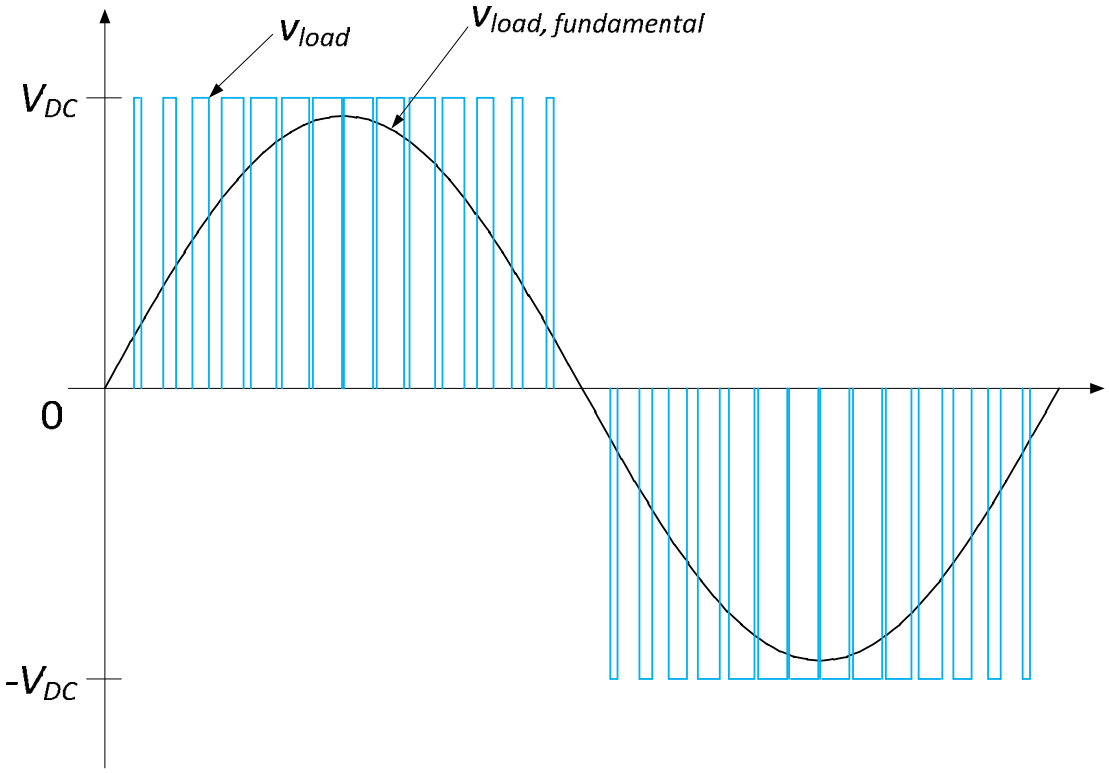


Figure 29 Unipolar PWM voltage waveform at the load of circuit in Figure 22

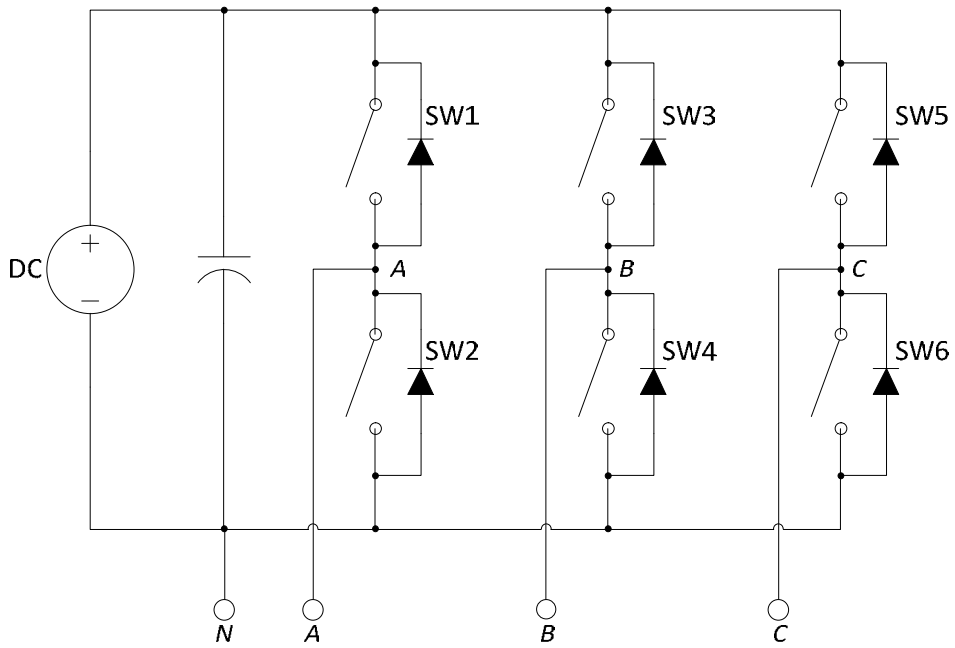


Figure 30 General 3-phase inverter circuit

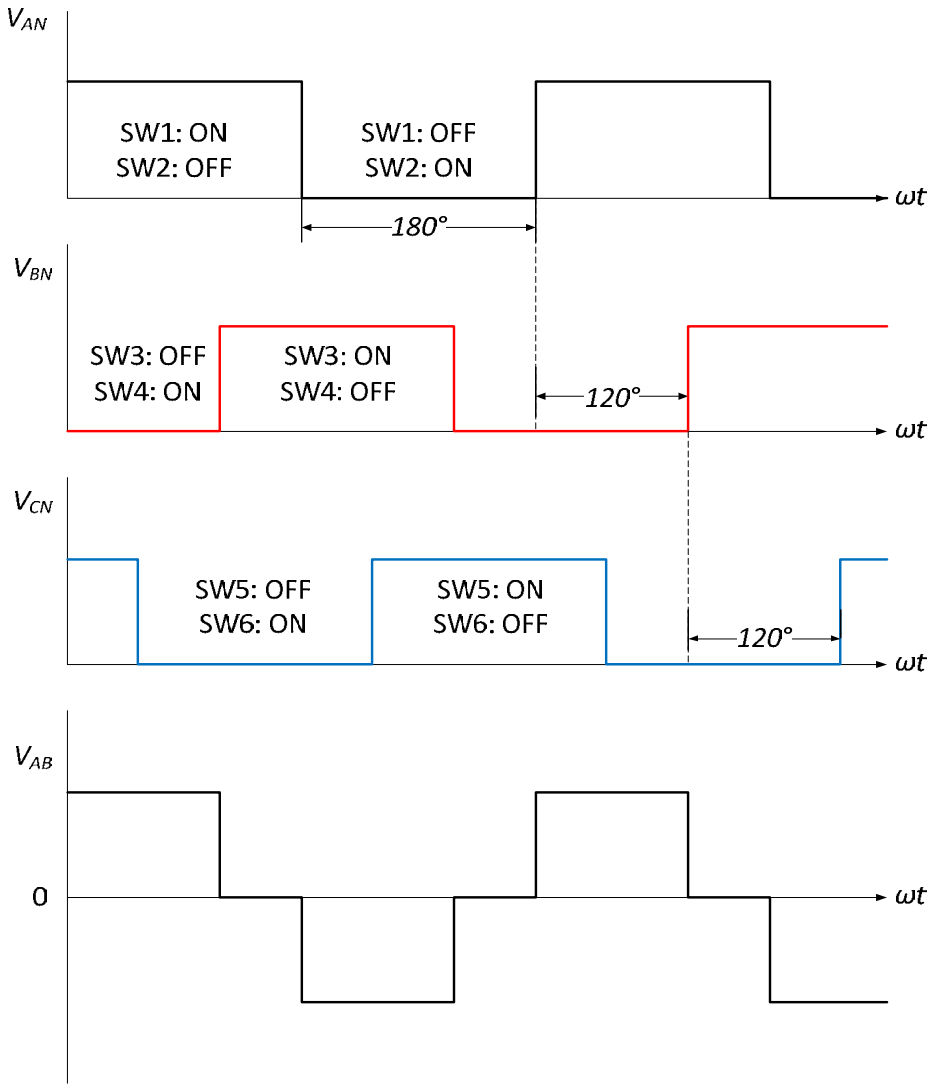


Figure 31 Three-phase square wave inverter voltage waveforms (V_{BC} and V_{CA} not shown)

We can see that the operation is exactly the same as in the single phase inverter, with the only difference being the additional switching leg. It should be noted that in the square wave mode of operation, the inverter itself cannot control the magnitude of the output AC voltages. Therefore, it is essential that the DC input be controlled in order to control the output in magnitude.

From Fourier analysis, we calculate the following fundamental –frequency line-to-line RMS voltage component of the output operating in square-wave mode to be

$$(40) \quad V_{LL_1} = \frac{\sqrt{3}}{\sqrt{2}}\frac{4}{\pi}\frac{V_{DC}}{2} = \frac{\sqrt{6}}{\pi}V_{DC} \cong 0.7797V_{DC}$$

The line-to-line output voltage waveform does not depend on the load and contains harmonics ($6n \pm 1$; n = 1, 2, …) whose amplitudes decrease inversely proportional to their harmonic order shown by

$$V_{LL_h} = \frac{0.7797}{h} V_{DC} \quad (41)$$

where

$$h = 6n \pm 1 \; (n = 1, 2, 3, \ldots)$$

In addition to the square wave control scheme, we can also implement a three-phase PWM control scheme to better reduce the harmonics, as shown in Figure 32.

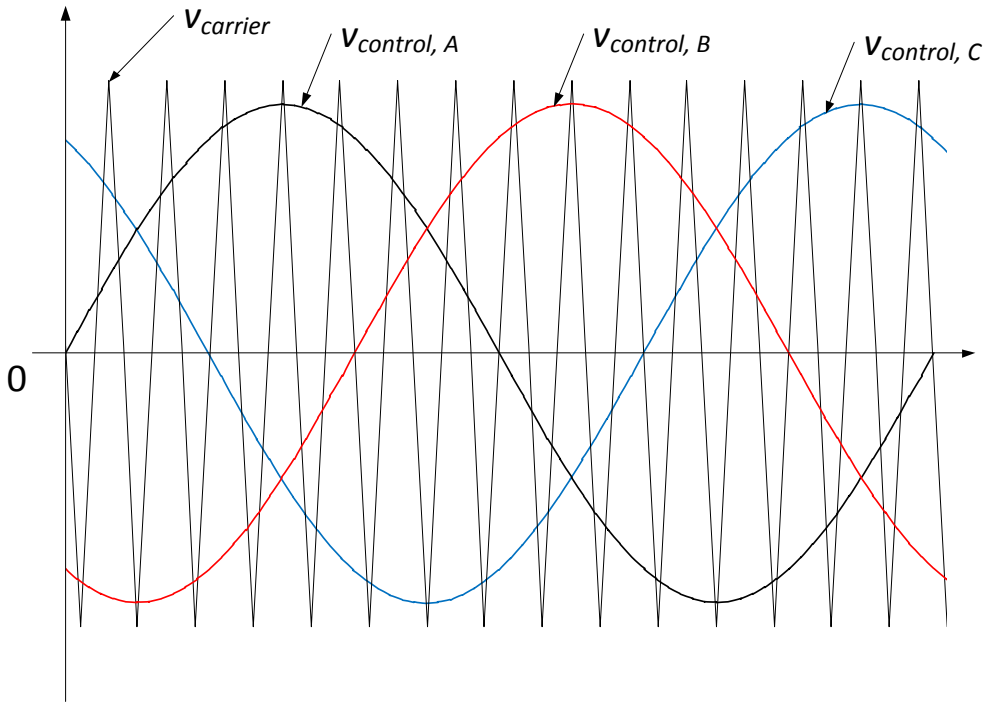


Figure 32 Three-phase control and carrier waveforms for PWM

This is achieved much the same as it is implemented in a single phase system, however, we utilize 3 sinusoidal control voltages that are 120° apart from one another to obtain a balanced three phase output. This PWM scheme will be a unipolar switching scheme as we are comparing three different control waveforms. As in the square wave mode of

operation, we will need at least three control signals to operate the semiconductor switches. The control and output waveforms are shown in Figure 33.

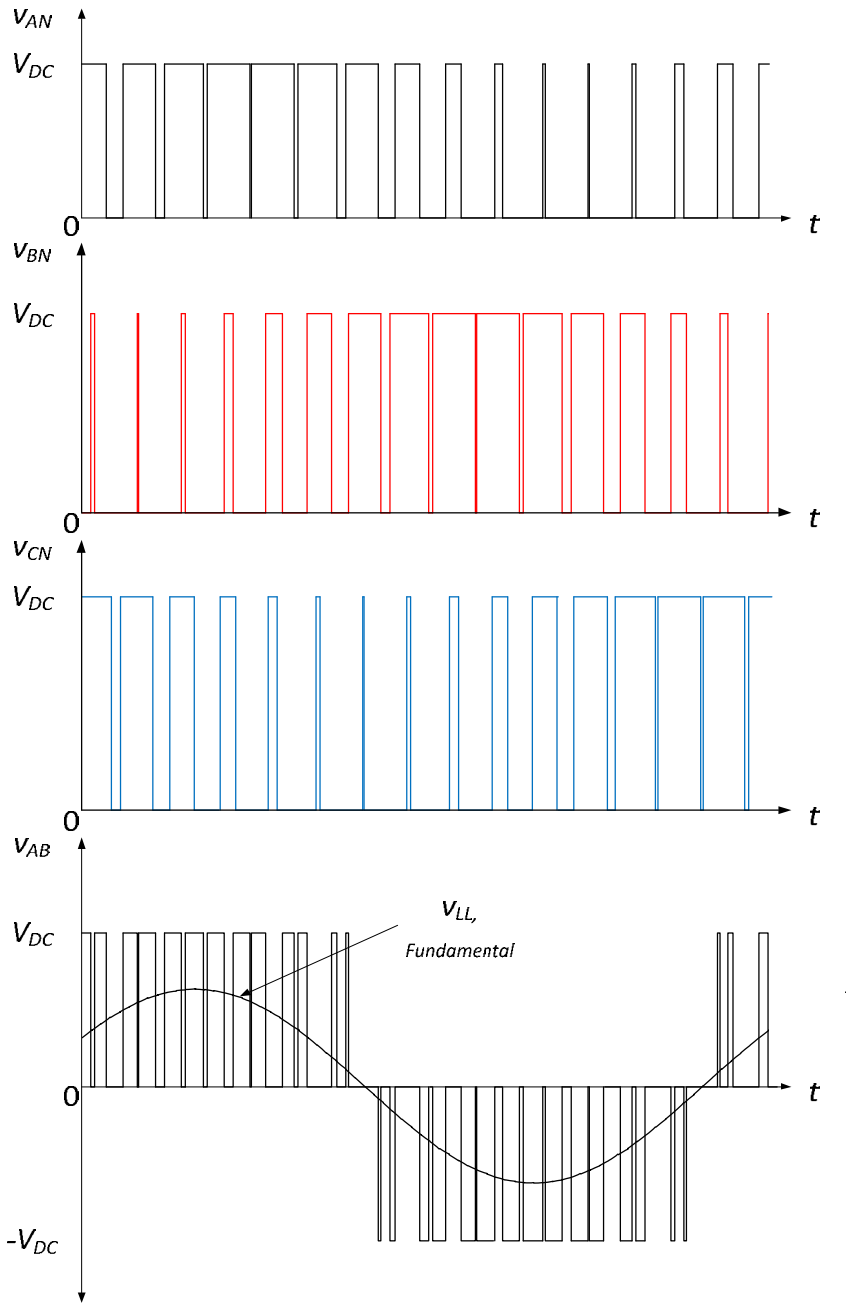


Figure 33 Three-phase PWM inverter voltage waveforms (V_{BC} and V_{CA} not shown)

The following logic applies when employing a three-phase PWM and was illustrated in Figure 33:

$v_{control,\,A} > v_{carrier}$, SW1 ON & SW2 OFF
$v_{control,\,A} < v_{carrier}$, SW1 OFF & SW2 ON
$v_{control,\,B} > v_{carrier}$, SW3 ON & SW4 OFF
$v_{control,\,B} < v_{carrier}$, SW3 OFF & SW4 ON
$v_{control,\,C} > v_{carrier}$, SW5 ON & SW6 OFF
$v_{control,\,C,} < v_{carrier}$, SW5 OFF & SW6 ON

It should be noted that if m_f is chosen to be odd and a multiple of 3, the phase difference between the m_f harmonic in the three phases will be equivalent to zero, thus eliminating line-to-line even and dominant harmonics. This applies to low values of m_f ($m_f \leq 21$). For large values of m_f ($m_f > 21$), an asynchronous PWM should be employed where the frequency of the triangular carrier signal is kept constant and the frequency of the control signal varies, resulting in non-integer values of m_f. However, subharmonics at zero or close to zero frequency will cause large currents, and therefore, this method is not recommended for loads such as AC motors. During over-modulation, ($m_a > 1.0$), regardless of the value of m_f, a synchronized PWM with m_f designated to be a multiple of 3 should be employed.

There are additional control schemes and strategies employed in the design of inverters; however, for the purposes of this project, we will conclude the discussion here. The reader may wish to research additional texts and technical documentation regarding proposals of newer, more efficient control techniques. We will however, turn now to some basic inverter topologies and concentrate on those more prevalent in utility interactive, or grid-tied inverters.

Inverter Topologies

There are three main topologies used in utility interactive inverters: the low frequency transformer topology, high frequency transformer topology and the transformerless topology. There obviously exists variations on each of the topologies just listed, however, we will only focus on these general topologies to provide an adequate understanding of the operating characteristics of the utility interactive inverter. Most of the inverter topologies used today are based on McMurray's H-Bridge topology. Let us begin with the low frequency transformer topology as shown in Figure 34.

As we can see from the figure, this topology's name is derived from the fact that a low frequency transformer (rated at the grid's line frequency) is directly connected to the grid. Two filters are placed in the circuit, one on the DC side and the other just after the inversion process and ahead of the transformer. A DC boost stage without a transformer

is utilized in this topology, if required [10]. The advantages of the low frequency transformer topology are its robustness and electrical isolation from the grid. However, due to the

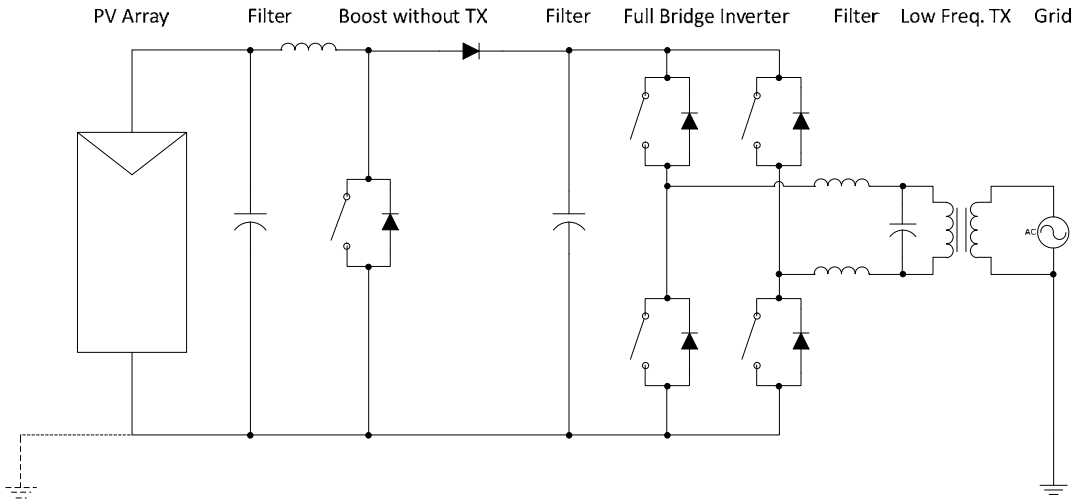


Figure 34 Low frequency transformer topology

fact that a low frequency transformer is being utilized, the overall weight of the inverter is increased significantly along with its volume.

The next evolution in inverter topologies was the high frequency transformer topology shown in Figure 35.

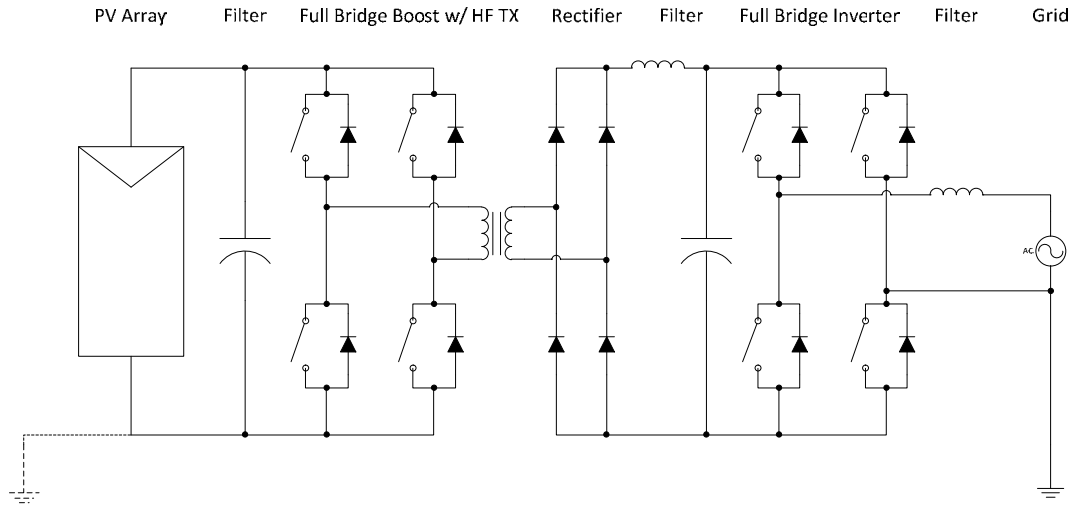


Figure 35 High frequency transformer topology with boosting inverter

This topology contains three stages of conversion. The first stage converts and boosts the DC input from the photovoltaic source into a high frequency AC signal. This high frequency AC signal is then fed into a high frequency transformer. The secondary of the transformer serves as the input to a rectifier circuit which transforms the high frequency AC back to DC. At this point, the signal undergoes a final inversion process, is filtered, and fed into the grid. The low weight and small size of high frequency transformers provides a great weight and size reduction compared to inverters using topologies with low frequency transformers. As with the previous topology, electrical isolation is achieved using the high frequency transformer. However, the drawbacks to this topology are the reduced efficiency due to the high switching losses, the increased complexity of the topology and, most importantly, an increased cost due to the higher number of parts used.

The current trend in inverter topology design is the transformerless topology as shown in Figure 36.

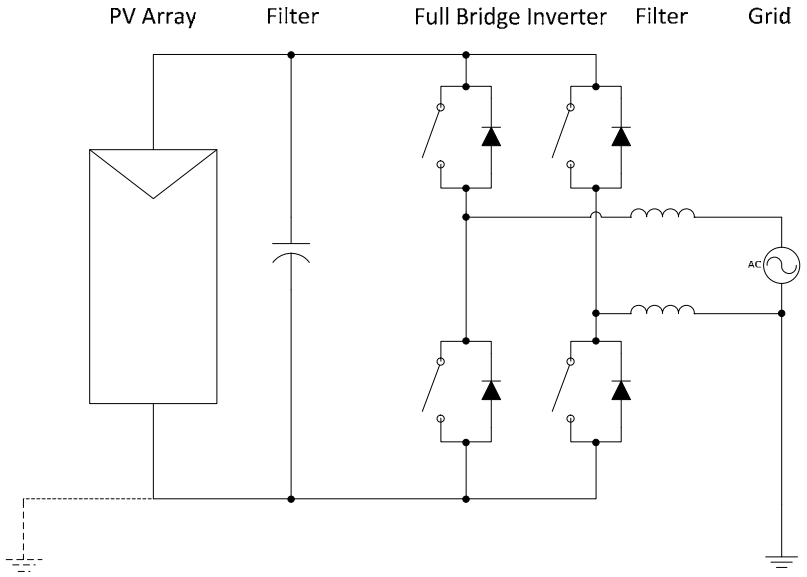


Figure 36 Transformerless inverter topology

The transformerless topology generally involves only two stages, a boost stage, followed by the inversion stage and is similar to the inverter discussed earlier. The signal is then filtered prior to being fed into the grid. This topology provides reduced size, reduced cost, reduced weight and higher efficiency compared to the prior two topologies utilizing transformers. However, the one major drawback is its lack of electrical isolation. Many inverter manufacturers have already developed numerous inverter topologies based on the transformerless model. Reference [10] outlines and discusses a variety of implementations based on this type of topology.

Design Considerations in Accordance with IEEE 1547 –*Standard for Interconnecting Distributed Resources with Electric Power Systems*

The general characteristics of the inverter and its operation have been explained. We are now ready to discuss pertinent and practical topics related to utility interactive inverters used in photovoltaic applications.

The Institute of Electrical and Electronics Engineers (IEEE) has written a standard that deals with the presence of distributed systems, such as photovoltaic systems, in the electrical power grid. IEEE 1547 outlines the minimum operating requirements of an inverter to ensure safety amongst the public and utility workers. Underwriters Laboratories (UL) has adopted this standard and harmonized it with its own respective standard to ensure electrical safety. It is essential that engineers, who design inverters for utility interactive applications, comply with these requirements. Keep in mind that the IEEE standard is relevant in the United States and other standards exist for different locales, such as Europe and Asia, however, we will be concentrating solely on the IEEE standard requirements in the upcoming analysis.

IEEE 1547 requires that certain conditions be met during the operation of a utility interactive, or grid-tied, inverter. These conditions have been set to ensure the safety of utility workers and the public alike. The first major requirement in our discussion is in regard to the voltage output of the inverter and its deviation from the utility supplied voltage. The inverter must disconnect from the utility line within certain prescribed time intervals in the event that the output voltage of the inverter deviates from the utility supply by a certain percentage. This requirement is outline in Table 4.

Voltage Range (%)	**Disconnection Time (s)**
$V < 50$	0.16
$50 \leq V \leq 88$	2.00
$110 \leq V \leq 120$	1.00
$V \geq 120$	0.16

Table 4 IEEE 1547 Disconnection Requirements for Voltage Deviation

It can be seen that the safe operating range is $88 < V < 110$, and during extreme deviations ($V < 50$, $V \geq 120$) the inverter must disconnect within 10 cycles of operation ($T = 1/f = 1/60\ Hz = 0.0167$). To comply with this requirement, voltage sensing must be employed within the inverter control scheme to detect these variations and disconnect itself from the utility if needed.

The other major requirement is frequency deviations in the inverter's output signal. A major difference between the inverter frequency and that of the utility will cause havoc among protective devices in the utility and subject loads to unwanted frequencies that can cause permanent damage. The frequency deviation requirement is summarized in Table 5.

Frequency Range (Hz)	**Disconnection Time (s)**
$f < 59.3$ or $f > 60.5$	0.16

Table 5 IEEE 1547 Disconnection Requirement for Frequency Deviation

The standard allows for the adjustment of the lower limit of the frequency provided that the nominal power of the system is less than 30 kW. Again we see a disconnection requirement of 10 cycles.

The next requirement involves minimization of DC current injection into the grid and applies mainly to the transformerless inverter since conventional inverter systems utilize transformers, providing galvanic isolation and thus minimizing the injected DC current. DC current fed into the utility can saturate distribution transformers, which leads to overheating and tripping of the overcurrent protection devices. The standard requires that the DC current component in the output of the inverter must be less than 0.5% of the rated RMS output current. This should be done using harmonic analysis via Fast Fourier Transform (FFT) to measure the DC component of the current. It should also be noted that the standard does not explicitly state a maximum trip time condition.

Another important requirement of IEEE 1547 is the minimization of current harmonics. Low distortion levels ensure that no adverse effects are caused to other equipment connected to the utility system. Table 6 summarizes the maximum allowable current harmonics in the output of an inverter.

Individual harmonic order (odd)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	Total Harmonic Distortion (THD)
%	4.0	2.0	1.5	0.6	0.3	5.0

Table 6 IEEE 1547 Maximum Allowable Current Harmonics

The most technically challenging requirement set forth by IEEE 1547 is what is called the Anti-Islanding requirement. Islanding, in terms of grid connected photovoltaic systems, takes place when the inverter fails to disconnect from the grid within a period of time after the grid has tripped. For example, if a local distribution transformer is overloaded,

and the pole top fuses blow, the grid is now disconnected from the homes connected to that transformer. If one of those connected houses utilizes a photovoltaic system and it fails to disconnect from the grid, it would be generating a voltage at the open conductors. Utility line workers sent to repair the problem will not know a voltage is present at those conductors and it will pose a serious safety hazard. Also, in the event that the protective devices are closed, an out of phase source from the inverter will cause damage to the line, the associated equipment and may injure the utility line workers. As such, in order to avoid these serious consequences, IEEE 1547 requires that an inverter involved in an islanding scenario disconnect from the grid within 2 seconds.

A testing condition is required by IEEE 1547 as is shown in Figure 37.

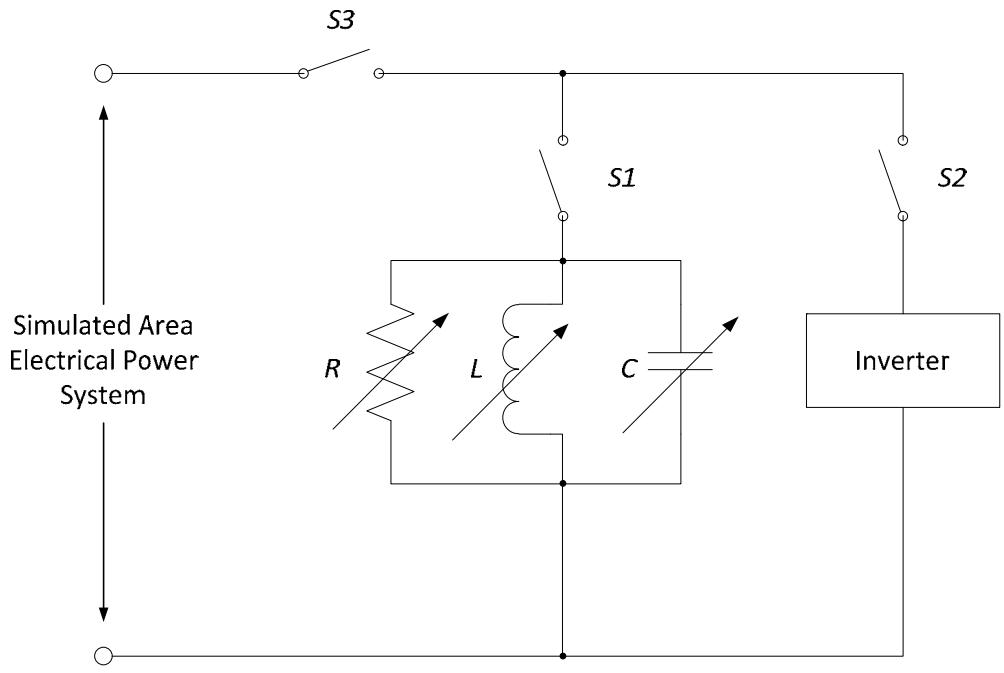


Figure 37 IEEE 1547 Anti-islanding test setup

The test conditions require that an adjustable RLC load be connected in parallel between the inverter and grid. The resonant LC circuit should be adjusted to resonate at the rated grid frequency f and to have a quality factor of $Q_f = 1$, or in other words, the reactive power generated by C should equal the reactive power absorbed by L and should equal the power dissipated in R at the nominal power P and rated grid voltage V. As such, the values for the local RLC load shown in Figure 37 can be calculated as

$$(42) \quad R = \frac{V^2}{P}, L = \frac{V^2}{2\pi f P Q_f}, C = \frac{P Q_f}{2\pi f V^2}$$

The parameters in (42) should be fine-tuned until the grid current through *S3* is lower than 2% of the rated value in steady-state. In this condition, *S3* should open, and the time it takes for it to open should be measured and required to be less than 2 seconds. In three-phase inverters (grounded neutral Y), each phase should be tested with respect to the neutral conductor individually. For three-wire three-phase systems (ungrounded Delta), the RLC load should be connected between the phases.

IEEE 1547 also outlines a requirement for reconnection, in the event that one of the previously mentioned requirements caused the inverter to disconnect from the utility. This requirement states that an inverter cannot reconnect to the grid unless the voltage V is in the range of $88 < V < 110$ (%) of the rated grid voltage and the frequency f is in the range $59.3 < f < 60.5$ (Hz) of the rated grid frequency. This ensures the safety of utility personnel and the public from dangerous reconnection scenarios.

These requirements must be accounted for during the inverter design process. We will discuss the methodology in designing for and dealing with these very important requirements in the following sections.

UTILITY SYNCHRONIZATION FOR SINGLE PHASE INVERTERS

Introduction

Utility synchronization is an essential aspect of all utility interactive inverters. Synchronization ensures that the inverter output works in unison with the utility power and mitigates the passage of harmful harmonics and DC components into the grid. Due to the unpredictable nature of utility power (i.e. faults, constantly changing loads, etc.), the inverter must be able to monitor and respond to any changes in the utility variables at a very fast speed. Several synchronization methods will be discussed, from the use of the impractical Fourier based adaptive filters to the more robust, practical and accurate phase-locked and frequency-locked loop methods.

The Fourier Adaptive Filter

To begin this discussion on the Fourier adaptive filter, let us recall equations (21), (22), (23) and (24) and only rewrite the integration limits and terms in equations (23) and (24) for a more general description.

$$(21) \quad f(t) = F_0 + \sum_{h=1}^{\infty} f_h(t) = \frac{1}{2}a_0 + \sum_{h=1}^{\infty}\{a_h \cos(h\omega t) + b_h \sin(h\omega t)\}$$

$$(22) \quad F_0 = \frac{1}{2}a_0 = \frac{1}{2\pi}\int_0^{2\pi} f(t)d(\omega t) = \frac{1}{T}\int_0^{T} f(t)dt$$

$$(43) \quad a_h = 2\frac{1}{T}\int_0^{T} f(t)\cos(h\omega t)\,dt = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\theta)\cos(h\theta)\,d(\theta)$$

$$(44) \quad b_h = 2\frac{1}{T}\int_0^{T} f(t)\sin(h\omega t)\,dt = \frac{1}{\pi}\int_{-\pi}^{\pi} f(\theta)\sin(h\theta)\,d(\theta)$$

By analyzing the equations above, we can see that they can be used to implement a selective band-pass filter by multiplying an input signal, *v*, by the sine and cosine basic functions at the desired frequency. Assuming the utility frequency is a constant and well known magnitude, the order of the harmonic to be extracted at the output of this proposed band-pass filter, *v'*, is selected by setting the value of the parameter *h*. This proposed adaptive band-pass filter is illustrated in Figure 38.

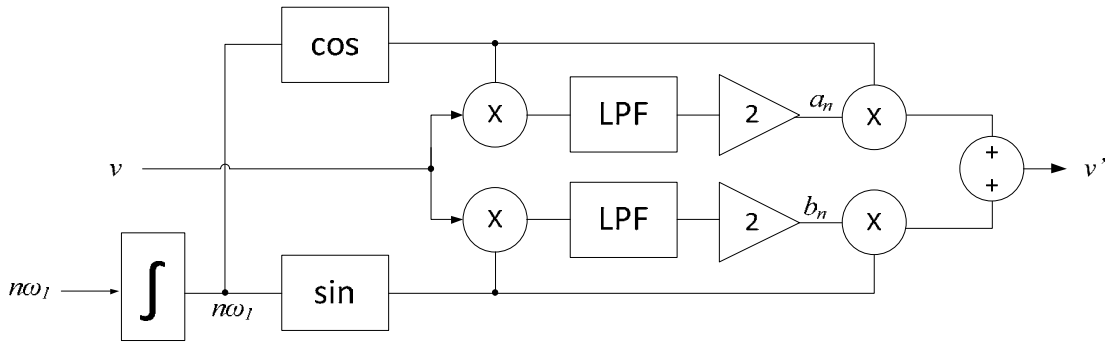


Figure 38 Adaptive filter based on Fourier series decomposition

As we can see, the mean value of the signals resulting from multiplying *v* by the sine and cosine functions is obtained by using a low-pass filter (LPF). The cut-off frequency of this LPF is a function of the lowest frequency component of the input signal, which under normal operating conditions, matches the fundamental frequency component ω_1 (f = 60 Hz). Sufficed to say, ω_1 is the variable of interest when designing inverter control systems for utility synchronization, and thus, we shall set h = 1 in the sine and cosine functions of filter shown in Figure 38. As a result, the lowest frequency component at the input of the LPF will be at $2\omega_1$(f = 120 Hz). This implies that the cut-off frequency of the LPF should be at least one decade lower than $2\omega_1$, at 12 Hz, which denotes a very slow dynamic response of the system. In addition, this cut-off frequency should be even lower if either subharmonics or DC components are present in the input signal, which could very well be the case in utility sources. Also, this method of synchronization would be impractical due to the fact that in a real world situation, we cannot assume that the utility frequency is a constant and well known magnitude.

Let us define equations (43) and (44) in terms of Euler's identities of the sine and cosine functions shown as

$$\cos(h\omega t) = \frac{e^{jh\omega t} + e^{-jh\omega t}}{2} \tag{45}$$

$$\sin(h\omega t) = \frac{e^{jh\omega t} - e^{-jh\omega t}}{2j} \tag{46}$$

By plugging in equations (45) and (46) into equations (43) and (44), and rearranging the resulting range of the summations, we end up with the compact complex form of the Fourier series as shown below in equation (47), in which both positive and negative frequencies are considered.

$$(47)\quad f(t) = a_0 + \sum_{h=1}^{\infty} c_h e^{jh\omega t} + \sum_{h=1}^{\infty} c_h e^{-jh\omega t}$$
$$= \sum_{h=0}^{\infty} c_h e^{jh\omega t} + \sum_{h=-1}^{-\infty} c_h e^{jh\omega t}$$
$$= \sum_{h=-\infty}^{\infty} c_h e^{jh\omega t}$$

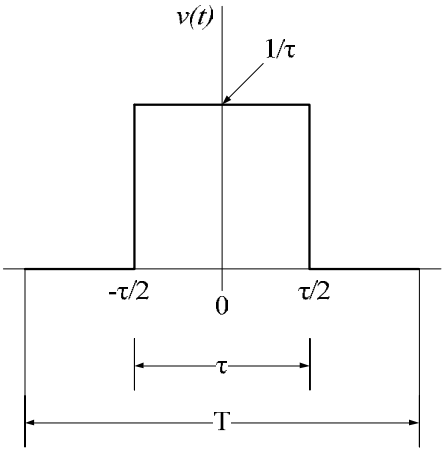
where

$$(48)\quad c_h = \frac{1}{2}(a_h - jb_h) = \frac{1}{T}\int_0^T f(t)\, e^{-jh\omega t} dt$$

Equation (47) provides a great introduction to the concept of the Discrete Fourier Transform and its use in utility synchronization.

The Discrete Fourier Adaptive Filter

To introduce the concept of the discrete Fourier transform, let us consider a pulse function which repeats every time period *T* and defined by the following expressions. These "train" of pulses will be processed using equation (48).



$$(49)\quad v(t)\begin{cases} 0, & -T \le t < -\frac{\tau}{2} \\ 1/\tau, & -\frac{\tau}{2} \le t \le \frac{\tau}{2} \\ 0, & \frac{\tau}{2} < t \le T \end{cases}$$

The complex coefficients of the Fourier series of the above waveform are calculated by solving the integral in equation 48. If we gradually made the period *T* longer while keeping the pulse duration, τ, constant, we can see that the complex coefficients calculated by equation 48 become smaller each time since the integral is being divided by *T*. In fact, as *T* approaches infinity, the signal *v(t)* becomes aperiodic and all the

coefficients calculated by equation (48) are equal to zero. Since the signal is now aperiodic, we can apply the principal of time/frequency duality by removing the period *T* in equation (48) and rewriting equation (47) as follows:

$$V(\omega) = \mathcal{F}[v(t)] = \int_{-\infty}^{\infty} v(t)e^{-j\omega t} \quad (50)$$

Equation 50 is known as the Fourier transform, which transforms a function in the time domain, periodic or aperiodic, into its dual in the frequency domain, provided that the integral exists. However, equation (50) must be able to be utilized by a digital signal processor; therefore, the integral in equation is calculated by a summation of a finite number of equally spaced samples in time. This is defined as

$$v[k] = v(t)\delta(t - kT_s) \quad \text{with} \quad k = 0, 1, \dots, N-1 \quad (51)$$

where $\delta(x)$ is the unit impulse function, T_s is the sampling period and *N* is the number of samples to be processed. The product NT_S provides the duration of the repetition pattern of the input signal and usually matches *T*, the period of the fundamental frequency component. Therefore, from equations (50) and (51) we can a define the discrete Fourier Transform (DFT) as

$$V[n] = \sum_{k=0}^{N-1} v[k] \cdot e^{-j2\pi\frac{k}{N}n} \quad \text{with} \quad n = 0, 1, \dots., N-1 \quad (52)$$

We can also define the inverse discrete Fourier Transform (IDFT) as

$$v[k] = \frac{1}{N}\sum_{n=0}^{N-1} V[n]e^{j2\pi\frac{n}{N}k} \quad (53)$$

As we can see by equation (52), the DFT algorithm requires N^2 complex multiplications and $N^2 - N$ complex additions. The calculation of the DFT algorithm for each sampling period is a great burden on the inverter's digital controller, despite the fact that only a single frequency component of the utility voltage is computed. As such, a recursive formulation of the DFT is usually used to reduce the computational burden on the microcontroller.

In the recursive algorithm, the *n*th frequency component of the input signal at the [k_S] instant is calculated from the value of the input signal at the [k_S] instant and the value of the *n*th frequency component at the [k_S-1] instant. To better explain this process, the DFT

algorithm is computed at the [k_S-1] and [k_S] instants in order to extract the *n*th harmonic of the input signal:

$$(54) \quad V[n]|_{k_{S-1}} = \sum_{k=k_S-N}^{k_S-1} v[k]e^{-j2\pi\frac{k}{N}n}$$

$$(55) \quad V[n]|_{k_S} = \sum_{k=k_S-N+1}^{k_S} v[k]e^{-j2\pi\frac{k}{N}n}$$

Subtracting equation (54) from (55) gives

$$(56) \quad V[n]|_{k_S} = V[n]|_{k_{S-1}} + v[k_S]e^{-j2\pi\frac{k_S}{N}n} - v[k_S - N]e^{-j2\pi\frac{k_S-N}{N}n}$$

Since $e^{-j2\pi\frac{k_S-N}{N}n} = e^{-j2\pi\frac{k_S}{N}n}$, the recursive discrete Fourier Transform (RDFT) algorithm can be formulated as

$$(57) \quad V[n]|_{k_S} = V[n]|_{k_{S-1}} + (v[k_S] - v[k_S - N])e^{-j2\pi\frac{k_S}{N}n}$$

Keep in mind that the discrete Fourier transforms presented so far are based on the complex form of the Fourier series shown by equation (47), which includes positive and negative frequencies. Taking into account that the complex values resulting from the Fourier transform are symmetric with respect to the zero frequency with half the amplitude of the corresponding *n*th harmonic, such an *n*th harmonic can be reconstructed in the time domain by

$$(58) \quad v[k] = \frac{2}{N}V[n]e^{j2\pi\frac{n}{N}k}$$

As a result, the RDFT algorithm can be implemented in a discrete adaptive band-pass filter to extract the *n*th frequency component of the input signal, as shown in Figure 39.

However, please be aware that as in all discrete Fourier analysis, RDFT gives rise to errors in amplitude and phase-angle estimation when NT_S does not match the fundamental frequency input signal. This inherent problem is one of the reasons why Fourier techniques are not the best choice in utility synchronization systems.

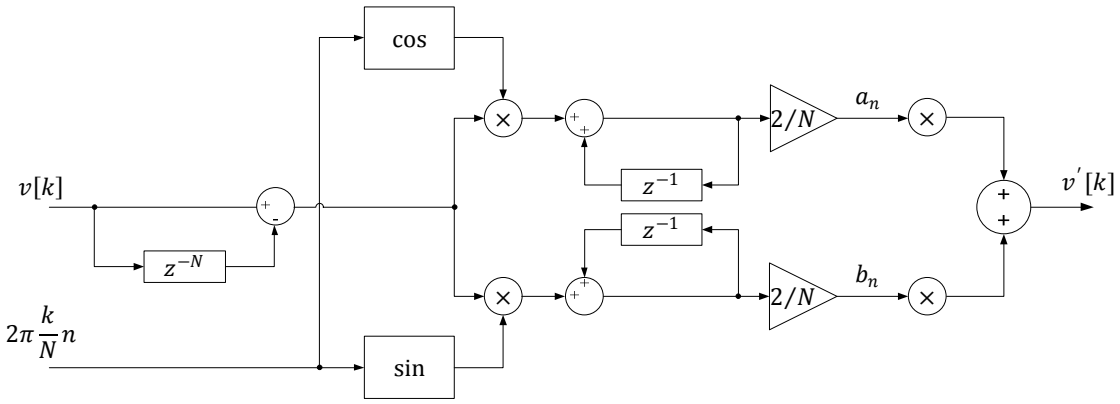


Figure 39 Discrete adaptive filter based on the RDFT

The Basic Phase-Locked Loop

A phase-locked loop (PLL) is a closed-loop system in which an internal oscillator is controlled to keep the time of some external periodic signal by using a feedback loop. PLLs can generate stable frequencies synchronized with external periodic events, recover signals from distorted sources or distribute clock-timing pulses in complex control systems. It is for these reasons that PLLs are so popular in utility interactive inverter systems. Additionally, the PLL provides continuous information about the phase angle and amplitude of the utility voltage, which allows space vector based controllers and modulators to be implemented, even if the signals are single-phase.

The basic structure of an elementary PLL consists of three fundamental blocks: the phase detector, the loop filter and the voltage-controlled oscillator, as can be seen in Figure 40.

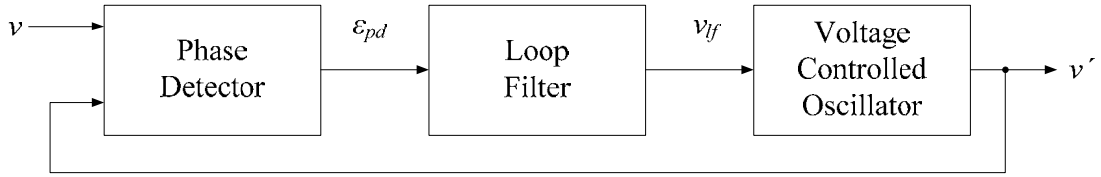


Figure 40 Basic structure of a PLL

The phase detector (PD) generates an output signal proportional to the phase difference between the input signal, *v*, and the signal generated by the internal oscillator of the PLL, *v'*. Depending on the type of PD being employed, high-frequency AC components appear together with the DC phase-angle difference signal.

The loop filter (LF) attenuates the high-frequency AC components from the PD output by means of a low-pass filter characteristic. As such, this block is typically constituted by a first-order low pass filter or a proportional-integral (PI) controller.

The last block in the PLL is the voltage-controlled oscillator (VCO) which generates an AC signal whose frequency is shifted with respect to a given central frequency, ω_c, as a function of the input voltage provided by the LF.

The implementation of these blocks is not rigid, and therefore different techniques can be utilized to design and build a PLL. The reader may wish to consult reference [11] if further, more detailed information regarding the PLL is required.

Figure 41 illustrates the block diagram of an elementary PLL.

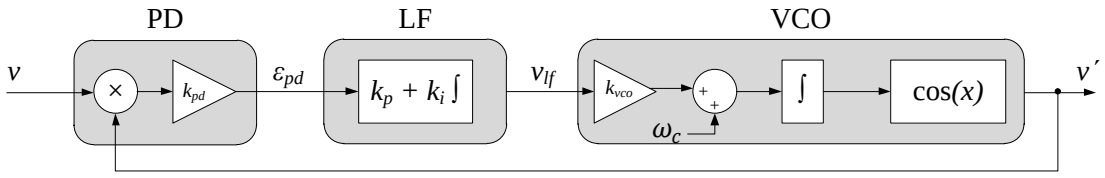


Figure 41 Block diagram of an elementary PLL

As we can see in the figure, the PD is implemented by means of a simple multiplier, the LF by means of a simple PI controller and the VCO consists of a sinusoidal function supplied by a linear integrator.

If the input signal applied to this system is given by

$$(59) \quad v = V\sin(\theta) = V\sin(\omega t + \varphi)$$

and the signal generated by the VSO is given by

$$(60) \quad v' = \cos(\theta') = \cos(\omega' t + \varphi')$$

The phase error signal from the PD output can be written as

$$(61) \quad \varepsilon_{pd} = Vk_{pd}\sin(\omega t + \varphi)\cos(\omega' t + \varphi')$$

$$= \frac{Vk_{pd}}{2}\left[\sin\left((\omega - \omega')t + (\varphi - \varphi')\right) + \sin((\omega + \omega')t + (\varphi + \varphi'))\right]$$

where $\sin\big((\omega-\omega')t+(\varphi-\varphi')\big)$ is the low frequency term and $\sin((\omega+\omega')t+(\varphi+\varphi'))$ is the high frequency term. Since the high frequency components of the PD error signal will be cancelled out by the LF, only the low frequency term will remain in equation (61). Thus, the PD error signal will be defined as follows

$$\bar{\varepsilon}_{pd}=\frac{Vk_{pd}}{2}\sin((\omega-\omega')t+(\varphi-\varphi')) \quad (62)$$

If it is assumed that the VCO is well tuned to the input frequency (i.e. $\omega\approx\omega'$), the DC term of the phase error signal is given by

$$\bar{\varepsilon}_{pd}=\frac{Vk_{pd}}{2}\sin(\varphi-\varphi') \quad (63)$$

We can see in equation (63) that the multiplier PD produces nonlinear phase detection due to the sinusoidal function. However, in the event that the phase error is very small (i.e. $\varphi\approx\varphi'$), the output of the multiplier PD can be linearized in the vicinity of such an operating point since $\sin(\varphi-\varphi')\approx\sin(\theta-\theta')\approx(\theta-\theta')$. Thus, once the PLL is locked, a relevant term of the phase error can be given by

$$\bar{\varepsilon}_{pd}=\frac{Vk_{pd}}{2}(\theta-\theta') \quad (64)$$

By applying Laplace transform to the previous equations, we can translate them into the complex frequency domain, where the analysis will be much simpler. If we consider that $k_{pd}=k_{vco}=1$ in Figure 41, then the following equations for the pertinent signals of the PLL will be obtained through Laplace transform:

$$E_{pd}(s)=\frac{V}{2}\big(\Theta(s)-\Theta'(s)\big) \quad (65)$$

$$V_{lf}(s)=k_p\left(1+\frac{1}{T_i s}\right)E_{pd}(s) \quad (66)$$

$$\Theta'(s)=\frac{1}{s}V_{lf}(s) \quad (67)$$

Equations (65), (66) and (67) represent the outputs, in the complex frequency domain, of the PD, LF and VCO respectively. As a result, we can represent the elementary PLL in the complex frequency domain in block diagram from as shown in Figure 42.

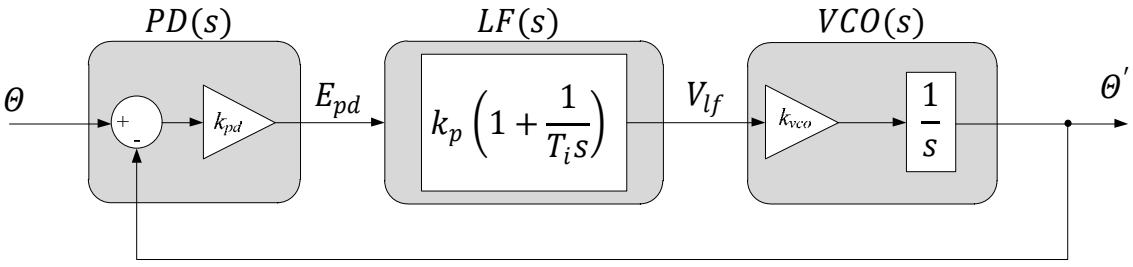


Figure 42 Small signal model of an elementary PLL

Furthermore, we can develop the following transfer functions of this closed loop system as shown by the following (assuming : $k_{pd} = k_{vco} = 1, V = 1$)
Open Loop Transfer Function:

$$(68) \quad F_{OL}(s) = PD(s) \cdot LF(s) \cdot VCO(s) = \frac{k_p s + \frac{k_p}{T_i}}{s^2}$$

Closed Loop Transfer Function:

$$(69) \quad H_\Theta(s) = \frac{\Theta'(s)}{\Theta(s)} = \frac{LF(s)}{s + LF(s)} = \frac{k_p s + \frac{k_p}{T_i}}{s^2 + k_p s + \frac{k_p}{T_i}}$$

Closed Loop Error Transfer Function:

$$(70) \quad E_\Theta(s) = \frac{E_{pd}(s)}{\Theta(s)} = 1 - H_\Theta(s) = \frac{s}{s + LF(s)} = \frac{s^2}{s^2 + k_p s + \frac{k_p}{T_i}}$$

The transfer functions (68) – (70) shows that the PLL is a 2nd order system with two poles located at the origin. This means that the PLL is able to track even a constant slope ramp in the input phase angle without any steady-state error. The transfer function of (69) indicates that the PLL exhibits a low pass filtering characteristic in the detection of the input phase angle, which attenuates the detection error caused by noise and higher order harmonics in the input. Transfer functions (69) and (70) can be written in the normalized general normalized form as follows:

$$(71) \quad H_\Theta(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$(72) \quad E_\Theta(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where

$$\omega_n = \sqrt{\frac{k_p}{T_i}} \quad \text{and} \quad \zeta = \frac{\sqrt{k_p T_i}}{2}$$

The following approximated expression is proposed in reference [12] for estimating the settling time, t_s, measured from the start time to the time in which the system stays within 1% of the steady state response of a particular second order system responding to a step input:

$$(73) \quad t_S = 4.6\tau \quad \text{with} \quad \tau = \frac{1}{\zeta\omega_n}$$

The approximation in (73) can also be used to obtain a rough estimate of the settling time of a system defined by (71), and hence the tuning parameters of the PI controller of the PLL of Figure 41 can be set as a function of the settling as follows:

$$(74) \quad k_p = 2\zeta\omega_n = \frac{9.2}{t_s}, \quad T_i = \frac{2\zeta}{\omega_n} = \frac{t_s\zeta^2}{2.3}$$

Keep in mind that the expression in (74) are obtained under the assumption of a unitary input signal (V = 1). For any non-unitary input signal, the expressions for setting the tuning parameters of the PI controller should be divided by the amplitude of the input signal V. Also, (73) should only be used as a guide and the final system should be checked to verify compliance with specifications.

We can also define the bandwidth of our PLL system to be

$$(75) \quad \omega_{-3dB} = \omega_n\sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta)^2 + 1}}$$

However, it can be shown through simulations that the results of these equations and the response of the PLL differ greatly. This is due to the fact that we made an assumption that the frequency of the input signal is much higher than the bandwidth of the PLL. Therefore, we neglected the high frequency term of the phase error signal provided by the

PD. The issue here is that in a grid connected application, such as a utility interactive inverter, the utility frequency is very close to the cut-off frequency of the PLL. As such, the assumption of high frequency cancellation can no longer be accepted and a new PD must be used when designing a PLL for utility interactive applications.

In-Quadrature Phase Detection

One such PD that can be designed for utility interactive applications is based on a set of in-quadrature signals, that is, signals that are out of phase from one another by 90° (π/2). At the heart of the PD would be a quadrature signal generator (QSG), such as the one shown in Figure 43.

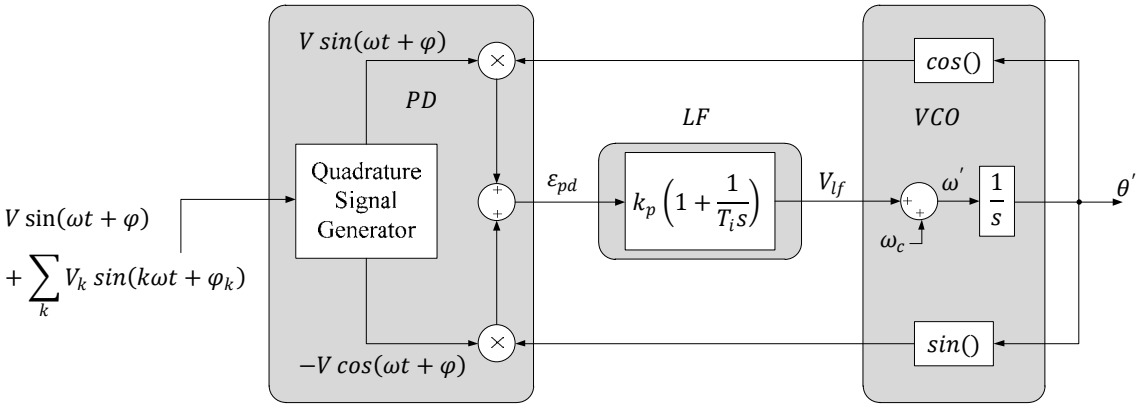


Figure 43 Diagram of a PLL with an in-quadrature PD

An ideal QSG is assumed to be able to extract a clean set of in-quadrature signals without introducing any delay at any frequency from a given distorted input signal. The phase angle error signal resulting from this ideal in-quadrature PD is given by

$$\varepsilon_{pd} = V\sin(\omega t+\varphi)\cos(\omega' t+\varphi') - V\cos(\omega t+\varphi)\sin(\omega' t+\varphi') \tag{76}$$

$$= V\sin\big((\omega-\omega')t+(\varphi-\varphi')\big) = V\sin(\theta-\theta')$$

Based on (76), when the PLL is well synchronized (i.e. $\omega=\omega'$), the in-quadrature PD does not generate any steady state oscillatory term, thereby increasing the PLL bandwidth and overcoming cut-off frequency issue stated earlier.

Analysis of (76) reveals that it is a part of the Park transformation, which is defined in [13]. As such, the diagram illustrated in Figure 43 can be redrawn in Figure 44, where the $\alpha\beta$ to dq transformation block corresponds to the following transformation matrix:

$$(77) \quad \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}$$

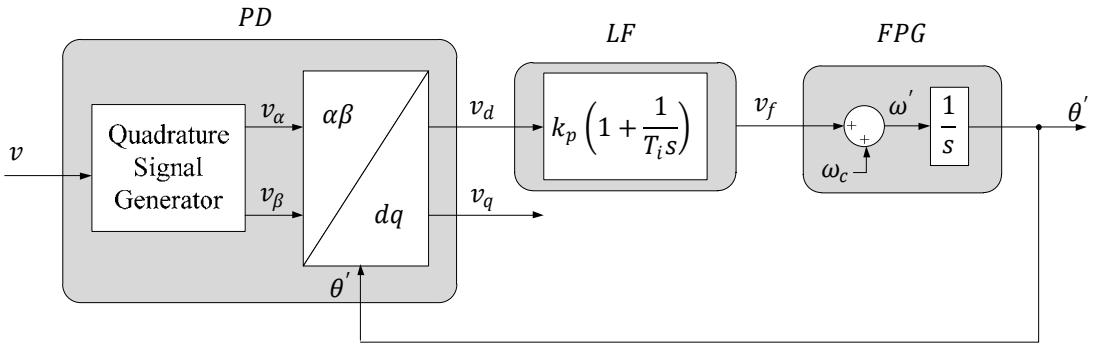


Figure 44 PD based on the quadrature signal generator and the Park transformation

We can see the VCO used earlier has been replaced by a new block called the frequency/phase-angle generator (FPG). This has been done to provide the phase-angle for the sinusoidal functions of the Park transformation, making it a sort of synchronous phase detector.

If the input voltage of the PLL is given by

$$(78) \quad v = V\sin(\theta) = V\sin(\omega t + \varphi)$$

then the output signals from the quadrature signal generator can be expressed by the following vector:

$$(79) \quad \boldsymbol{v}_{(\alpha\beta)} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = V \begin{bmatrix} \sin(\theta) \\ -\cos(\theta) \end{bmatrix}$$

Consequently, by substituting (79) into (77), the output of the PD of Figure 44 is given by the voltage vector of the following equation, which will be free of oscillations if the PLL is well tuned to the input frequency.

$$(80) \quad \boldsymbol{v}_{(dq)} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = V \begin{bmatrix} \sin(\theta - \theta') \\ -\cos(\theta - \theta') \end{bmatrix}$$

The use of a QSG in the PLL of Figure 44 allows a vector approach to be adopted when dealing with single phase systems. In Figure 45, the QSG output signals of (79) are represented on an orthogonal and stationary reference frame defined by the $\alpha\beta$ axes, which gives rise to the virtual input vector $\vec{v}$. Likewise, the output signals of the Park

transformation are represented by the projections of the voltage vector $\vec{v}$ on an orthogonal and rotating reference frame defined by the *dq* axes. If the input voltage is defined by $v_\alpha = V\sin(\theta)$, it can be understood as the projection of the input voltage on the stationary α axis. On the other hand, the angular position of the *dq* rotating reference frame, θ', is given by the PLL. When the PLL is well tuned to the input frequency (i.e. $\omega \approx \omega'$), the virtual input vector and *dq* reference frame have the same angular speed.

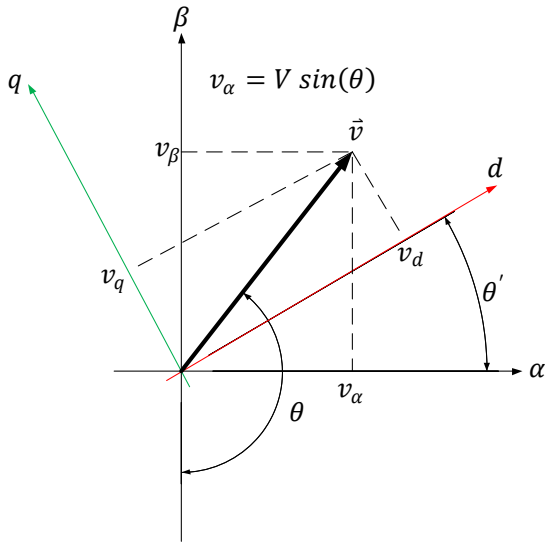


Figure 45 Vector representation of the QSG output signals

Furthermore, when the PLL is perfectly locked, one of the axes of the *dq* reference frame will overlap the virtual input vector. As seen in Figure 44, the PI regulator of the LF will set the angular position of the *dq* reference frame to make $v_d = 0$ in the steady state, which means that the virtual input vector will rotate orthogonally to the *d* axis. In the case where the PI regulator is connected to the v_q output of the PD, as shown in Figure 46, the virtual input vector will rotate, overlapping the *d* axis of the *dq* reference frame in the steady state. In such a case, the v_d signal will provide the amplitude of the input voltage vector and phase angle detected by the PLL will be in phase with the virtual input vector, which means that the detected phase angle will be 90° lagging with respect to the sinusoidal input voltage (i.e. $\theta' = \theta - \pi/2$).

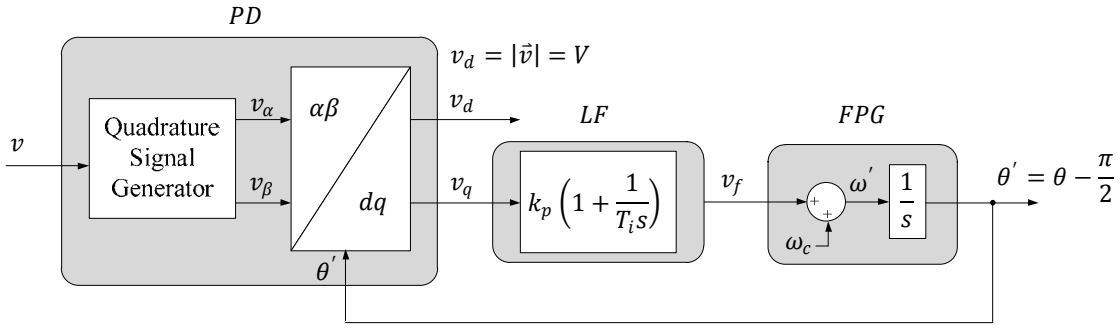


Figure 46 PLL with the LF on the *q* axis of the QSG

This analysis of the in-quadrature signals has shed some light as to the importance of QSG in the design of an accurate PLL synchronized with the single phase utility supply. Let us now realize some techniques so as to develop a sound QSG to achieve in-quadrature signals.

T/4 Transport Delay PLL

The *T*/4 transport delay technique (Figure 47), with *T* being the fundamental grid frequency period, is probably the easiest way to implement a QSG. The transport delay block can be effortlessly programmed through the use of a first-in-first-out (FIFO) buffer, whose size is set to one-fourth of the number of samples contained in one cycle of the fundamental frequency. The QSG based on the *T*/4 transport delay buffer works will if the input voltage is a purely sinusoidal waveform at the rated utility frequency. If the grid voltage frequency changes with respect to its rated value, the output signals of the QSG will not be perfectly orthogonal, which will give rise to errors in the PLL synchronization.

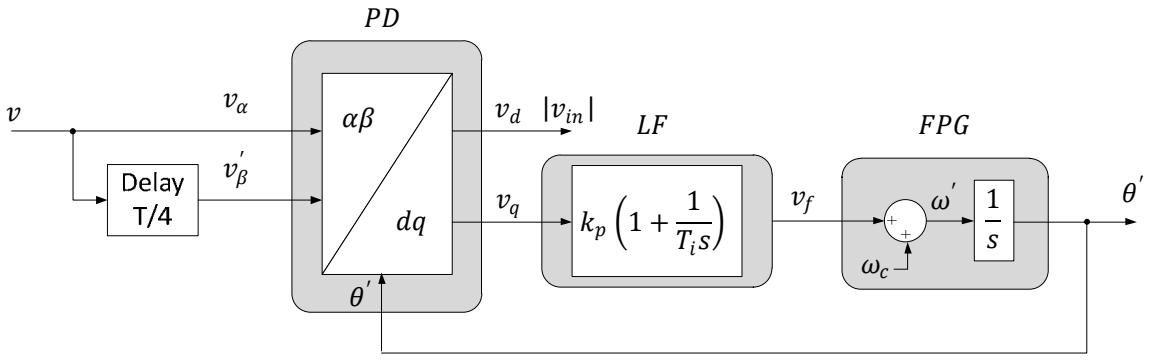


Figure 47 PLL based on a T/4 transport delay

This QSG technique does not provide any filtering capability, so if the single phase input voltage is tainted with harmonic components, they will act as a perturbation for the PLL. Additionally, the orthogonal signals generated by the QSG based on a *T*/4 transport delay block will not actually be in-quadrature, since each of the frequency components of the input signal had to be delayed by one-fourth of its fundamental period.

It is clearly evident that the rudimentary *T*/4 transport delay PLL will not suffice as an adequate synchronization method for utility interactive inverters.

Adaptive Filtering PLL – Enhanced PLL

An adaptive filter (AF) is a filter that has the ability to adjust its own parameters automatically according to an optimization algorithm, and their design requires little or no prior knowledge of the signal to be filtered. A basic diagram describing the adaptive noise cancelling (ANC) concept is shown in Figure 48.

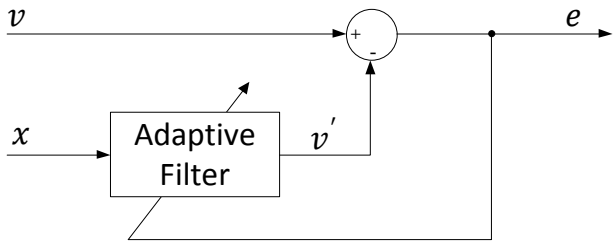


Figure 48 Adaptive noise cancelling (ANC) system

The signal to be filtered is applied to the input *v*. This input signal consists of a primary signal *s* plus a noise n_0 uncorrelated to the signal *s*. An auxiliary reference signal n_1, correlated to the noise signal n_0, is applied to the input *x*. The reference signal n_1 is adaptively filtered to produce an output signal *v'* that is as close a replica as possible of n_0. This output signal is subtracted from the primary input to produce the output signal *e*. As a result, the primary noise is eliminated by cancellation. When the ANC technique is used to cancel out specific frequency components of the input signal, this filtering concept is also called adaptive notch filtering (ANF) [14].

In the digital implementation of an ANC filter, the reference signal *x* is sampled at a proper sampling period T_S and stored in an *N*-length buffer to generate the reference vector $\boldsymbol{x}$. Thus, at the *k*th sample, i.e. at the time $t = kT_S$, the reference vector is given by $\boldsymbol{x}_k = [x_k, x_{k-1}, \dots, x_{k-N}]$. The elements of the $\boldsymbol{x}_k$ vector are weighted and summed to give the adaptive filter output v'_k. The most extended adaptation algorithm used to set the weights of the adaptive filter, $\boldsymbol{w}_k = [w_k, w_{k-1}, \dots, w_{k-N}]$, is the least-mean-squares

(LMS) algorithm. A simple version of the LMS algorithm at the time *k* can be given by the following equations:

$$v'_k = \boldsymbol{w}_k^T \cdot \boldsymbol{x}_k \quad (81)$$

$$e_k = v_k - v'_k \quad (82)$$

$$\boldsymbol{w}_{k+1} = \boldsymbol{w}_k + \alpha e_k \boldsymbol{x}_k \quad (83)$$

The LMS algorithm is an iterative gradient-descent algorithm that uses an estimate of the gradient on the mean-square error surface to seek the optimum weight vector at the minimum mean-square error point. The term $e_k \boldsymbol{x}_k$ represents the estimate of the negative gradient and the adaptation gain α determines the step size taken at each iteration along that estimated negative-gradient direction. A simple LMS algorithm is illustrated in Figure 49 with only one weight, $N = 1$. It is interesting to note the forward Euler discrete integrator *S(z)* built into the algorithm.

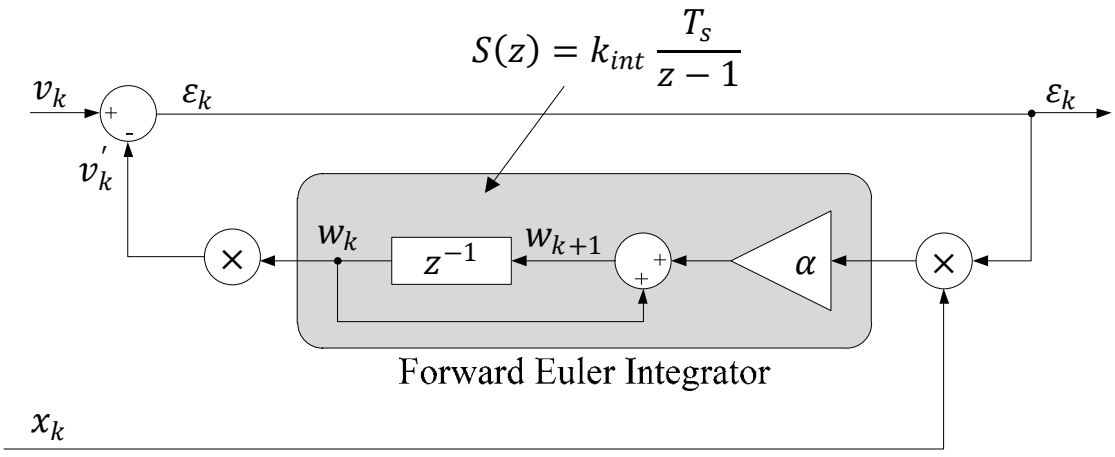


Figure 49 A simple least mean square algorithm with one weight

This ANC can be applied to the conventional single phase PLL described earlier, so as to enhance the performance of the multiplier PD. In this application, the ANC works as an ANF in which the grid voltage signal is applied to the input *v* and a unitary sinusoidal signal, provided by the VCO of the PLL, is applied to the input *x* as a reference signal. This is better known as the Enhanced PLL (EPLL) and is shown in Figure 50.

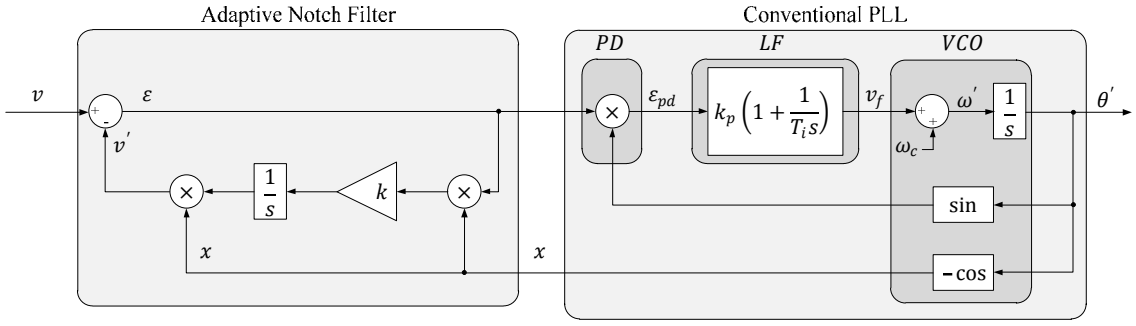


Figure 50 Enhanced PLL (EPLL)

In the EPLL, the output of the ANF becomes zero as the frequency and phase angle of the reference signal generated by the VCO, $x = \cos(\theta')$, match those of the input signal *v*. Thus, signal oscillations at the output of the multiplier PD are completely cancelled out and the input signal phase angle is properly detected by the conventional PLL. However, there will exist a 90° phase shift between θ and θ' in the steady state due to the effect of the multiplier PD.

Second-Order Adaptive Filtering PLL

An important piece of information that we can take from the previous section is that if a single-frequency sinusoidal signal *v* is applied to the input of the ANC in Figure 49, the output error signal ε is equal to zero (at steady state), if and only if the both the frequency and the phase angle of the sinusoidal input match those of the sinusoidal reference signal *x*. We would, however, like to have the output error signal ε equal zero when just the frequency of *v* and *x* are equal, independent of their phase angles.

This can be accomplished by adding another stage of adaptive weights to the diagram in Figure 49, and thus turning it into a second order adaptive filter. This filter utilizes two sinusoidal reference signals at the frequency ω and shifted by 90° as inputs to the adaptive algorithm. The discrete form of this second order AF can be seen in Figure 51 and the continuous time domain form in Figure 52.

Let us turn our attention to the diagram in Figure 52 so that we may extract its transfer function. Defining $g = k\varepsilon_v$, the v_d and v_q signals of Figure 52 can be expressed as

$$(84) \quad v_d = g\cos(\omega' t) = \frac{1}{2} g\left[e^{j\omega' t} + e^{-j\omega^t t}\right]$$

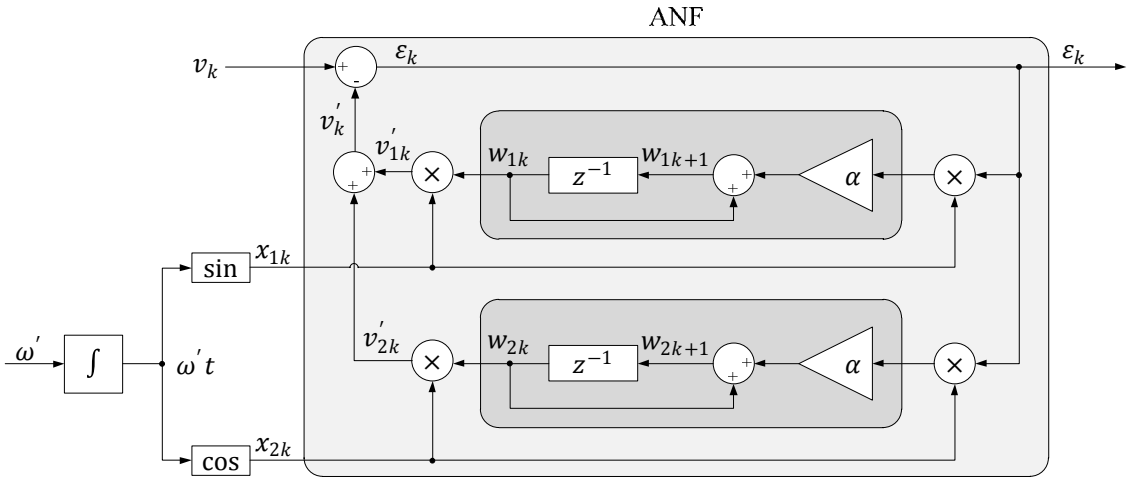


Figure 51 Discrete form of second order ANF with LMS algorithm

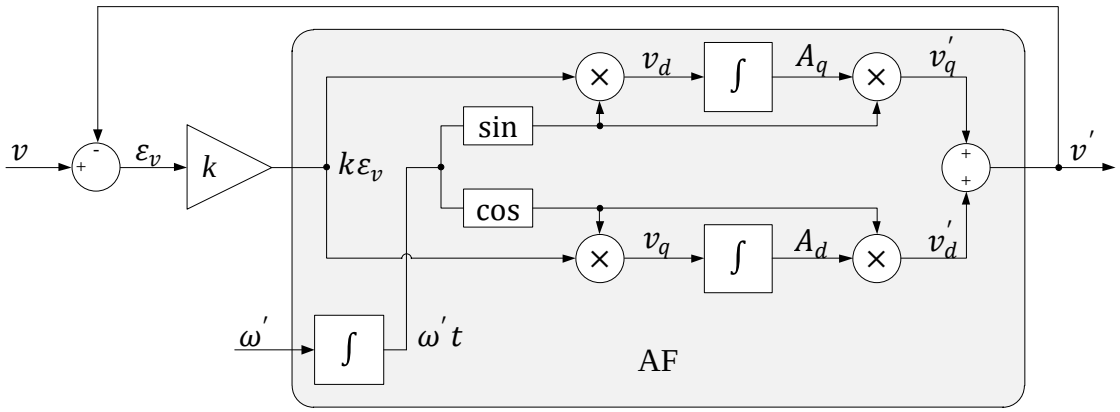


Figure 52 Second order adaptive filter in the continuous time domain

$$v_d = g\cos(\omega' t) = \frac{1}{2} g\left[e^{j\omega' t} + e^{-j\omega^t t}\right] \quad (84)$$

$$v_q = g\sin(\omega' t) = \frac{1}{j2} g\left[e^{j\omega' t} - e^{-j\omega^t t}\right] \quad (85)$$

The variables, A_d and A_q, corresponding to the output of the integrators for v_d and v_q, can be expressed in the frequency domain as

$$A_d(s) = \frac{1}{s} v_d(s) = \frac{1}{2s}[g(s + j\omega' t) + g(s - j\omega' t)] \quad (86)$$

$$(87) \quad A_q(s) = \frac{1}{s} v_q(s) = \frac{1}{j2s}[g(s + j\omega' t) - g(s - j\omega' t)]$$

In the same manner, we can obtain the Laplace transforms for v'_d and v'_q as follows

$$(88) \quad v'_d(s) = \frac{1}{2}[A_d(s + j\omega' t) + A_d(s - j\omega' t)]$$

$$= \frac{1}{4(s + j\omega')}[g(s) + g(s + 2j\omega')] + \frac{1}{4(s - j\omega')}[g(s) + g(s - 2j\omega')]$$

$$(89) \quad q(s) = \frac{1}{j2}[A_q(s + j\omega' t) - A_q(s - j\omega' t)]$$

$$= \frac{1}{4(s + j\omega')}[g(s) - g(s + 2j\omega')] + \frac{1}{4(s - j\omega')}[g(s) - g(s - 2j\omega')]$$

Lastly, by adding (88) and (89), we obtain the output of the AF, v', as follows:

$$(90) \quad v'(s) = v'_d(s) + v'_q(s) = \frac{s}{s^2 + \omega'^2} g(s)$$

As such, the transfer function of the AF is given by

$$(91) \quad AF(s) = \frac{v'}{k\varepsilon_v}(s) = \frac{s}{s^2 + \omega'^2}$$

Thus, the response of the system is defined by two second-order transfer functions, one being an adaptive band-pass filter (ABPF) and the other an adaptive notch filter (ANF), as shown below:

$$(92) \quad ABPF(s) = \frac{v'}{v}(s) = \frac{AF(s)}{1 + AF(s)} = \frac{ks}{s^2 + ks + \omega'^2}$$

$$(93) \quad ANF(s) = \frac{\varepsilon_v}{v}(s) = 1 - ABPF(s) = \frac{s^2 + \omega^2}{s^2 + ks + \omega'^2}$$

The band-pass characteristic of this adaptive filter implies that we can extract a particular component at a frequency of interest, ω', even if the input is affected by harmonics and distortion. Moreover, by adding a scaled integrator at the output of the filter, we are able

to use it as a quadrature signal generator as shown in Figure 53. In fact, since v' and qv' are 90° shifted, we can apply this adaptive filter to the input of any phase detector based on QSG and thereby improve the performance of the conventional single phase PLL.

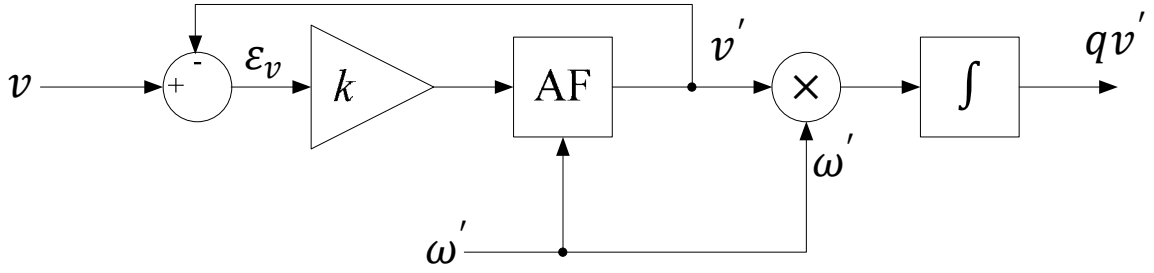


Figure 53 QSG based on a second order AF

Second-Order Generalized Integrator PLL

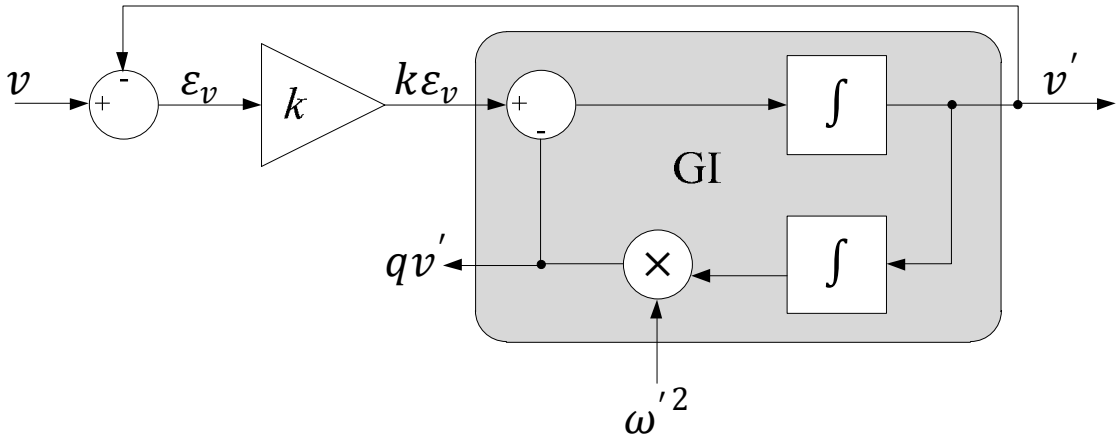


Figure 54 Second order AF based on general integrator (GI)

The generalized integrator (GI) can be defined as the transfer function shown in (91) multiplied by 2. However, the model shown in Figure 52 is not the only way implement a GI. For example, Figure 54 shows a second order AF based on a very efficient implementation of the GI. The characteristic transfer functions of the AF of Figure 54 are calculated to be

$$(94) \quad GI(s) = \frac{v'}{k\varepsilon_v}(s) = \frac{s}{s^2 + \omega'^2}$$

$$(95) \quad D(s) = \frac{v'}{v}(s) = \frac{ks}{s^2 + ks + \omega'^2}$$

$$(96) \quad Q(s) = \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + ks + \omega'^2}$$

We can clearly see that the transfer function of (94) is identical to that of (91). However, the model illustrated in Figure 54 is much simpler than that described by Figure 52. First of all, the use of sinusoidal functions in Figure 52 requires large lookup tables that increase computation time and introduce additional quantization noise into the discrete system. More importantly, by analyzing (92) and (93), we see that the bandwidth of the band-pass filter and the static gain of the low-pass filter are not only a function of the gain *k*, but also of the center frequency of the filter, ω'. This poses a huge dilemma if designing for variable-frequency systems, such as in PLL design.

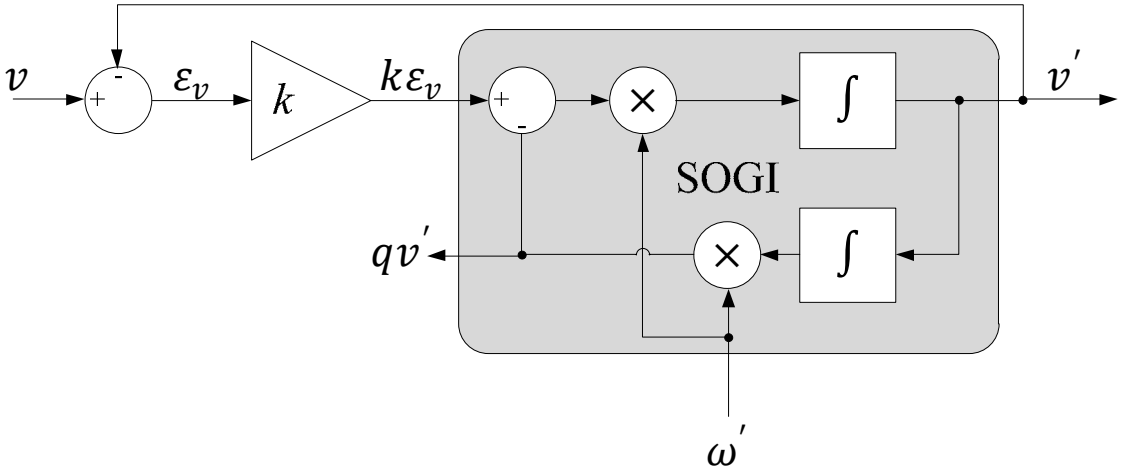


Figure 55 Second order adaptive filter based on a Second Order Generalized Integrator (SOGI-QSG)

A novel solution to this problem is the second-order generalized integrator (SOGI) shown by Figure 55. The characteristic functions of the SOGI can be found to be

$$(97) \quad SOGI(s) = \frac{cc}{k\varepsilon_v}(s) = \frac{\omega' s}{s^2 + \omega'^2}$$

$$(98) \quad D(s) = \frac{v'}{v}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2}$$

$$(99) \quad Q(s) = \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2}$$

We can see from (98) and (99) that the bandwidth of the SOGI filter is not a function of the center frequency but only depends on the gain *k*, which obviously makes it very suitable in variable-frequency applications. Also, the amplitudes of the in-quadrature signals, v' and qv', match the amplitude of the input signal *v* when the center frequency of the filter ω', matches the input frequency, ω. This proves to be a very suitable method for QSG, and as such, we can utilize this in conjunction with a Park Transform discussed earlier, and create a very robust and practical phase detector (PD) as part of a complete SOGI-based PLL (SOGI-PLL) shown in Figure 56. It can be shown that this implementation significantly improves phase angle detection in a conventional PLL [15]. Our goal, however, is to develop a system in which the algorithm responds well to both amplitude and frequency changes. This is shown through the SOGI frequency-locked loop.

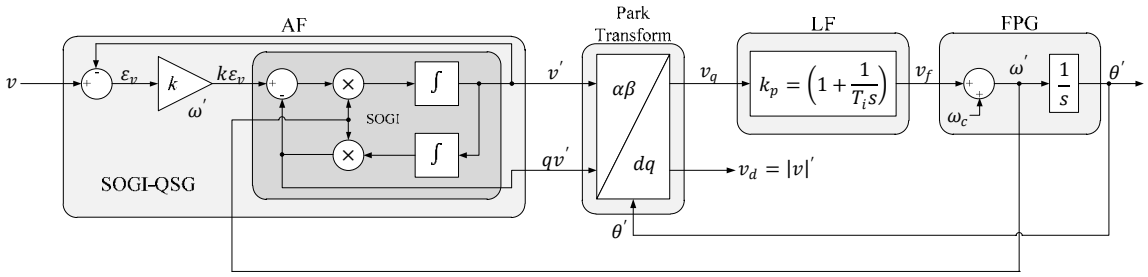


Figure 56 SOGI-based PLL (SOGI-PLL)

SOGI Frequency-Locked Loop

We can further improve upon the SOGI-QSG by recognizing that its inherent resonant character makes itself work as a voltage-controlled oscillator. Thus, we could develop a control to auto-adapt the center frequency of the SOGI resonator to the input frequency and discard the PLL block from the SOGI-PLL, hence creating a frequency-locked loop (FLL). The first step to making the SOGI-QSG auto-tunable is to analyze the error signal ε_v and see how the center frequency might be controlled by using this error signal. Below is the transfer function from the input *v* to the error signal ε_v:

$$(100) \quad E(s) = \frac{\varepsilon_v}{v}(s) = \frac{s^2 + \omega'^2}{s^2 + k\omega' s + \omega'^2}$$

This transfer function corresponds to a second-order notch filter with attenuation at the center frequency. Let us now recall (99) and use it to find a relationship between the error signal ε_v and the in-quadrature signal at the AF output, qv'. Figure 57 is the Bode diagram of both *Q(s)* of (99) and *E(s)* of (100) at 60 Hz center frequency with a gain of $k = \sqrt{2}$.

We can see from the Bode plot an interesting relationship. The signals ε_v and qv' are in phase when the input frequency is lower than the SOGI resonance frequency ($\omega < \omega'$) and are opposite in phase (180°) when the input frequency is higher than the SOGI resonance frequency ($\omega > \omega'$).

Thus, a frequency error variable, ε_f, can be defined as the product of ε_v and qv', whose average value, $\bar{\varepsilon}_f$, will be positive when $\omega < \omega'$, zero when $\omega = \omega'$, and negative when $\omega > \omega'$. This allows for a simple frequency locking loop (FLL) to be designed, as shown in Figure 58. In the FLL, an integral controller with a negative gain, $-\gamma$, is used to eliminate the DC component of ε_f by shifting the center frequency of the SOGI-QSG, ω', until it matches the input frequency, ω.

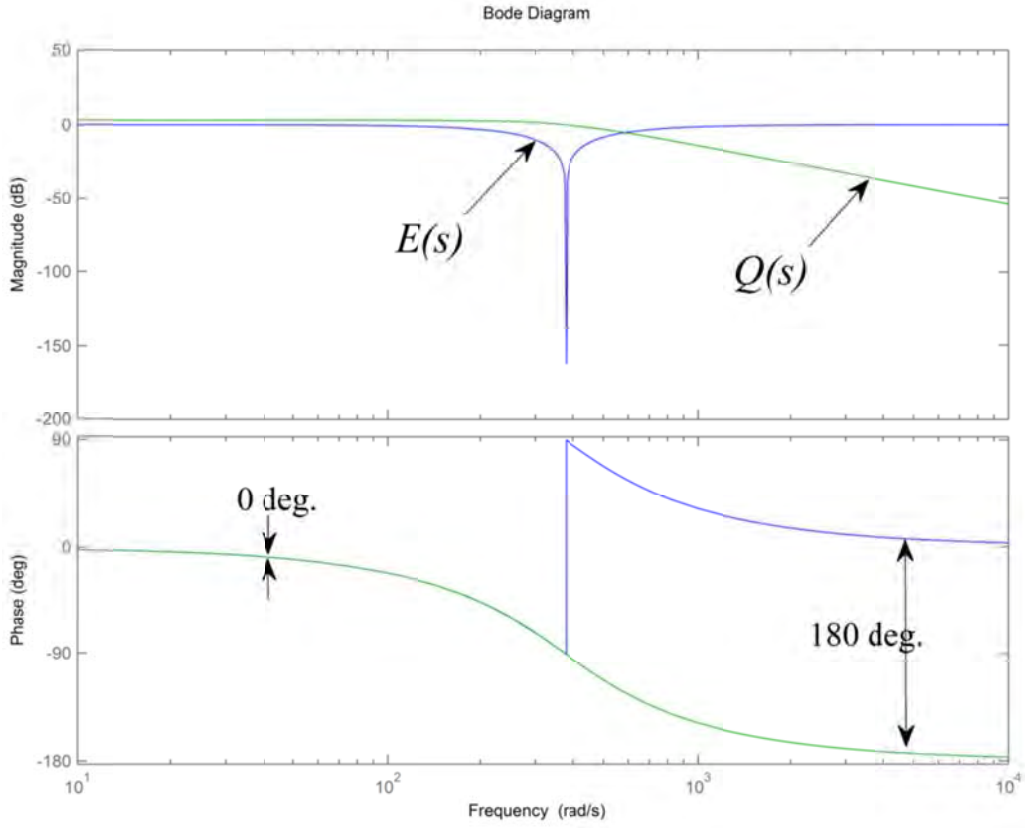


Figure 57 Bode plot of *E(s)* and *Q(s)*

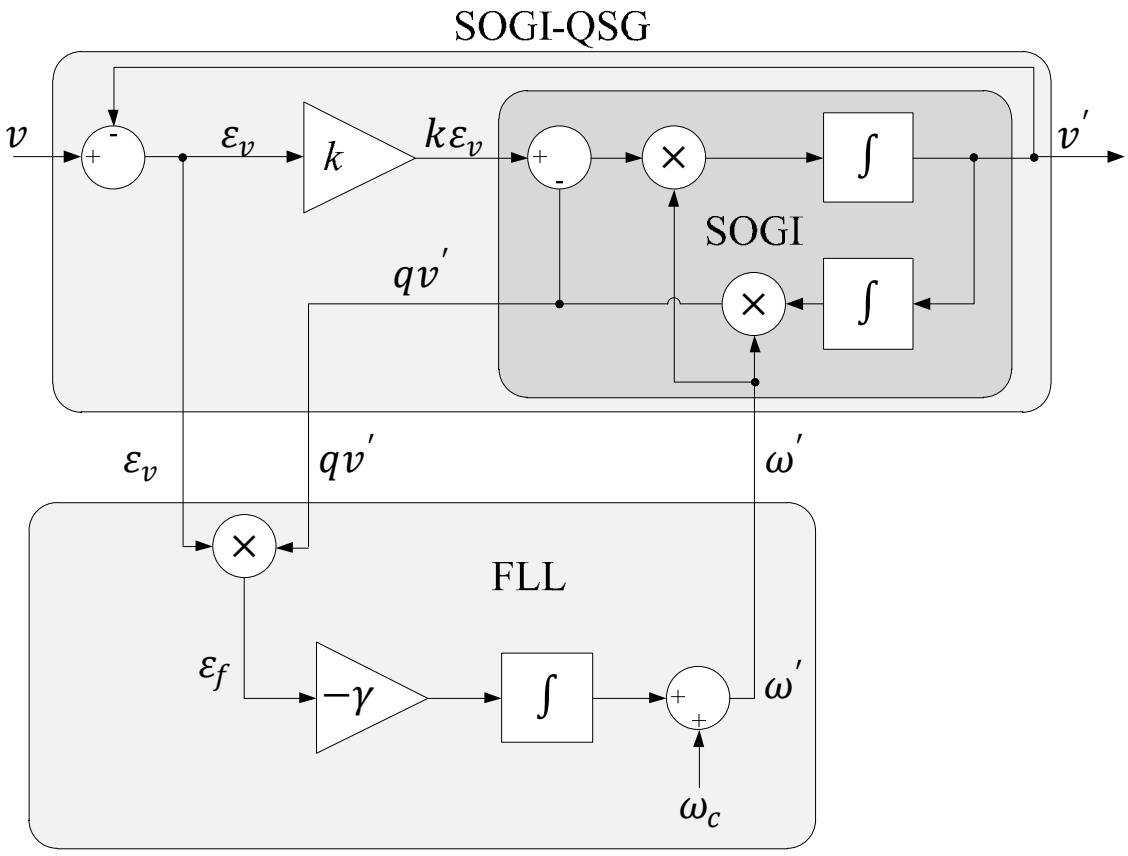


Figure 58 SOGI-based QSG with FLL

Also, the nominal value of the utility frequency, in our case roughly 377 rad/s, is added to the FLL output as feed-forward variable, ω_c, to accelerate the initial synchronization process. By combining the SOGI-QSG with the FLL, we are given a single phase utility synchronization system: the SOGI-FLL. However, it can be shown that the negative gain $-\gamma$ can be normalized by feeding back the estimated grid operating conditions, guaranteeing a constant settling time in the frequency estimation independently of the input signal parameters. This is shown by the SOGI-FLL with FLL gain normalization in Figure 59. It can also be shown that the SOGI-FLL with FLL gain normalization operates superbly in the event of simultaneous changes to the voltage amplitude and frequency, usually occurring during utility faults.

It is shown in [10] that the SOGI-FLL provides the fastest and most accurate response of any of the utility synchronization techniques discussed. It is also shown in [10] that a similar conclusion can be made regarding three-phase utility systems and that the implementation of a Double SOGI-FLL provides the fastest and most accurate response.

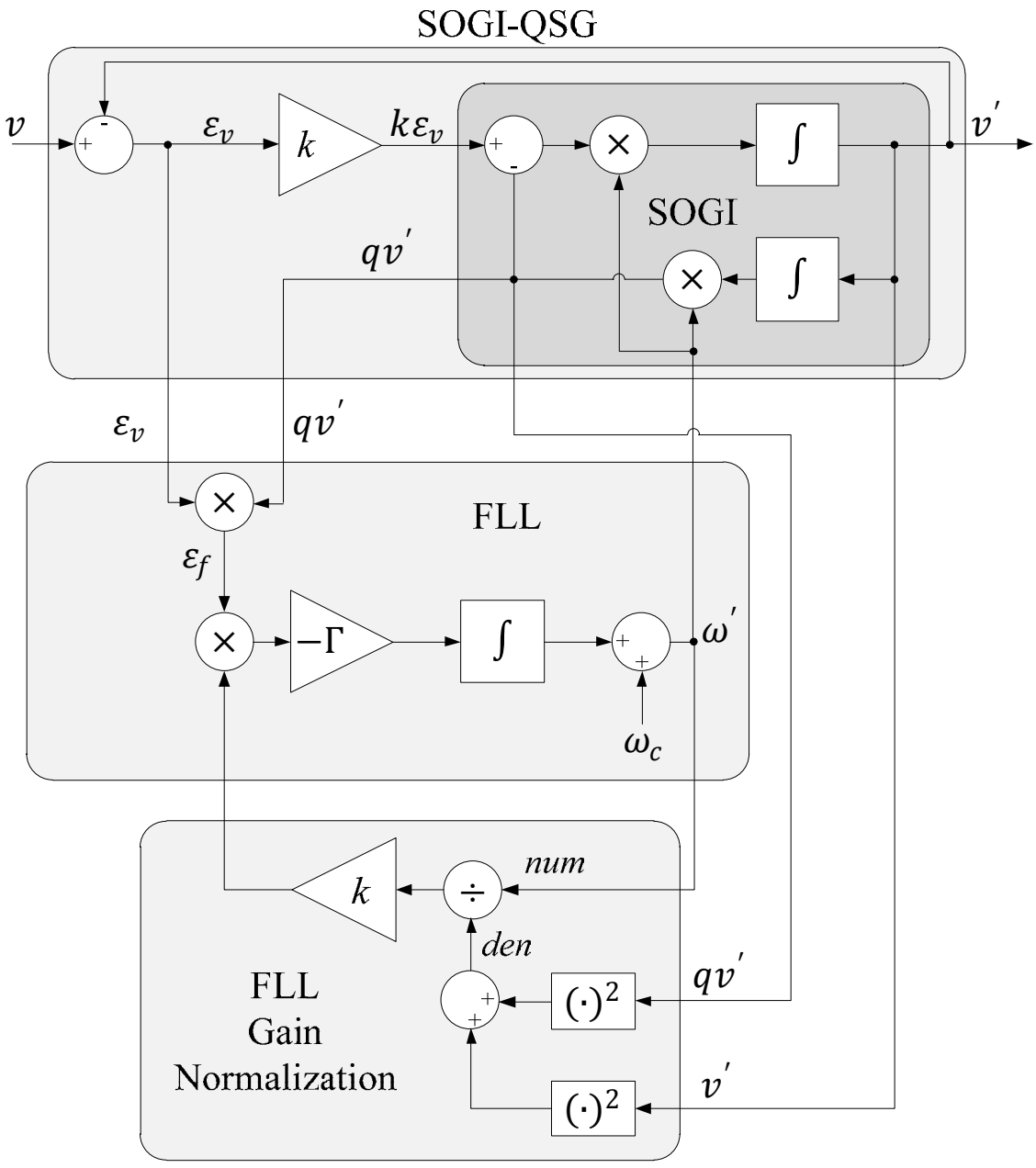


Figure 59 SOGI-FLL with FLL gain normalization

The creation of these synchronization blocks is essential in inverter systems as they will be utilized to provide reference signals to the PWM blocks discussed earlier and will directly impact the output waveforms generated by the inverter and injected into the grid. As such, standards like IEEE 1547 will be much easier to comply by.

ANTI-ISLANDING CONSIDERATIONS

Introduction

As discussed earlier, islanding poses some real problems in the event of a utility shutdown. Safety of the utility line workers must be ensured while preserving the power quality delivered to the grid. However, anti-islanding (AI) has proven to be a technically challenging characteristic of the utility interactive inverter. The issue arises in the fact that there exists a non-detection zone (NDZ) in which the inverter's measured control parameters, such as the voltage and frequency outline by IEEE 1547, do not stray away from their limits during an islanding condition. We will briefly discuss the concept of the NDZ so as to lay a foundation for methods to overcome it. We will discuss the three types of these methods: Utility level methods, Passive inverter level methods and Active inverter level methods. We will also briefly discuss two new active methods that have been recently proposed. A thorough analysis has been conducted in [16], in which different methods have been applied and the results have been documented along with the respective strengths and weaknesses of each method.

The Non-Detection Zone

The non-detection zone (NDZ) can best be described as a set of conditions in which the inverter fails to detect an abnormal or tripped condition in the grid and continues to operate, thus not complying with IEEE 1547. As such, we consider the reliability of different islanding detection methods based on their respective NDZ. The best way to describe the NDZ is to first consider the RLC test load prescribed by IEEE 1547 and definition of the following relationships:

$$\Delta P = P_{load} - P_{DG} \quad (101)$$

$$\Delta Q = Q_{load} - Q_{DG} \quad (102)$$

where P_{load} and Q_{load} are the real and reactive powers of the load respectively, P_{DG} and Q_{DG} are the real and reactive output powers of the inverter respectively and, ΔP and ΔQ, as seen from (101) and (102), are the real and reactive output powers of the utility respectively. This is best shown in Figure 60. Also, a general depiction (for most Passive AI methods) of the NDZ is shown in Figure 61. We can clearly see that in the event that the load's real and reactive powers are very close to those generated by the inverter, there isn't a large enough change in the real and reactive powers delivered by the grid to cause over/under-voltage (OV/UV) and/or over/under-frequency (OF/UF). Thus, it is said that there is no "mismatch" between the powers produced by the inverter

and that of the utility, hence leading to a NDZ. A worst-case scenario is possible and is determined to be the event in which a balance exists between the load and grid impedances. In this case, there is no change in amplitude or frequency of the measured signal, again leading to a NDZ. By understanding this relationship, we can easily conclude that the standard OUV/OUF protection schemes of the inverter are not at all sufficient to prevent an islanding condition. As such, other methods must be employed to ensure proper anti-islanding protection as prescribed by IEEE 1547.

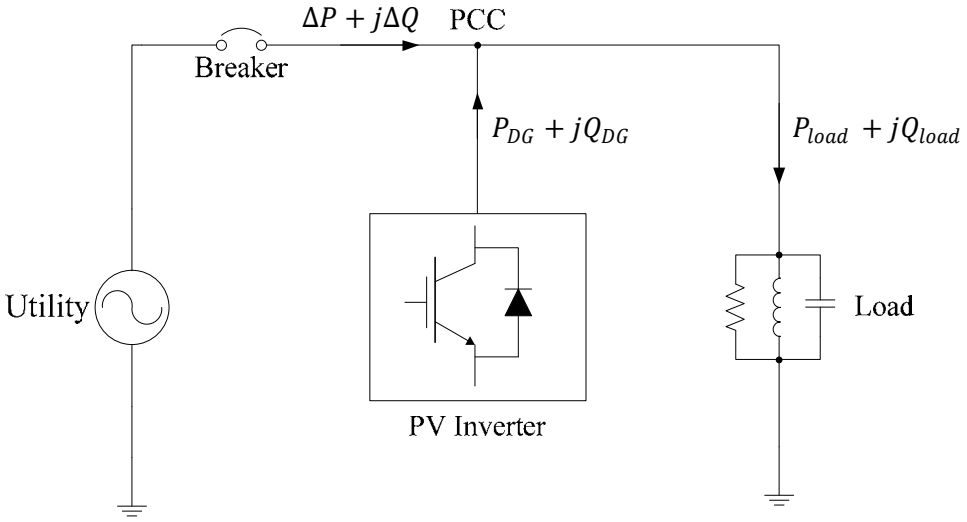


Figure 60 Diagram of test set-up required by IEEE 1547

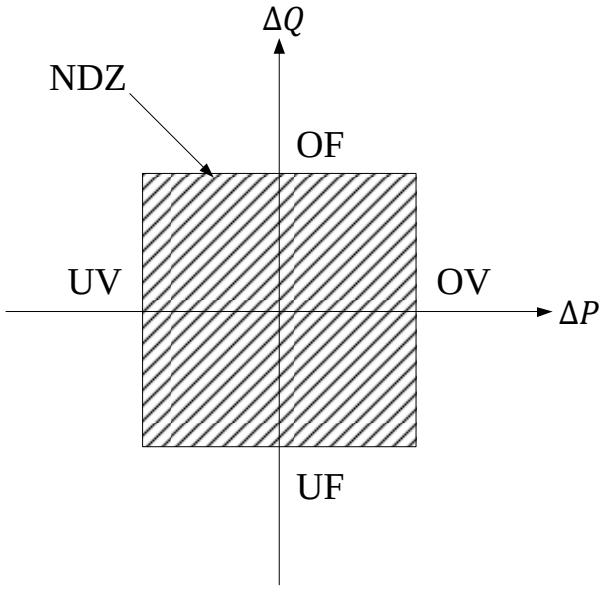


Figure 61 The non-detection zone (NDZ)

Utility Detection of Islanding

Utility detection methods were probably one of the first islanding detection methods to come into the minds of engineers trying to solve this problem. The reason being that it is probably the only method to ensure adequate anti-islanding and the elimination of the NDZ. The utilities employ a supervisory control and data acquisition (SCADA) system to constantly monitor and control all equipment involved in the power delivery process. As such, it is easy to envision that when part of the grid is disconnected, the utility can, with a control signal, effectively shut down any distributed generation (DG), like a PV system to prevent islanding; and conversely, once the grid is reenergized, the DG can be turned back on again. This appears to be a very straightforward and full-proof solution to islanding. However, the main drawback of this method is the amount of financial resources it will take to complete such a project, not to mention the burden it will place on the utility; which will probably result in higher utility bills for customers. Even if the financial hurdle can be overcome, in the present time, the amount of installed private DGs is not high enough to warrant such a project. As such, we are left with methods residing within the inverter itself.

Passive Detection of Islanding

Although we will briefly discuss some passive detection methods, such as the OUV/OUF stated earlier, in this section, it is worth noting that these methods will never reduce the NDZ down to an acceptable level to comply with any standard such as IEEE 1547. As such, either active methods or hybrid passive-active methods must be employed.

The phase jump detection (PJD) method monitors the phase difference between the inverter terminal voltage and its output current. During normal operation, the inverter current is synchronized with every zero-crossing of the grid voltage. Therefore, if the grid goes offline, the current is now synchronized with only the inverter's voltage reference. Therefore, a phase shift in the current must take place since there has been no change in frequency and the phase of the load has not changed. This phase shift is compared to the old value and if it passes a certain threshold, the inverter can be programmed to trip. The problem with this method is the same as other passive methods in that the choice of threshold values is a very difficult task, and will change for every installation, making it hard to make a universal utility interactive inverter. Also, loads such as motors cause significant transient phase jumps during startup, which will lead to nuisance tripping.

The other passive method we will discuss is the harmonic detection (HD) method. This method analyzes the THD of the voltage at the point of common coupling (PCC), where

the inverter terminals meet the utility supply. If the THD exceeds some threshold value, the inverter is programmed to shut down. Under normal operating conditions, the grid voltage will force the THD of the voltage to be approximately zero, forcing a low distortion sinusoidal signal at the terminals which forces the current drawn to the load to be sinusoidal. The inverter is designed to produce currents with THD of less than 5%, a low amount of harmonics. Due to the grid's low impedance, these low harmonic currents flow into the grid and interact with the low impedance to produce a low amount distortion in the signal. This distortion is not detectable during normal operation of the inverter while connected to the utility.

In the event an island occurs, the high frequency switching employed by inverters invariably causes harmonics in the output voltage. Without the presence of the "stiff" low distortion utility voltage, these harmonics can now be detectable and the inverter can be programmed to shut down if the value exceeds a certain threshold. However, as stated again, it is very difficult to set a universal THD limit for all inverters and their particular installations. Also, the nature of the load has a direct impact on the harmonics detected at the PCC. For example, let us assume our inverter produces a THD of 5%, which is the maximum allowable limit, and the utility is disconnected causing an island condition. If our load is purely resistive, the THD measured will also be 5%, preventing the inverter from tripping. Also, if the load is an *RLC* load, the low-pass characteristics of the load will attenuate the higher order harmonics, causing the THD to drop, which will definitely not trip the inverter. Lastly, using the HD method, the inverter is very susceptible to nuisance tripping in the event of transient voltage disturbance, such as the switching of capacitor banks that will momentarily increase the THD.

It can be seen that the passive methods alone are not suitable for implementation into the utility interactive inverter. Let us now explore a few active detection methods that may provide proper anti-islanding mechanisms.

Active Detection of Islanding

Active detection methods for the prevention of islanding rely upon the use of a microcontroller based inverter, along with some passive detection techniques. Microcontrollers allow engineers and designers to incorporate sophisticated control schemes in their designs. The premise behind active methods of islanding detection is to generate small perturbations of one of the system parameters at the inverter output. The systems parameters could be the frequency, harmonics, phase, *P*, or *Q*. This method has created a lot of buzz in the power systems and power electronics communities and has

fueled a steady development of ideas and publications. We will discuss only a couple and will leave the rest to be researched in [16].

The active frequency drift (AFD) method involves the output of a slightly distorted current waveform in the inverter output as shown in Figure 62.

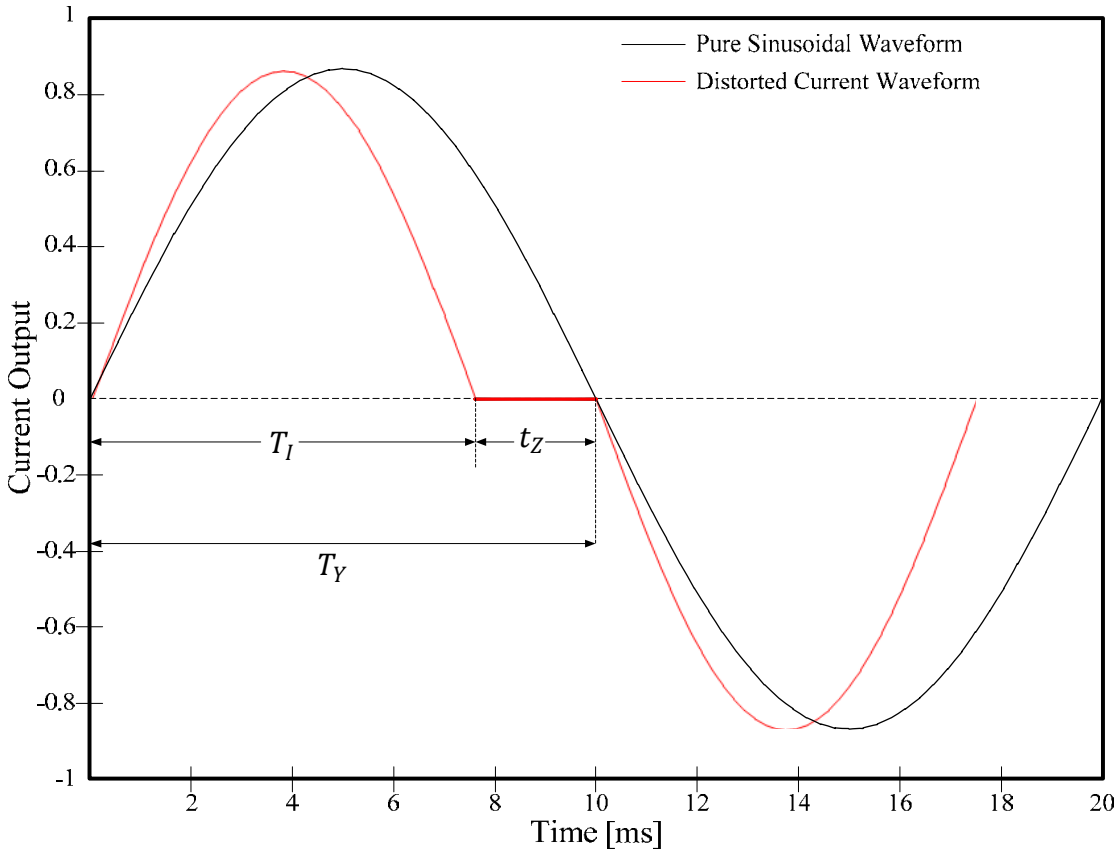


Figure 62 Current waveform using the AFD method

The waveform is distorted by forcing its frequency to be slightly higher than that of the voltage frequency from the previous cycle. Also, once the current waveform reaches zero, it remains at zero until a zero crossing of the voltage waveform, as illustrated by Figure 62. Let us define the following:

$$cf = \frac{2t_z}{T_{Vutil}} = \frac{\delta f}{f + \delta f} \tag{103}$$

$$i^* = \sqrt{2} I \sin[2\pi(f + \delta f)]\, t \tag{104}$$

$$\theta_{AFD} = \pi f t_z = \frac{\pi \delta f}{f + \delta f} \quad (105)$$

The "chopping fraction", cf, is the ratio between the forced frequency change in the current, $\delta f = \pm 0.5 - 1.5 Hz$, compared to the voltage frequency f. The time in which the current waveform is zero is called the zero time and is denoted by t_z. The period of the utility voltage is given by T_{Vutil}. The inverter current reference and angle in the steady state are shown in (104) and (105).

This method creates a phase difference between the voltage and current waveforms. If the inverter remains connected to the utility, the first zero crossing in each cycle of the current waveform directly coincides with that of the voltage, thus not resulting in an OUF condition. However, once the utility reference is removed, and the shifted current is applied to a resistive load, the voltage waveform will tend to that of the current. If the current waveform was distorted with a positive δf, then the voltage waveform would have its zero crossing sooner than in the previous, causing the phase error described above. The inverter will try to counteract this effect by increasing the frequency of the current waveform, thus again causing the first zero crossing of the voltage waveform to appear sooner than expected. As we can see, this drives the frequency of the current waveform ever higher and eventually exceeding the threshold set forth by the OUF protection scheme. It has been shown in [17], however, that the NDZ of this method cannot be reduced to zero and will be dependent upon the quality factor of the LC load (*Q)* and of δf being very close to the OUF-OUV method for high *Q* loads. In addition, if the island consists of multiple inverters and these multiple inverters are not identical (i.e. different manufacturers), a consensus choice would have to be made amongst the manufacturers as to shift the frequency up or down. Otherwise, if one decides to shift up while the other shifts down, they would in effect cancel each other and the islanding condition would not be ceased. Lastly, discontinuous waveforms, such as the one generated by this method, will cause radiated and conducted radio frequency interference (RFI). This would imply that the AFD method is not a viable method for anti-islanding detection.

The slip-mode frequency shift (SMS) method is one of the methods currently discussed that employs a positive feedback of the inverter output voltage. Of the three parameters that positive feedback can be applied to, amplitude, frequency and phase, SMS applies it to the phase, the short term frequency. The frequency of the grid, however, will not be impacted by this feedback. As such, let us define a few equations necessary for this method. The inverter current reference and phase for the SMS method in the steady state are

$$(106) \quad i^* = \sqrt{2}I \sin(2\pi f_{vk-1}\, t + \theta_{SMS})$$

$$(107) \quad \theta_{SMS} = \theta_m \sin\left(\frac{\pi}{2}\right)\frac{f_{ref} - f_{util}}{f_m - f_{util}}$$

where f_{vk-1} is the frequency value from the last cycle of the nominal utility frequency f_{util}, f_m is the frequency at which the maximum phase shift, θ_m, occurs and f_{ref} is the measured frequency. As we can see in (107), the phase shift, θ_{SMS}, is made a function of the frequency, thus obtaining the relationship illustrated in Figure 63. When the utility line is present, it forces the operating point in Figure 63 to be at point 1 by providing a solid frequency and phase reference. However, once the utility is removed and an islanding condition is present, any perturbation away from the utility nominal operating frequency experienced at the output of the inverter will cause a phase shift along the SMS curve shown in Figure 63. Thus, causing the phase error to increase, illustrating the positive feedback characteristic of the SMS method.

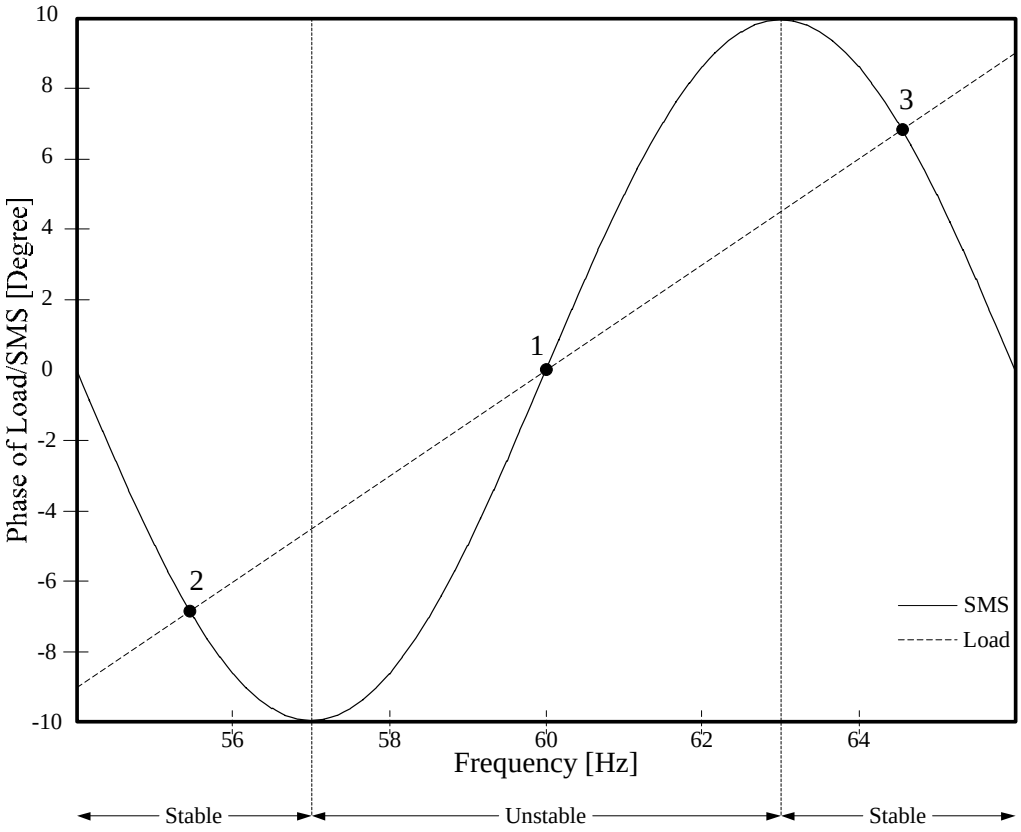


Figure 63 Phase vs Frequency relationship in the SMS method

In an islanding condition, it shown in [17] that for a given quality factor specification, Q_f, θ_m can be accurately calculated using

$$\frac{\theta_m}{f_m - f_{util}} \geq \frac{12Q_f}{\pi^2} \quad (108)$$

where $f_m - f_{util}$ is usually taken to be at 3 Hz so that stable operating points lie outside the normal frequency range. This method is shown to have great advantages over the other methods discussed earlier, and the potential elimination of the NDZ, as shown in [17]. However, as with all positive feedback systems, SMS could potentially cause system-level power quality and transient response problems at very high DG penetration level and high-gains in the feedback loop. Also, as shown in [16], high Q_f loads at resonant frequencies close to the utility operating frequency lie in the NDZ. These loads are rather rare however, and IEEE 1547 has required testing to be done with loads at $Q_f = 1$ for easier compliance.

There are some novel methods that have been recently proposed, such as the GE Voltage Shift, GE Frequency Shift and Wavelet-based detection methods in which the output waveforms are not degraded and can be kept stable, which have a high potential for standardization as they apply in general cases. It is recommended that the reader take advantage of any references that address these and other anti-islanding methods, as their progress is rather swift.

MAXIMUM POWER POINT TRACKING

Introduction

The last, but definitely not the least important operating characteristic of the utility interactive inverter we will discuss is the important maximum power point tracking (MPPT) algorithm. The MPPT algorithm is important in PV systems due to the inherent current-voltage characteristics of PV cells, as shown previously in Figure 6. As such, an efficient inverter must be able to determine the proper operating point at which the maximum power from the PV cells can be extracted, since knowledge of the MPP is not known a priori. This is done by controlling the PV module's current or voltage independently of the load. Another note of importance is that each PV cell has a different MPP and the MPP will surely change depending on the temperature of the cell, as shown earlier. We will discuss the most popular MPPT algorithms that do not involve a high cost to implement. There are other algorithms that have been proposed based on digital signal processors (DSP) and fuzzy logic, however these have been excluded as the cost of their commercial implementation makes them impractical at this moment.

Perturb and Observe

The perturb and observe (P&O) is by far the most widely used MPPT algorithm in commercial inverters today, mainly due to the fact that it is fairly easy and cheap to incorporate in an inverter system. The idea behind the P&O algorithm is rather elementary; the voltage at the converter stage of the inverter (DC-DC stage) is incremented by a small amount. The resulting change in power, ΔP, is measured. If $\Delta P$is measured to be positive, then the voltage is incremented once again, following the logic that an increase in voltage resulted in a move toward the MPP. If ΔP is measured to be negative, thus moving away from the MPP, then the voltage is decremented to try and reach back to the MPP.

The P&O algorithm has some disadvantages that reduce its MPP efficiency. One of these disadvantages is that the algorithm finds it difficult to discern the MPP when the irradiance is reduced, thus flattening out the *P-V* curve and making it difficult for the algorithm to detect the small changes in the power, as shown in Figure 64, for G=200. We can also determine from the aforementioned logic that this algorithm cannot determine the exact MPP, but rather it oscillates around the point. We can also see in Figure 65 that this algorithm behaves erratically during instances of rapid changes in irradiance, such as those experienced during partly cloudy days. As the irradiance rapidly changes (i.e. from curve 1 to 3), the current point of the algorithm moves further

and further away from the new MPP, that moves from point A to D to G instead of A to E to H.

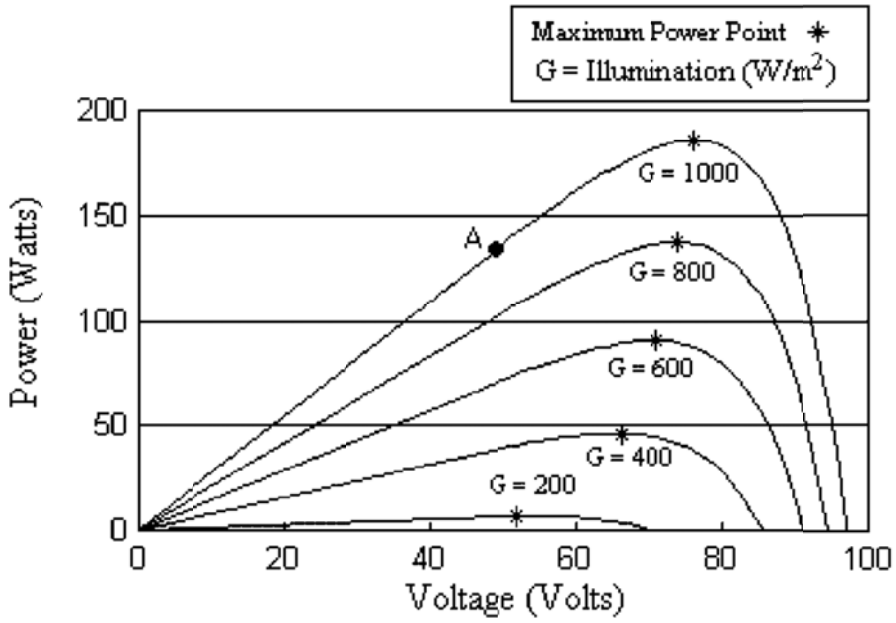


Figure 64 Photovoltaic array power-voltage relationship [18]

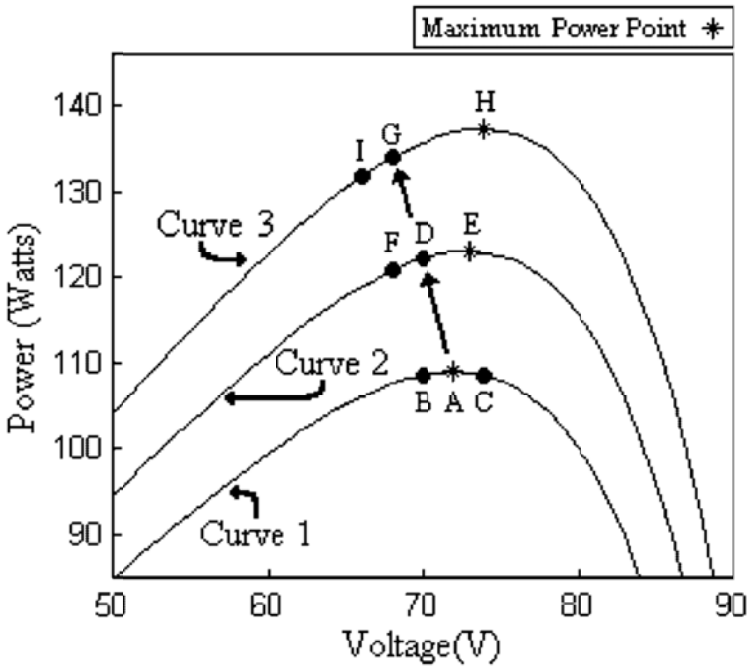


Figure 65 Erratic behavior of P&O under rapidly increasing irradiance [18]

There have been propositions of optimization of the P&O, such as the one shown in [19] and others. However, even without these optimizations, the P&O was shown to have an overall MPPT efficiency of 99.3%, as shown in [18].

Constant Voltage

The concept behind the constant voltage and current (CV) method is the observation that the ratio of the PV array's maximum power point voltage, V_{MP}, to its open circuit voltage, V_{OC}, is approximately constant, as seen in Figure 6 and is described by

$$\frac{V_{MP}}{V_{OC}} \cong K < 1 \quad (109)$$

This method can be implemented utilizing the logic depicted by the flowchart shown in Figure 66. The PV array is momentarily disconnected from the system and a measurement of the open circuit voltage is taken. Utilizing this measurement of V_{OC} and a predetermined value of *K*, the algorithm calculates the maximum power point voltage using equation (109) and sets the system to that voltage. This is constantly repeated over the course of the inverter's operation to constantly calculate the MPP voltage at different times.

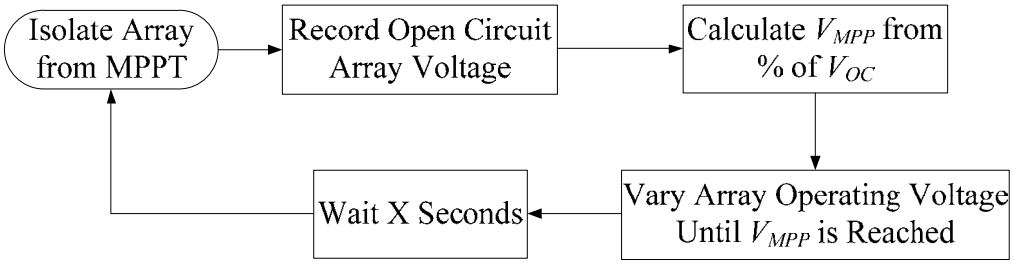


Figure 66 Perturb & Observe (P&O) MPPT algorithm

This poses a serious problem of inverter output efficiency as the algorithm must disconnect its input source periodically to make this calculation, which obviously significantly reduces the inverter's efficiency. Also, it is shown in [18] and other sources that the value of *K* is not in fact constant and its use would not be practical in an MPPT algorithm.

Pilot Cell

This method works under the same principal as the CV method with one main difference being that the open circuit voltage measurement is taken from a separate solar cell, called

a pilot cell. This eliminates the need to disrupt the power output of the inverter to take measurements, thus increasing its efficiency. However, the problem of determining the correct value of *K* is still present. Also, and more importantly, it is essential that the pilot cell's characteristics be precisely matched with those of the array or module, otherwise the measurements made will be of no value. This will require that each pilot/array pair be calibrated, increasing the energy cost of the system significantly. Thus, this is not a popular choice in the commercial market.

Incremental Conductance

The incremental conductance (IC) method is based on the assumption that the MPP can be calculated by taking the first derivative of the PV array power with respect to the voltage and setting it equal to zero, as prescribed in [20] and shown below.

$$\frac{dP}{dV} = \frac{d(VI)}{dV} = I + V\frac{dI}{dV} = 0 \tag{110}$$

which gives us

$$-\frac{I}{V} = \frac{dI}{dV} \tag{111}$$

By inspection of (111) we see that the left hand side of the equation denotes the opposite instantaneous conductance of the PV array and the right hand side denotes the incremental conductance (IC). As such, at the MPP, the instantaneous conductance and the incremental conductance must be equal in magnitude but opposite in sign. We can correlate this finding in (111) to a set of inequalities that will be the heart of the logic behind this algorithm as follows:

$$-\frac{I}{V} = \frac{dI}{dV} \quad \text{therefore} \quad \left(\frac{dP}{dV} = 0\right) \tag{112}$$

$$-\frac{I}{V} > \frac{dI}{dV} \quad \text{therefore} \quad \left(\frac{dP}{dV} > 0\right) \tag{113}$$

$$-\frac{I}{V} < \frac{dI}{dV} \quad \text{therefore} \quad \left(\frac{dP}{dV} < 0\right) \tag{114}$$

Equations (112) – (114) lead to the following logic diagram in Figure 67. This method is very similar to that of the P&O method with two distinct advantages, it can calculate which direction to perturb the voltage and can actually find and remain at the MPP.

However, this is at the cost of higher computational requirements, which may degrade the overall system performance. One could make the inference that the IC method would increase the overall MPPT efficiency as compared to the P&O method. However, it is shown in [18] that the overall MPPT efficiency of the IC method was 99.4%, not much of a difference from the P&O method. Thus, the P&O method is the preferred choice of MPPT algorithms amongst inverter manufacturers due to its simplicity and low cost of implementation.

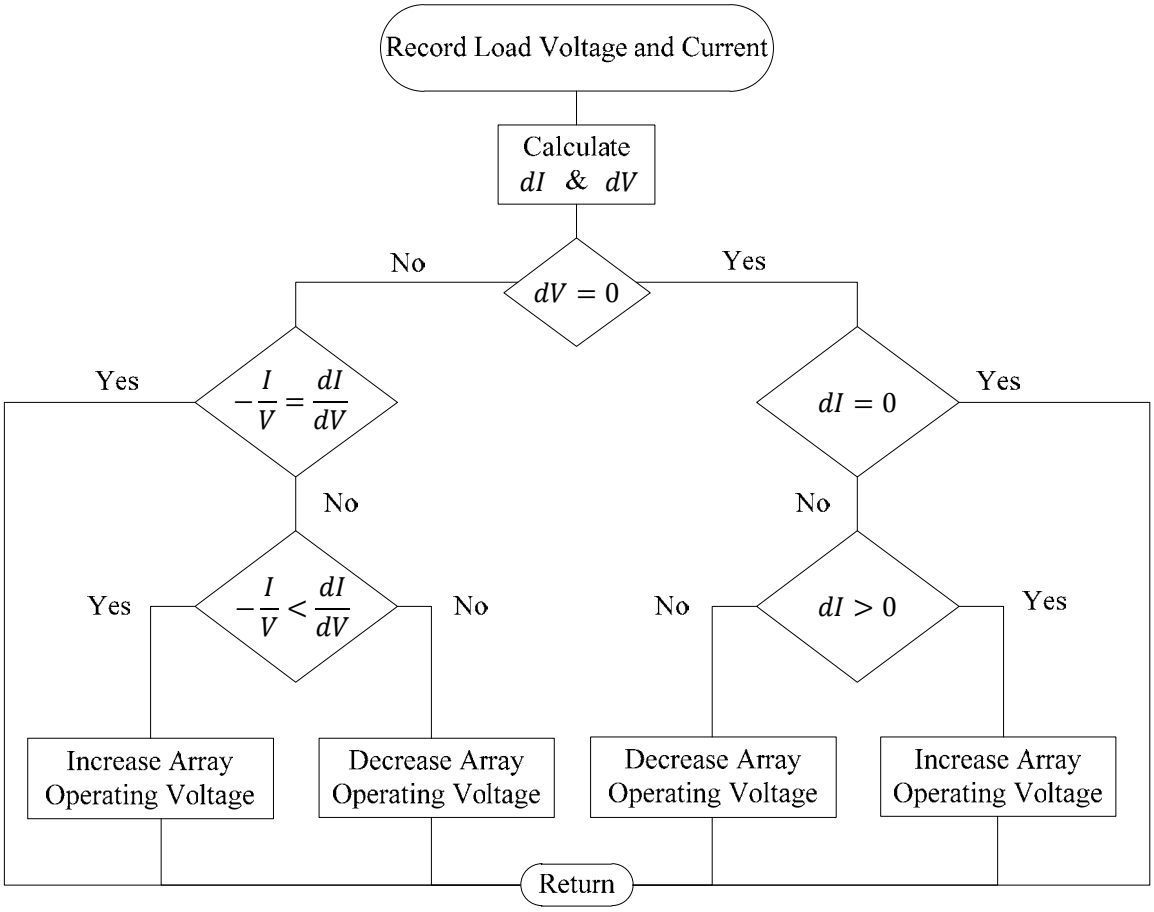


Figure 67 Incremental Conductance (IC) MPPT algorithm

Model Based Algorithms

Model based MPPT algorithms rely on the premise that values in equation (4) are precisely known. Therefore, all the MPP operating points can be calculated directly and thus applied to the system. This method, however, is not practical as the characteristic parameters of each solar cell cannot be precisely measured and the cost of purchasing an accurate enough light sensor to determine these parameters would be tremendous.

COMPUTER SIMULATIONS

Photovoltaic Array

As with all engineering work, theoretical findings must be determined to be either correct or incorrect. The first step in such a process is the implementation of computer simulations to determine the validity of the theoretical results and findings of this project. MATLAB®/Simulink® software suite by Mathworks® is utilized to facilitate the modeling and simulation of the various aspects of our complete inverter system. Throughout this section, figures will be presented in a tier fashion and may seem redundant, but are however required due to the modular nature MATLAB/Simulink. This is evident in the design of certain control blocks, such as the SOGI-FLL, in which at the top level shows just a control block, but exposing each underlying tier gives rise to the nature of that block. Therefore, when describing a certain aspect of the model, we will first display the top level block and work our way deeper. First we will begin with the modeling and simulation of a 2kW photovoltaic array based on equation [4] and ten series connected modules from [7]. However, for simplicity, a single diode model was employed but with a series and parallel resistance in order to exhibit a more characteristic response of a practical photovoltaic cell/module/array. The equation is as follows:

$$I = I_{pv} - I_d - I_{R_p} \tag{115}$$

where I_{pv} is the photovoltaic current, I_d is the diode current and I_{R_p} is the current flowing through the parallel resistance. Their equations are as follows:

$$I_{pv} = \left(I_{pv,n} + K_I(T_{cell} - T_n)\right)\frac{G}{G_n} \tag{116}$$

$$I_d = I_o\left[exp\left(\frac{V + R_s I}{V_t N}\right) - 1\right] \tag{117}$$

$$I_{Rp} = \frac{V + R_s I}{R_p} \tag{118}$$

I_o is the diode saturation current and is expressed as

$$I_o = \frac{I_{sc,n} + K_I(T_{cell} - T_n)}{exp\left(\left(V_{oc,n} + K_V(T_{cell} - T_n)\right)/NV_t\right) - 1} \tag{119}$$

V_t is the thermal voltage and is expressed as

$$V_t = N_s k T_{cell}/q \quad (120)$$

where N_s is the number of cells connected in series.

Using the information provided in [7] and an iterative shown in [21], the parameters in equations (116) through (120) are described and quantified in Table 7 below for a 2kW, 500 series cell, photovoltaic array.

Parameter	Description	Value
$I_{pv,n}$	Light generated current at STC (1kW/m^2, 25 °C)	8.6 A
$I_{sc,n}$	Short circuit current at STC	8.6 A
$V_{oc,n}$	Nominal open circuit voltage at STC	308 V
I_{mp}	Current at maximum power point at STC	8.07 A
V_{mp}	Voltage at maximum power point at STC	248 V
P_{mp}	Maximum power at STC	2001.36 W
T_n	Nominal cell temperature used for STC	298.15 K
T_{cell}	Array temperature	Varies
G	Irradiance on array	Varies
G_n	Nominal irradiance used for STC	1 kW/m^2
K_I	Current-Temperature coefficient	.00881567 A/K
K_V	Voltage-Temperature coefficient	-0.1973275 V/K
R_s	Internal series resistance	1.6733 Ω
R_p	Internal parallel resistance	1 x 10^6 Ω
N	Diode quality factor (1 ≤ N ≤ 2) (1 = Ideal)	1.3
N_s	Equivalent number of PV cells connected in series	500
k	Boltzmann Constant	1.3806503x10^{-23} J/K
q	Fundamental electron charge	1.6021765x10^{-19} C

Table 7 Calculated model parameters of a photovoltaic array using Mitsubishi 200W modules from [7]

Utilizing these parameters and their values, the following model shown in Figure 68 - 72 was created and a series of simulations were run to determine if the characteristics of the PV array we modeled behave as expected. The two main characteristics important in photovoltaic cells are the current to voltage and power to voltage relationships. If our model and simulation implementation is correct, we should expect to see a current-voltage response similar to that of Figure 6. Figures 73 - 76 are plots of the current-voltage and power-voltage waveforms from the simulation runs, first by keeping the operating temperature constant and varying the irradiance and last by keeping the irradiance constant and varying the operating temperature.

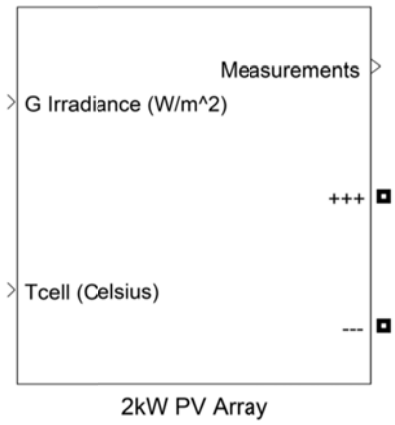


Figure 68 2kW Photovoltaic Array control block

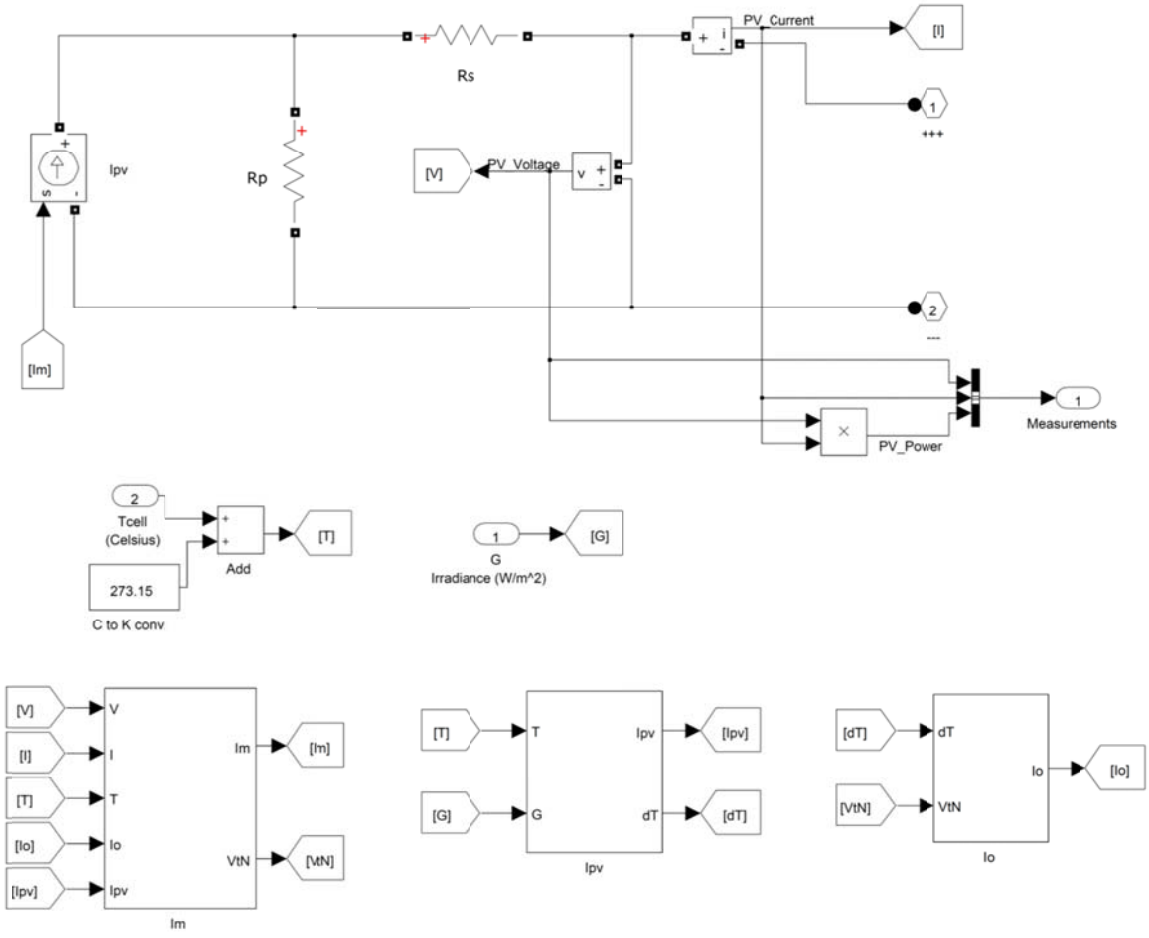


Figure 69 2kW Photovoltaic Array equivalent circuit and model

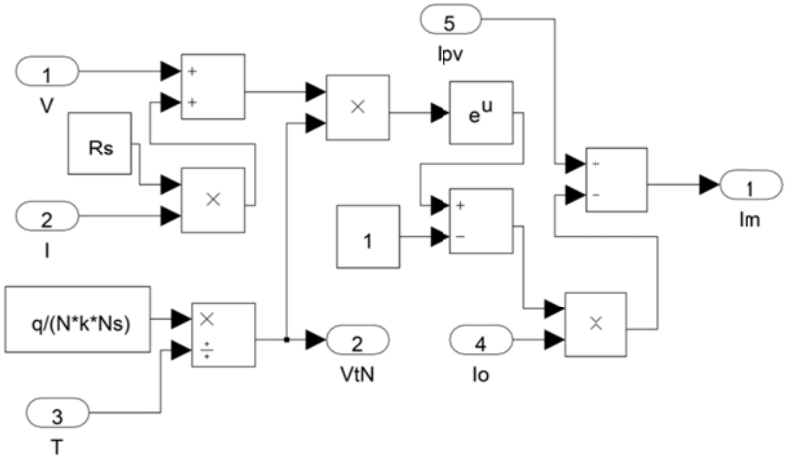


Figure 70 I_m block equivalent model

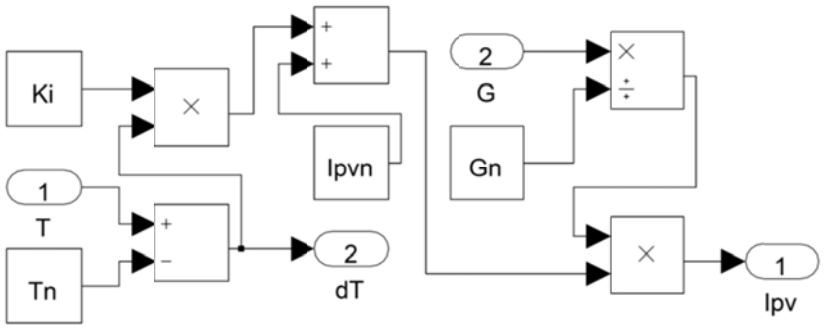


Figure 71 I_{pv} block equivalent model

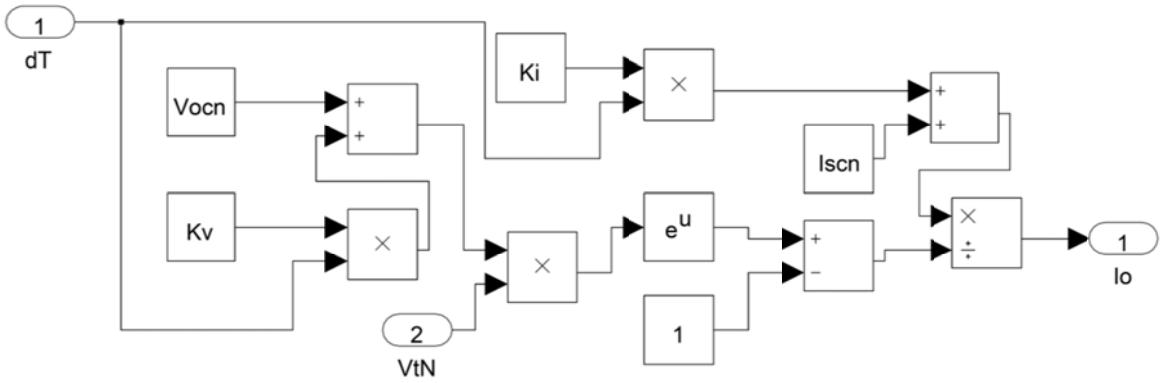


Figure 72 I_o block equivalent model

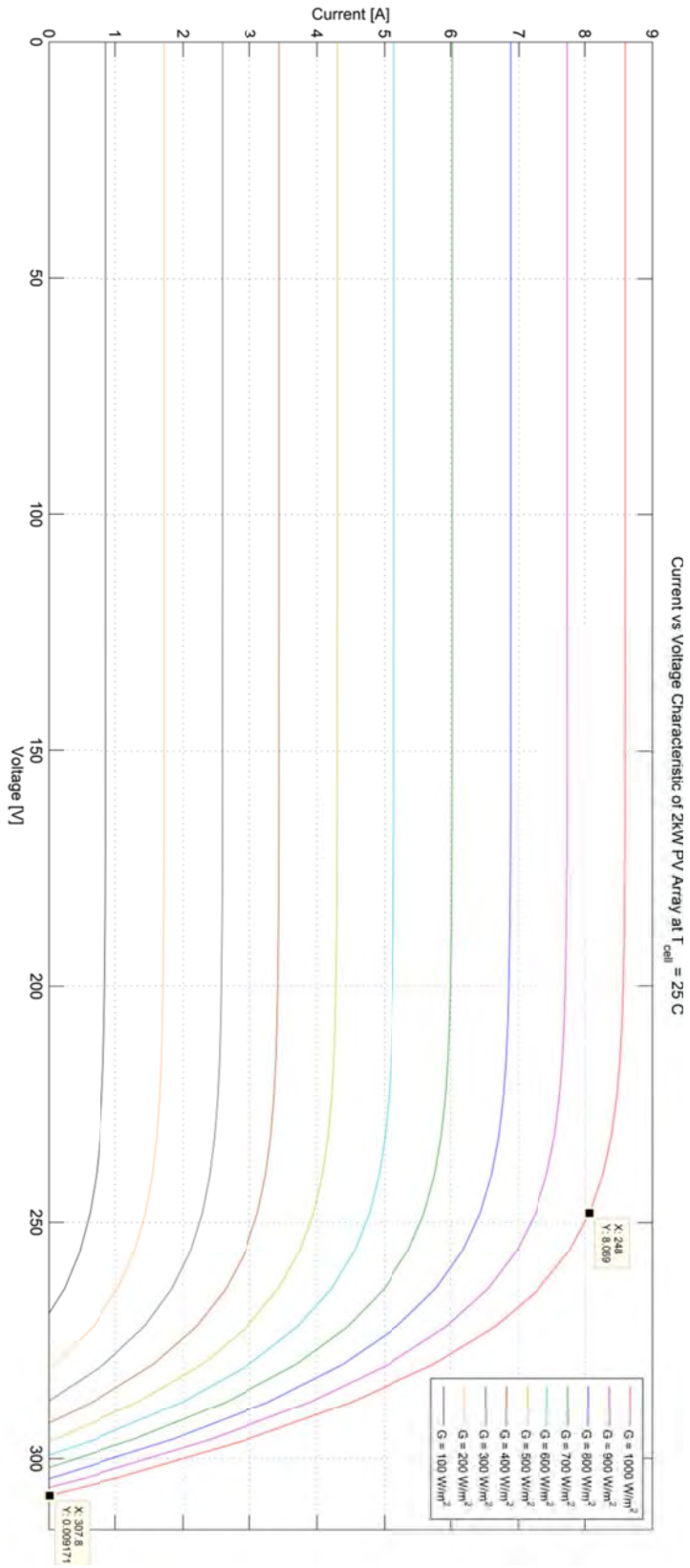


Figure 73 Current vs Voltage characteristic plot of 2kW PV array at varying G and T_{cell} = 25 °C

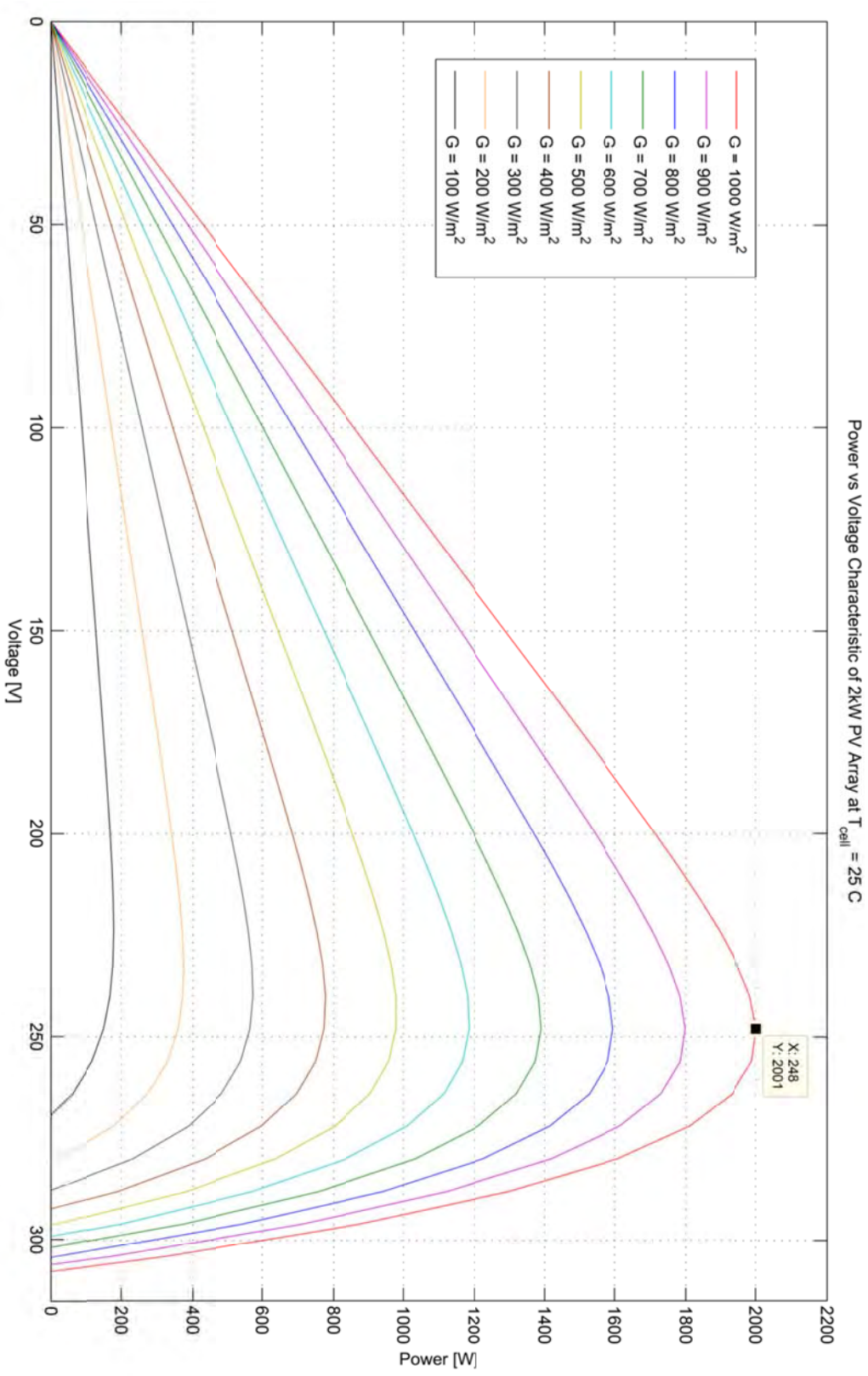


Figure 74 Power vs Voltage characteristic plot of 2kW PV array at varying G and T_{cell} = 25 °C

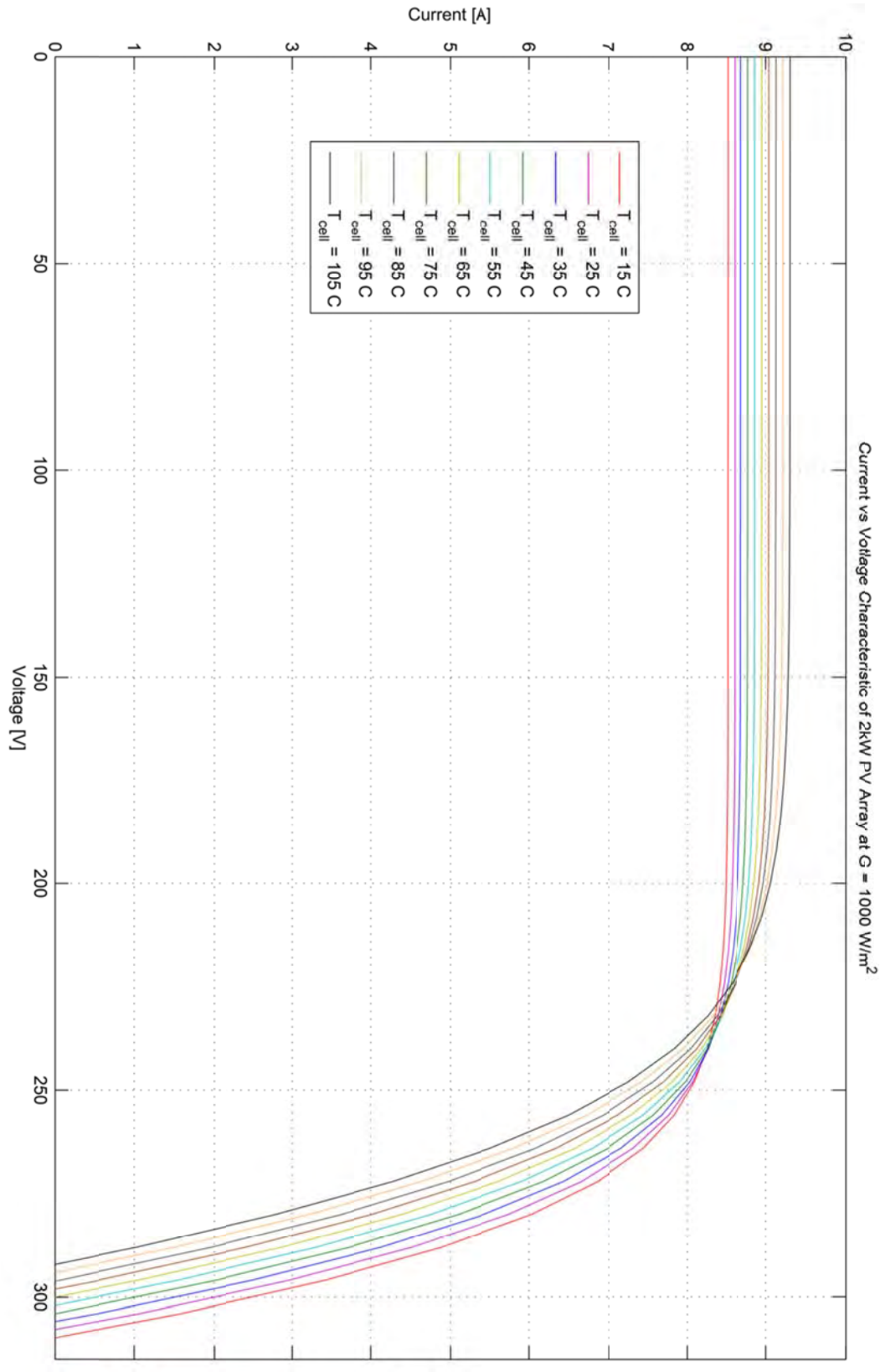


Figure 75 Current vs Voltage characteristic plot of 2kW PV array at G = 1kW/M^2 and varying T_{cell}

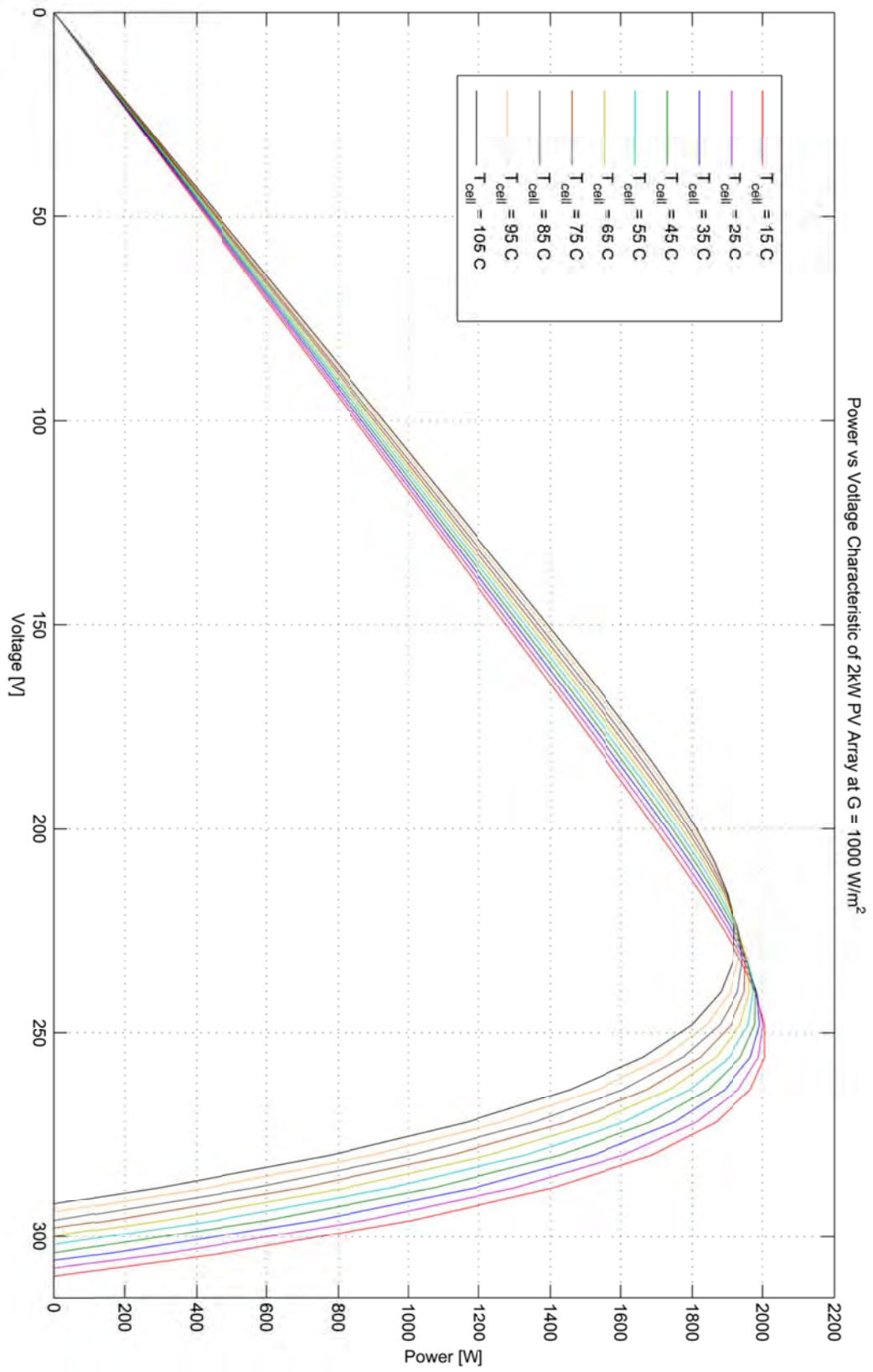


Figure 76 Power vs Voltage characteristic plot of 2kW PV array at G = 1kW/M^2 and varying T_{cell}

As we can see from the current-voltage plots obtained from the simulation, they match very closely to that of Figure 6 and the values at the maximum power point of Table 7, justifying the mathematical model employed. Secondly, we can clearly see a relationship between the irradiance and the maximum output current of the PV array; as the irradiance, or sunlight, on the array drops, so does the operating current and thus maximum power. We can also gather from the power-voltage plots that the maximum power point for each curve lies on the knee of the current-voltage curve, previously shown in Figure 6 as well.

Moving on to the constant irradiance plots we see an interesting relationship between the operating temperature and the maximum output current/power; as the operating temperature of the array rises, the maximum output current/power drops. This can be attributed to the internal series resistance characteristic of the photovoltaic cell, as temperature rises, so does the resistance, thus hindering the flow of current.

These plots have proven that the mathematical model utilized is sound and behaves as expected. This shows also that indeed each photovoltaic element has a maximum power point that varies depending on the irradiance from the sun, the temperature of the array and the load that it is feeding. Thus, the next step would be to implement a MPPT algorithm to dynamically adjust the output conditions of the PV array so that the maximum amount of power can be drawn from the PV source.

MPPT Implementation and Buck Converter Design

In order to implement a MPPT algorithm in our system, we must be able to vary the output voltage of the PV array. This is accomplished through DC-DC converters. Although the topic of DC-DC conversion was not discussed in this project, the reader may turn to [8], [22-24] for theoretical justification and practical implementation. Let us first begin with the implementation of the maximum power point tracking algorithm.

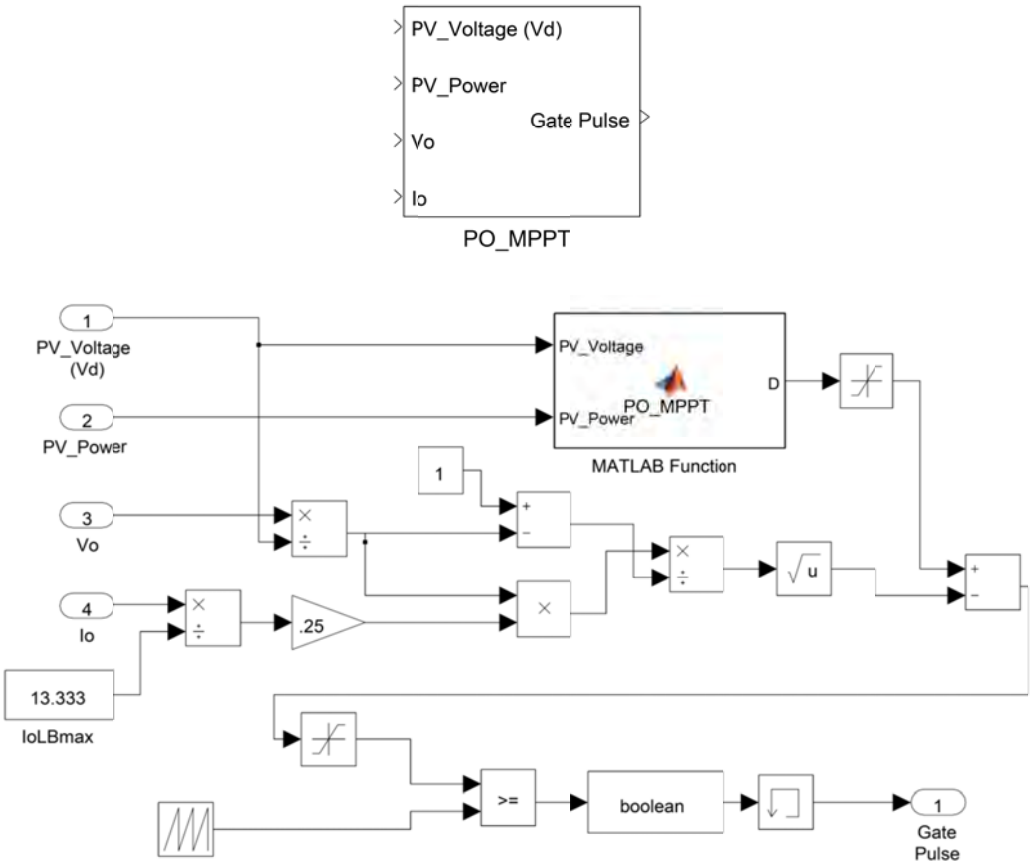


Figure 77 MPPT Control block and equivalent circuit

The MPPT algorithm chosen for our inverter system is the perturb and observe (P&O) method, due to its ease of implementation and accuracy as established previously. The easiest way to implement this algorithm is by use of a Simulink® function block that allows the user to run a MATLAB® script within the simulation, as shown in Figure 78.

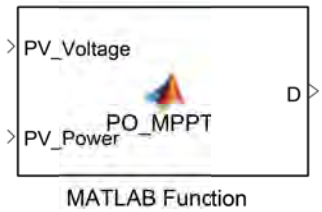


Figure 78 MATLAB® script control block

Two other methods can be used to implement the MPPT such as the Stateflow® toolset in MATLAB® or by implementing a mathematical equivalent model. Due to its ease of use and troubleshooting capabilities, a MATLAB® script was utilized. The complete script is inserted here for reference:

```
function D = PO_MPPT(PV_Voltage, PV_Power)

persistent Dprev Vprev Pprev count

if isempty(Dprev)
    Dprev = .4;
    Vprev = 0;
    Pprev = 0;
    count = 0;
end

deltaD = .000035;

if count >= 1

    D = Dprev;
    dV = PV_Voltage - Vprev;
    dP = PV_Power - Pprev;

        if dP >= -1 && dP <= 1
            D = Dprev;
            Vprev = PV_Voltage;
            Pprev = PV_Power;
            count = 0;
        end

        if dP > 1 && dV > 0
            D = Dprev - deltaD;
            Vprev = PV_Voltage;
            Pprev = PV_Power;
            Dprev = D;
            count = 0;
        end

        if dP > 1 && dV < 0
            D = Dprev + deltaD;
            Vprev = PV_Voltage;
            Pprev = PV_Power;
            Dprev = D;
            count = 0;
        end

        if dP < -1 && dV > 0
            D = Dprev + deltaD;
            Vprev = PV_Voltage;
            Pprev = PV_Power;
            Dprev = D;
            count = 0;
        end

        if dP < -1 && dV < 0
            D = Dprev - deltaD;
            Vprev = PV_Voltage;
```

```
            Pprev = PV_Power;
            Dprev = D;
            count = 0;
        end
else
    D = Dprev;
    count = count + .05;
end
```

The output of the algorithm is the desired duty cycle of the gate pulse used to drive the IGBT of the DC-DC converter, in this case a step-down or Buck converter. Thus by varying the duty cycle of the Buck converter, the output voltage is varied in accordance with the P&O algorithm and the maximum power point is reached. The control block and equivalent circuit diagram of the Buck converter are illustrated in Figures 79.

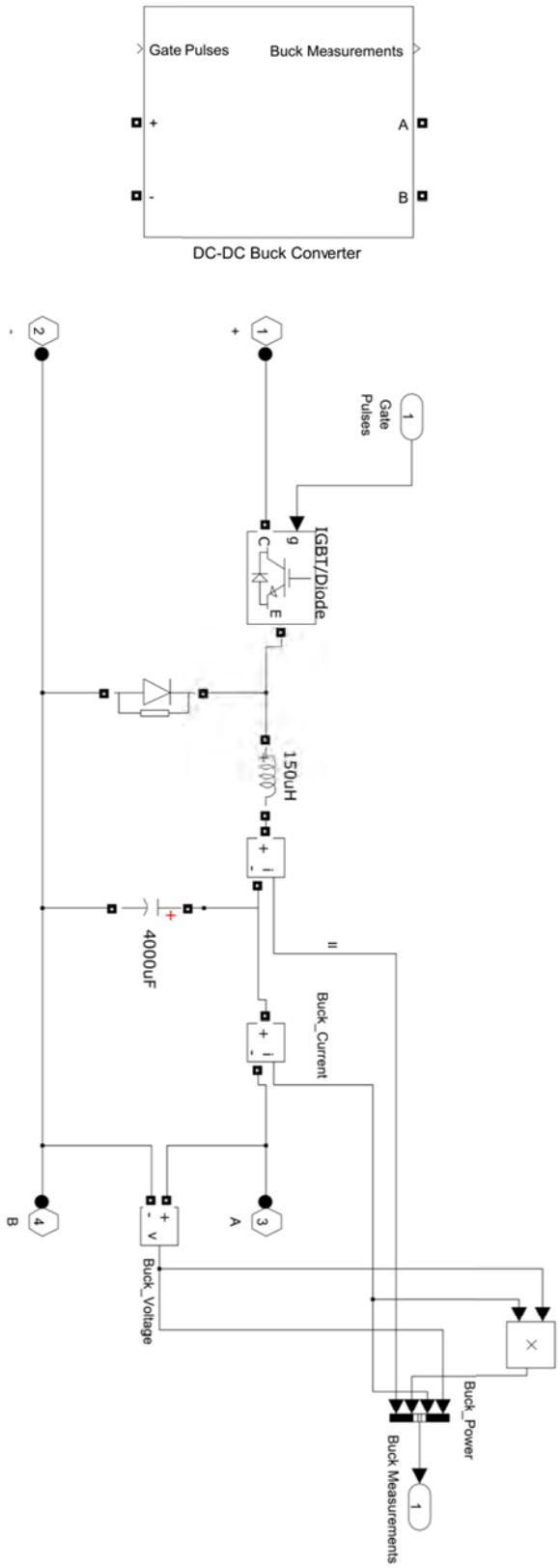


Figure 79 Buck converter control block and equivalent circuit

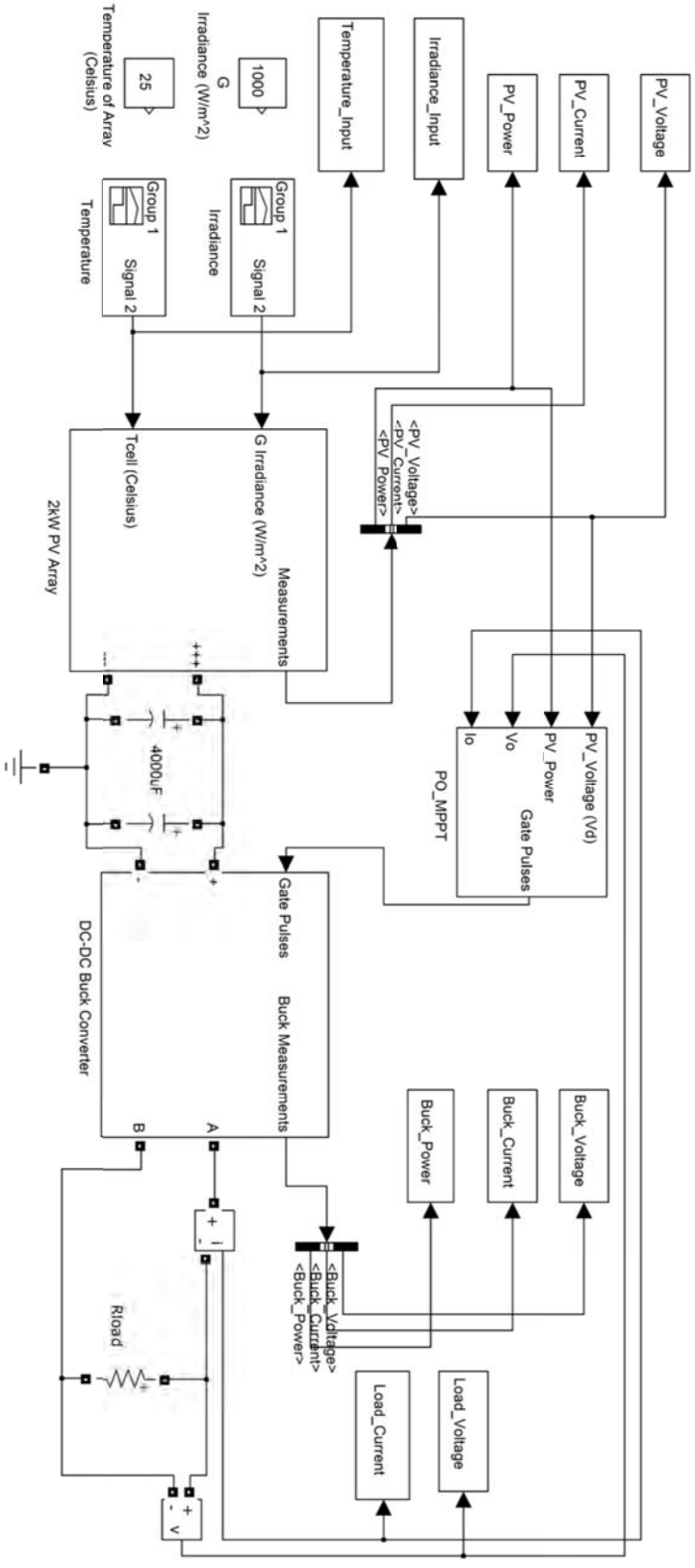


Figure 80 PV Array and Buck converter simulation set-up

Once again, we must determine the accuracy and validity of our design through simulation. This simulation involves the PV array model designed earlier along with the MPPT control block and DC-DC Buck converter block. Four different scenarios are simulated:

1. Constant irradiance and constant temperature
2. Varying irradiance and constant temperature
3. Constant irradiance and varying temperature
4. Varying irradiance and varying temperature

Figure 80 on the previous page illustrates the environment for these four simulations and Figures 81 through 92 are the input and output waveforms. If designed correctly, the output of the Buck converter will adjust accordingly so that the maximum power available from the PV array is delivered to the load.

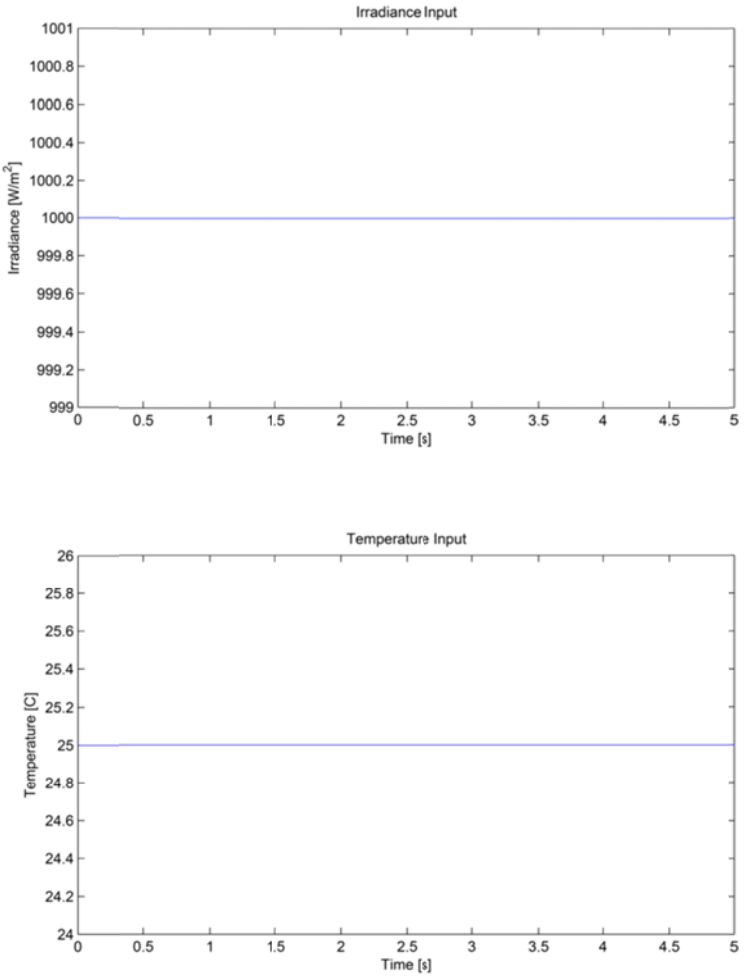


Figure 81 Irradiance and Temperature Input waveforms for constant G, constant T_{cell} simulation

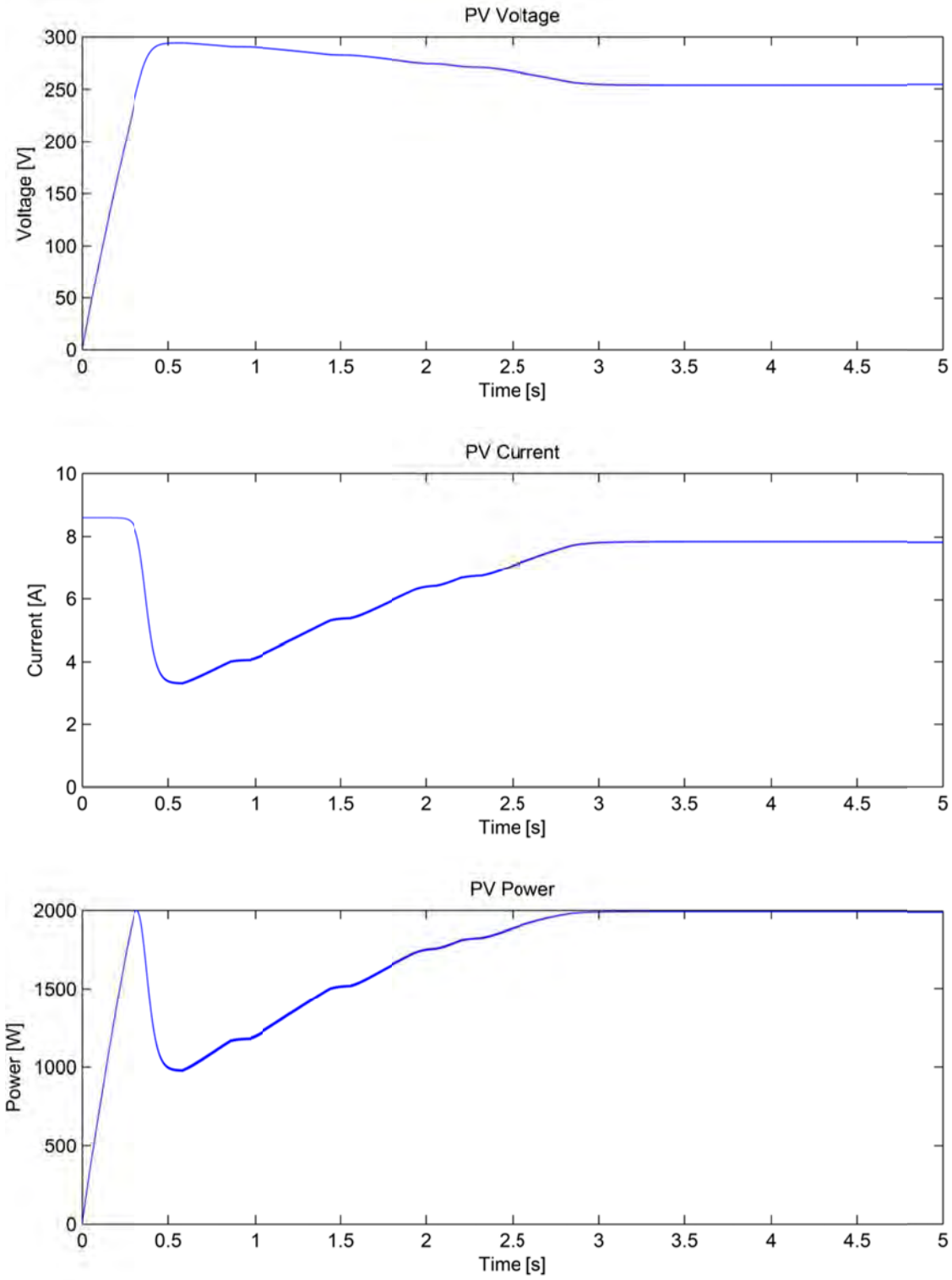


Figure 82 PV output waveforms for constant G, constant T_{cell} simulation

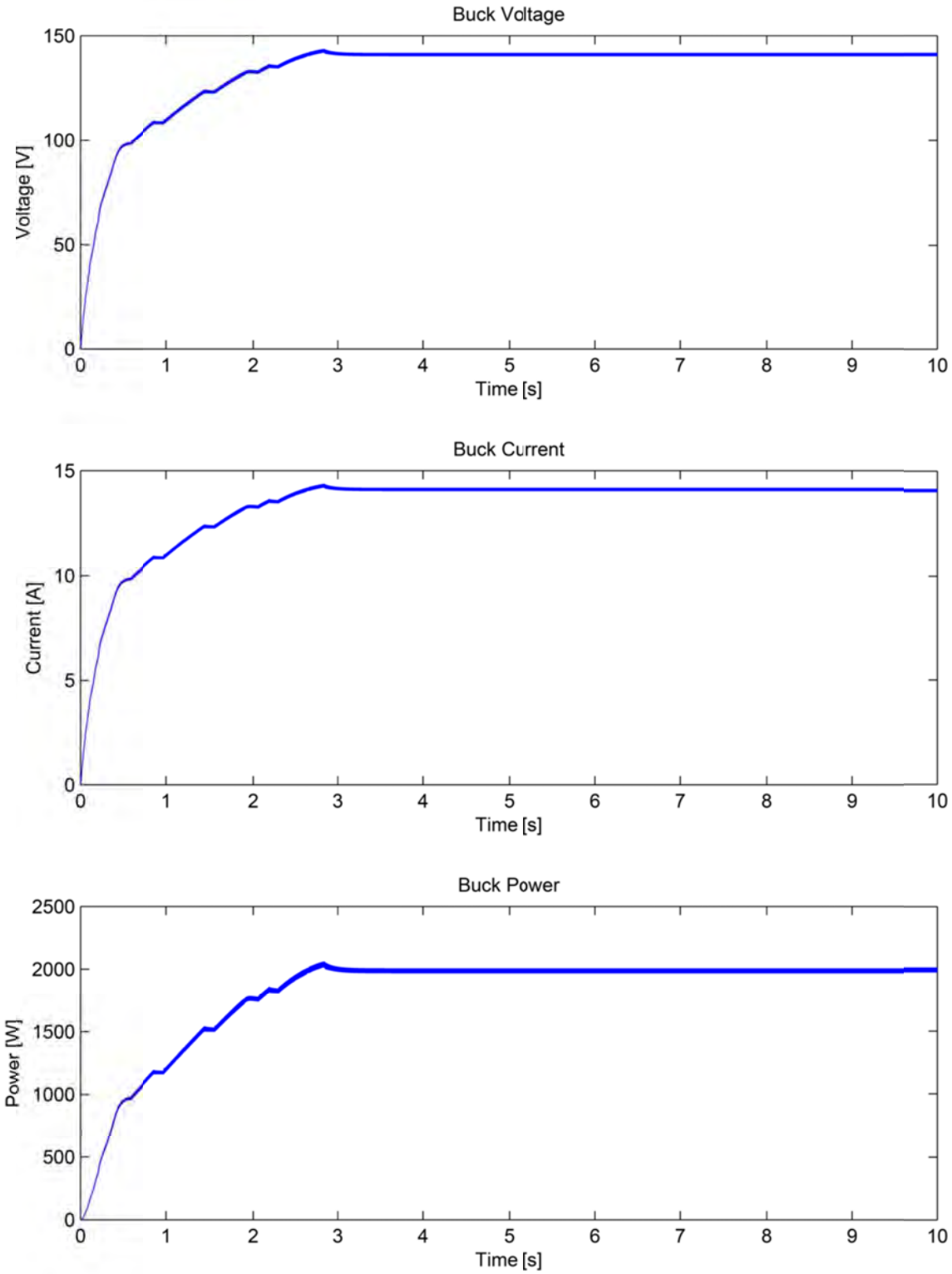


Figure 83 Buck converter output waveforms for constant G, constant T_{cell} simulation

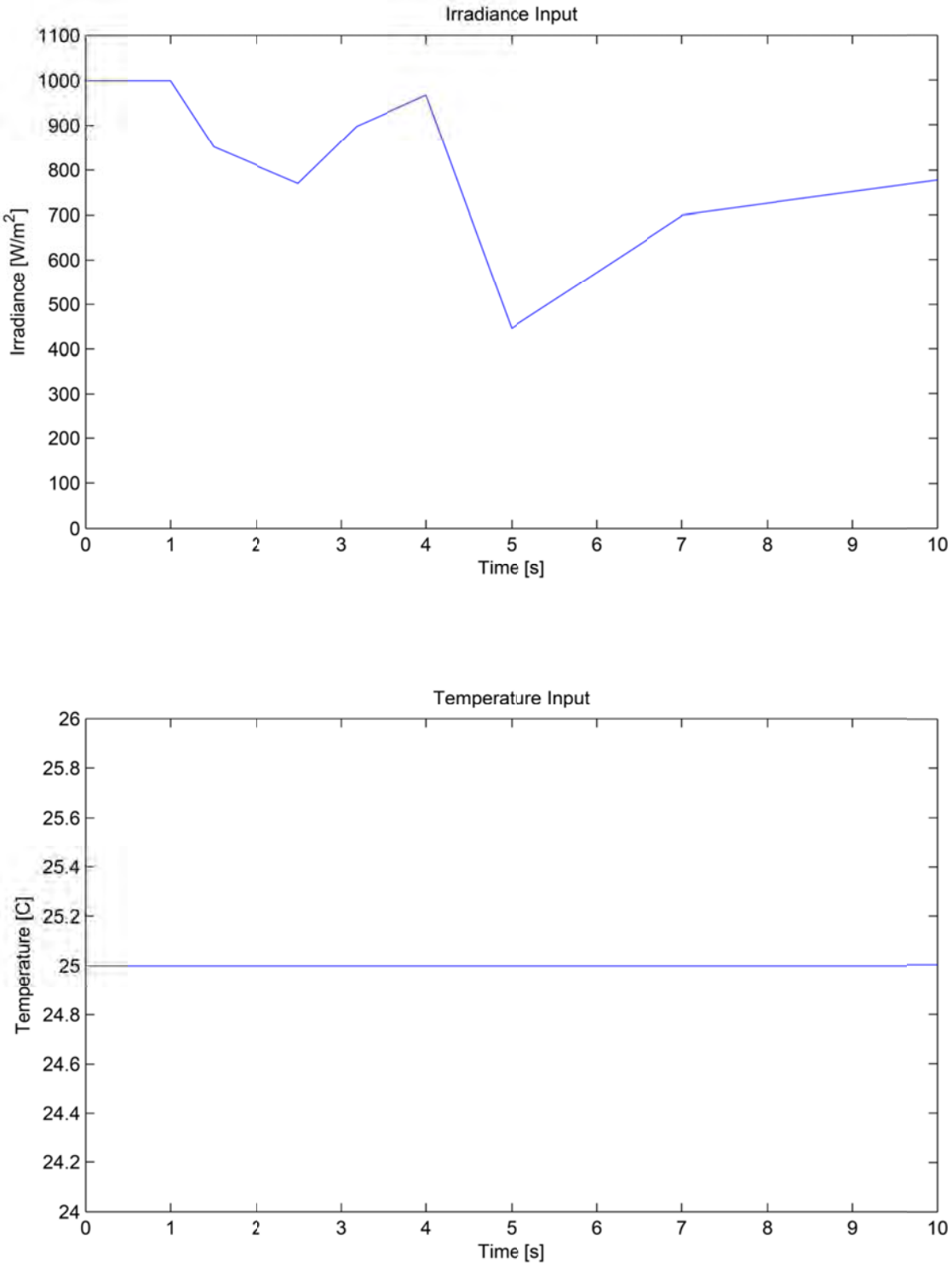


Figure 84 Irradiance and Temperature Input waveforms for varying G, constant T_{cell} simulation

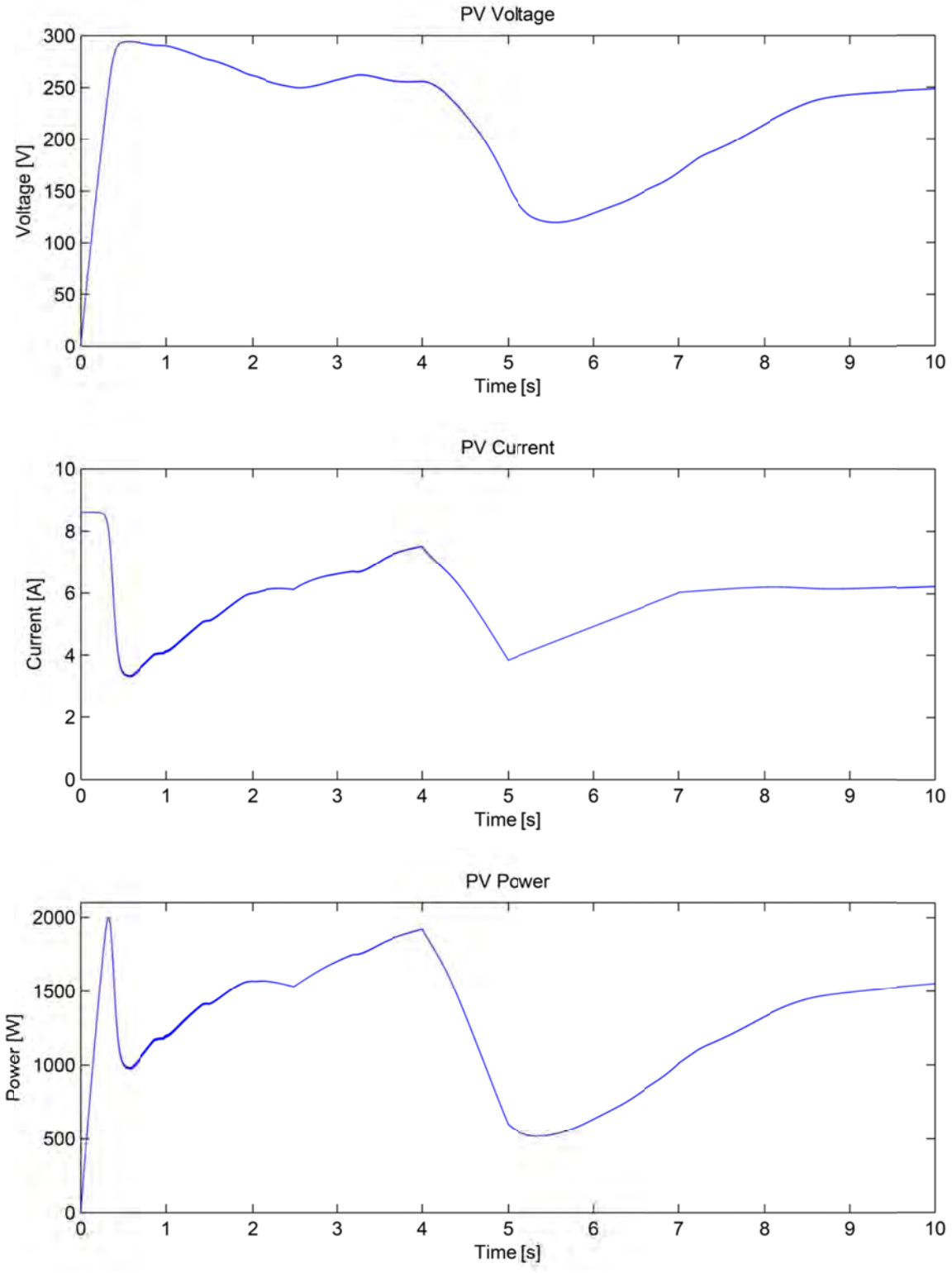


Figure 85 PV output waveforms for varying G, constant T_{cell} simulation

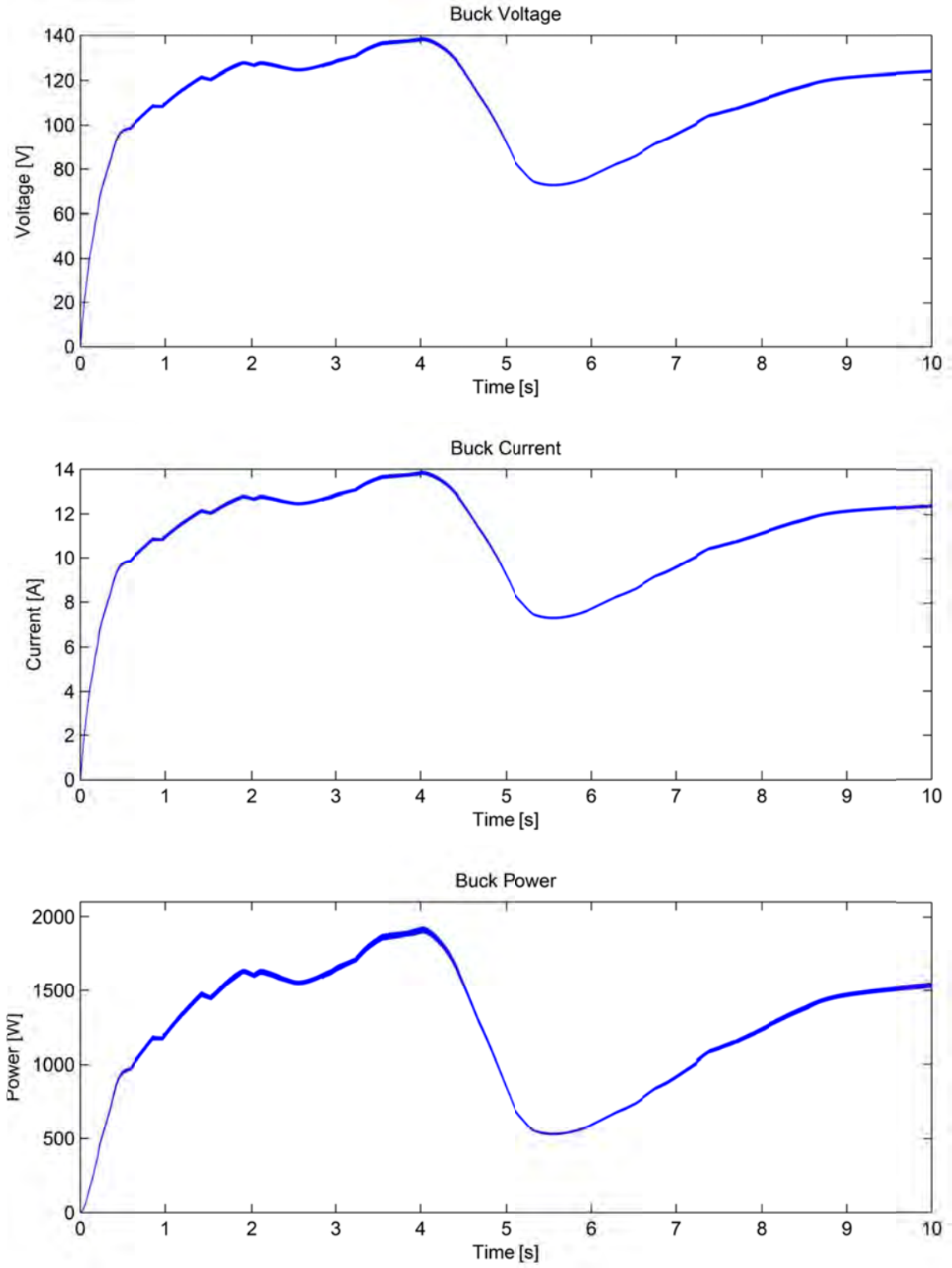


Figure 86 Buck converter output waveforms for varying G, constant T_{cell} simulation

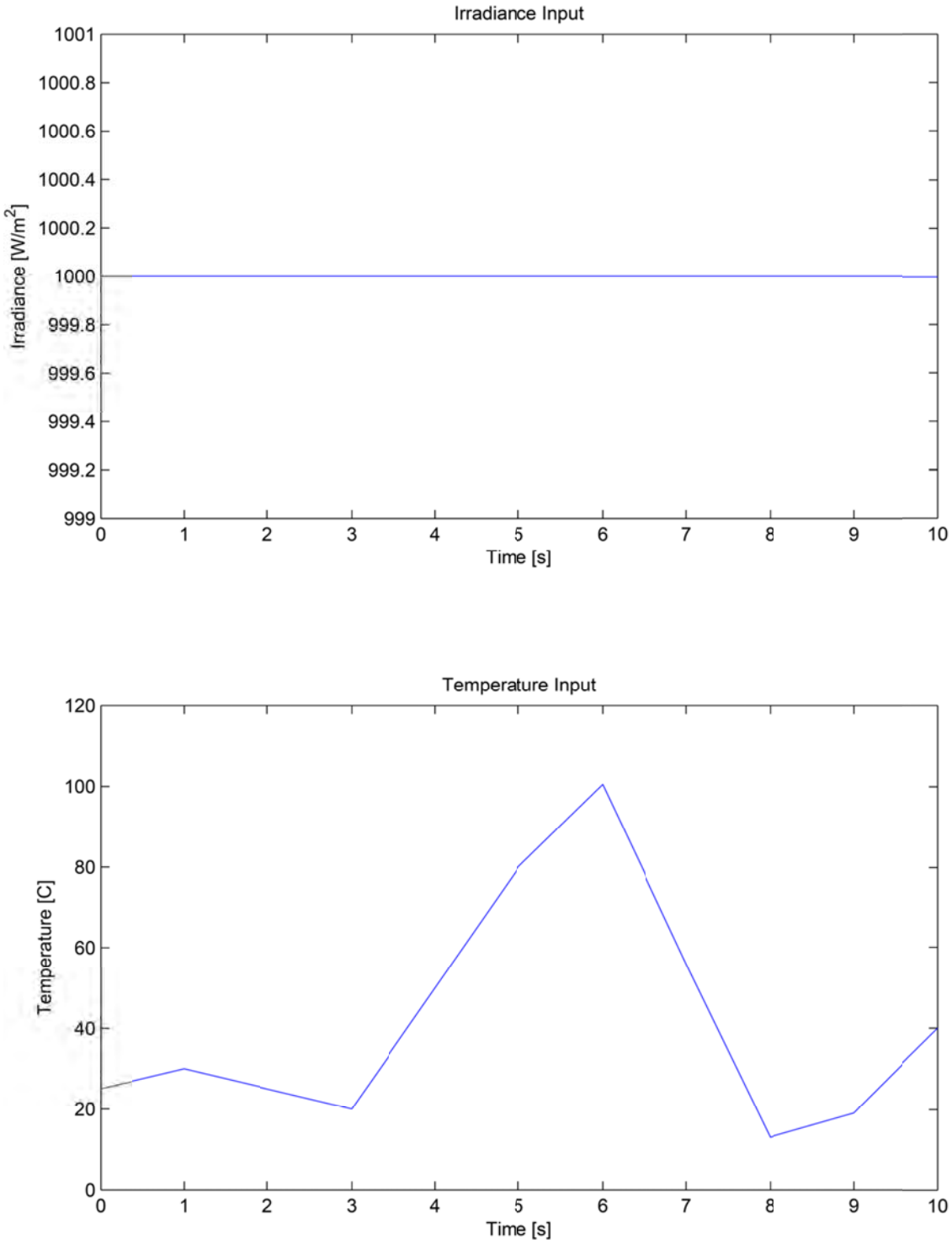


Figure 87 Irradiance and Temperature Input waveforms for constant G, varying T_{cell} simulation

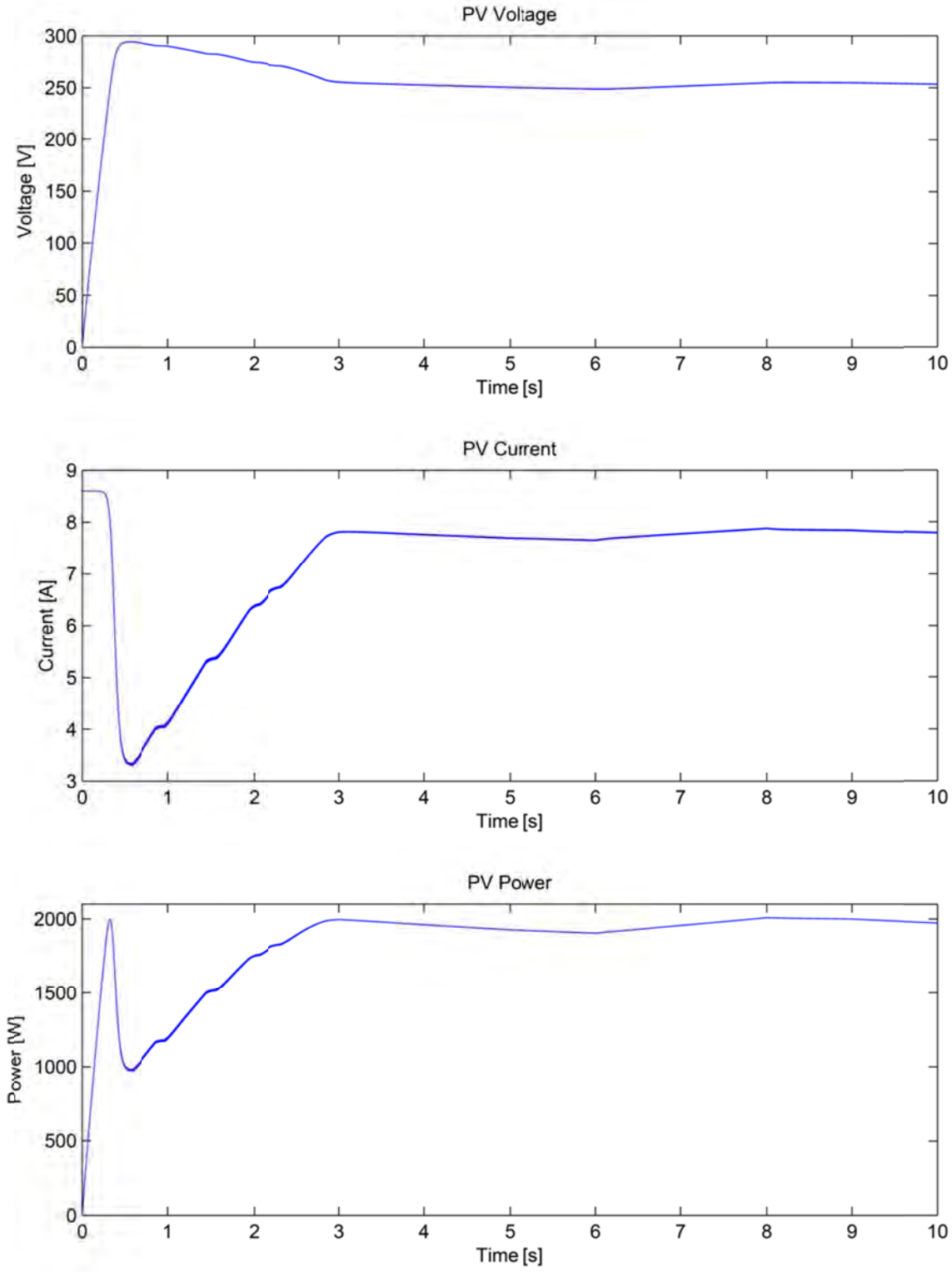


Figure 88 PV output waveforms for constant G, varying T_{cell} simulation

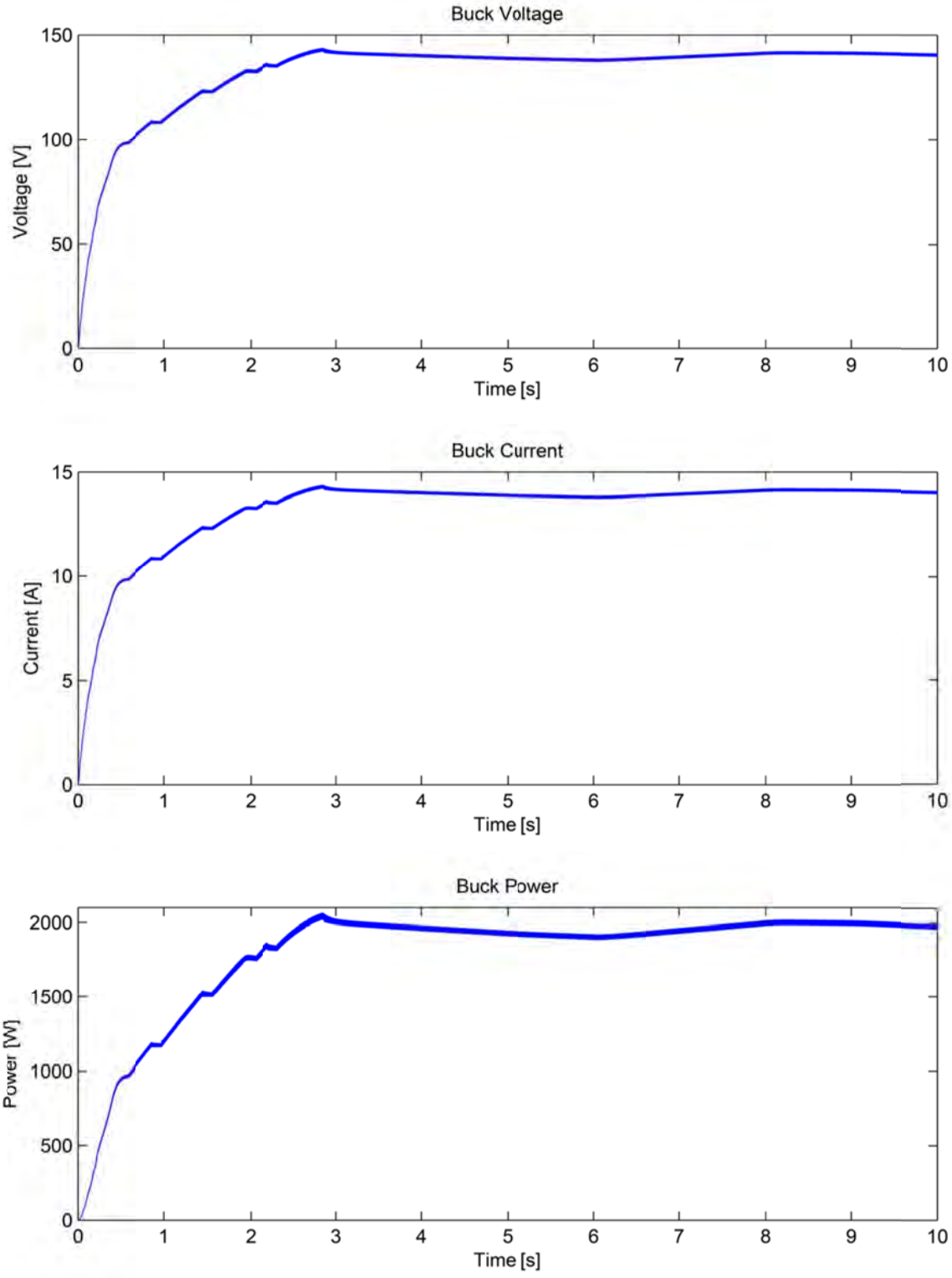


Figure 89 Buck converter output waveforms for constant G, varying T_{cell} simulation

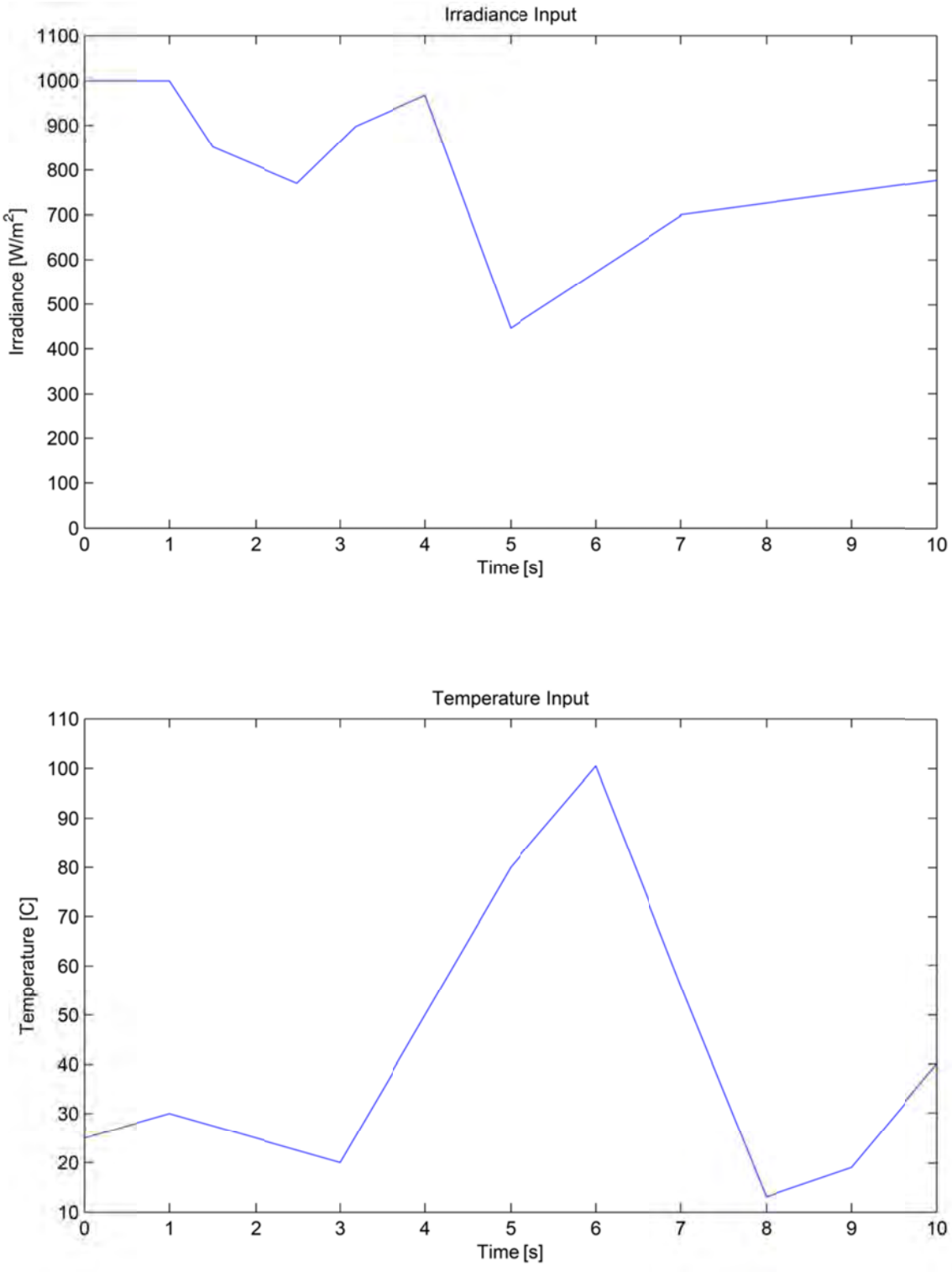


Figure 90 Irradiance and Temperature Input waveforms for varying G, varying T_{cell} simulation

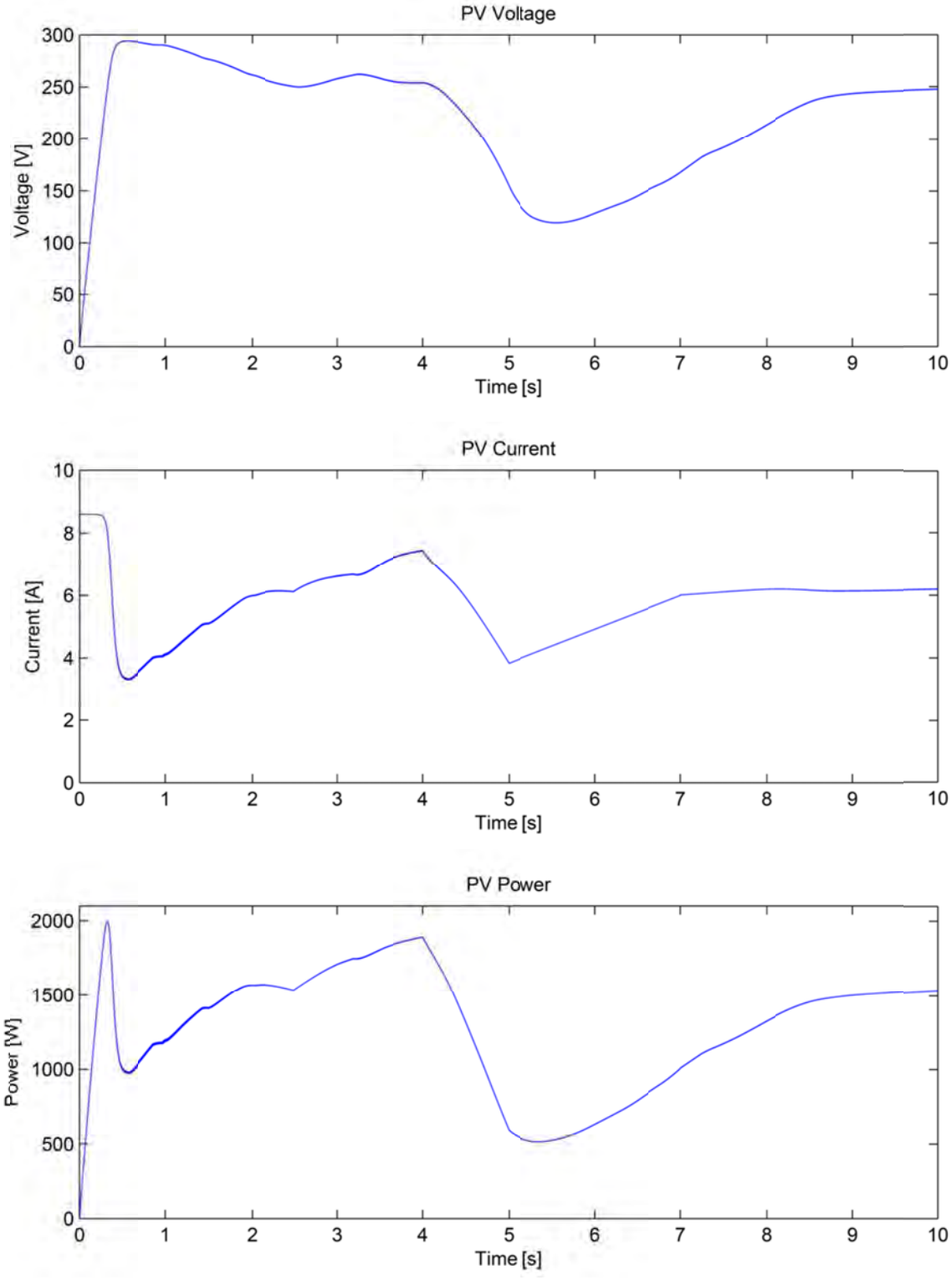


Figure 91 PV output waveforms for varying G, varying T_{cell} simulation

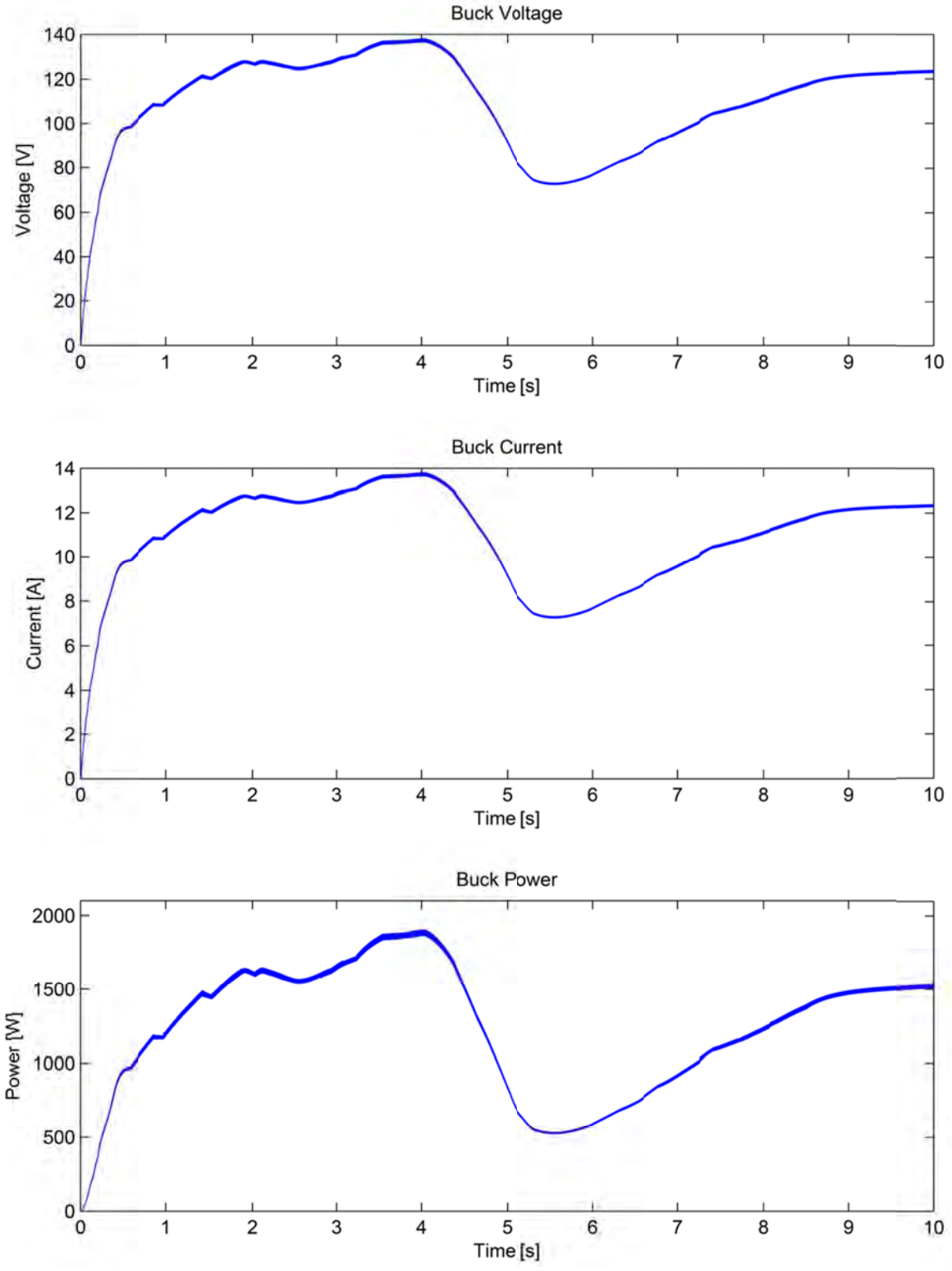


Figure 92 Buck converter output waveforms for constant G, varying T_{cell} simulation

The results observed in Figures 81 – 92 show that the MPPT control block is able to adequately track the proper maximum power point of the PV array and in turn, adjust the duty ratio of the step down converter so that the load receives that power. We see that regardless of irradiance and/or temperature change, the MPPT algorithm and control performs quite admirably in these simulations and justifies the design process.

It is important to note that there does exist a somewhat long settling time with regard to the output waveforms. This is due to the fact that we have employed large filtering capacitors to mitigate the rippling effect onto the PV array caused by the switching of the converter and also at the output of the converter itself. However, from the figures above, the largest settling time we observe is roughly 3 seconds, a decent time for practical applications.

Full Bridge Inverter

Now that we have successfully implemented the PV array with a DC-DC converter capable of tracking the maximum power point of the array, the next step is to introduce the full bridge inverter so that we may convert the DC waveform from the converter into an AC waveform suitable of being fed into the utility.

A simple H-type full bridge topology was employed for these simulations, as shown in Figure 68. IGBTs were used in the inverter's equivalent circuit design (SW1-SW4).

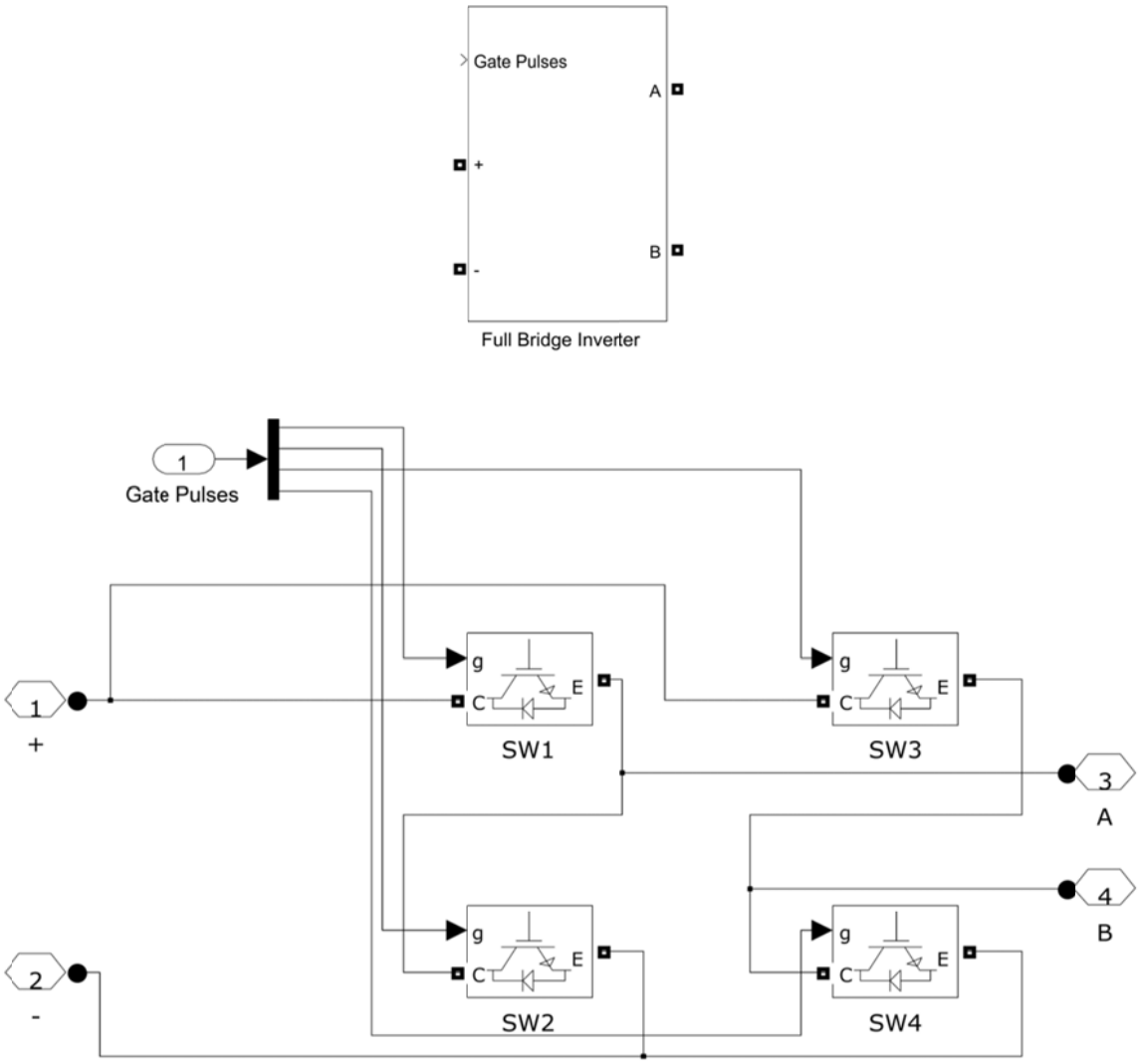


Figure 93 Full-bridge inverter control block and equivalent circuit

PWM Control

The inverter obviously cannot function without proper control signals. Therefore, a control block was designed using the Unipolar PWM switching technique, as shown in Figure 94, described earlier with a switching frequency of 20 kHz. The PWM control is also incorporated with a modulation factor control loop. This allows the PWM to control the amplitude of the output waveform by adjusting the modulation factor. This is essential in utility interactive inverters as the output amplitude must be constrained within the limits prescribed by IEEE 1547, as stated earlier.

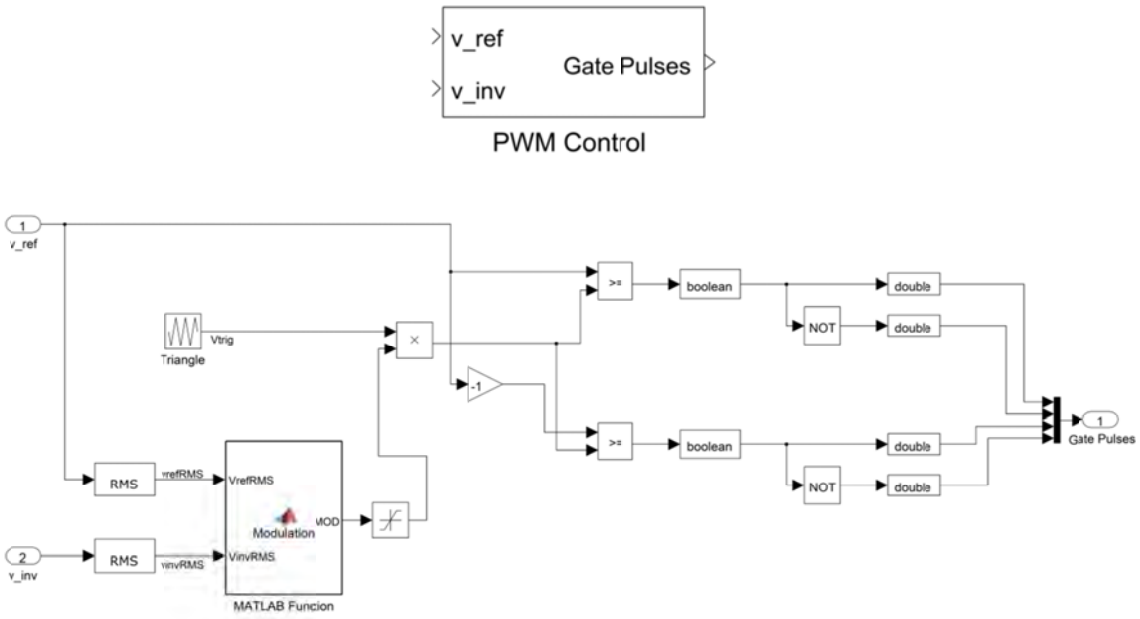


Figure 94 PWM control block employing unipolar switching logic and modulation control

By applying a sinusoidal reference signal at 60 Hz to the input of this block, we obtain the following output from the PWM control shown in Figure 95. Please note that the output has been slowed down and expanded for easier viewing. By combining the PWM control block with the full bridge inverter shown in Figure 68, we obtain the following output from the inverter shown in Figure 96. As we can see, the control signals provided by the PWM control block have produced a unipolar switching output at the value of the DC source, as we had desired.

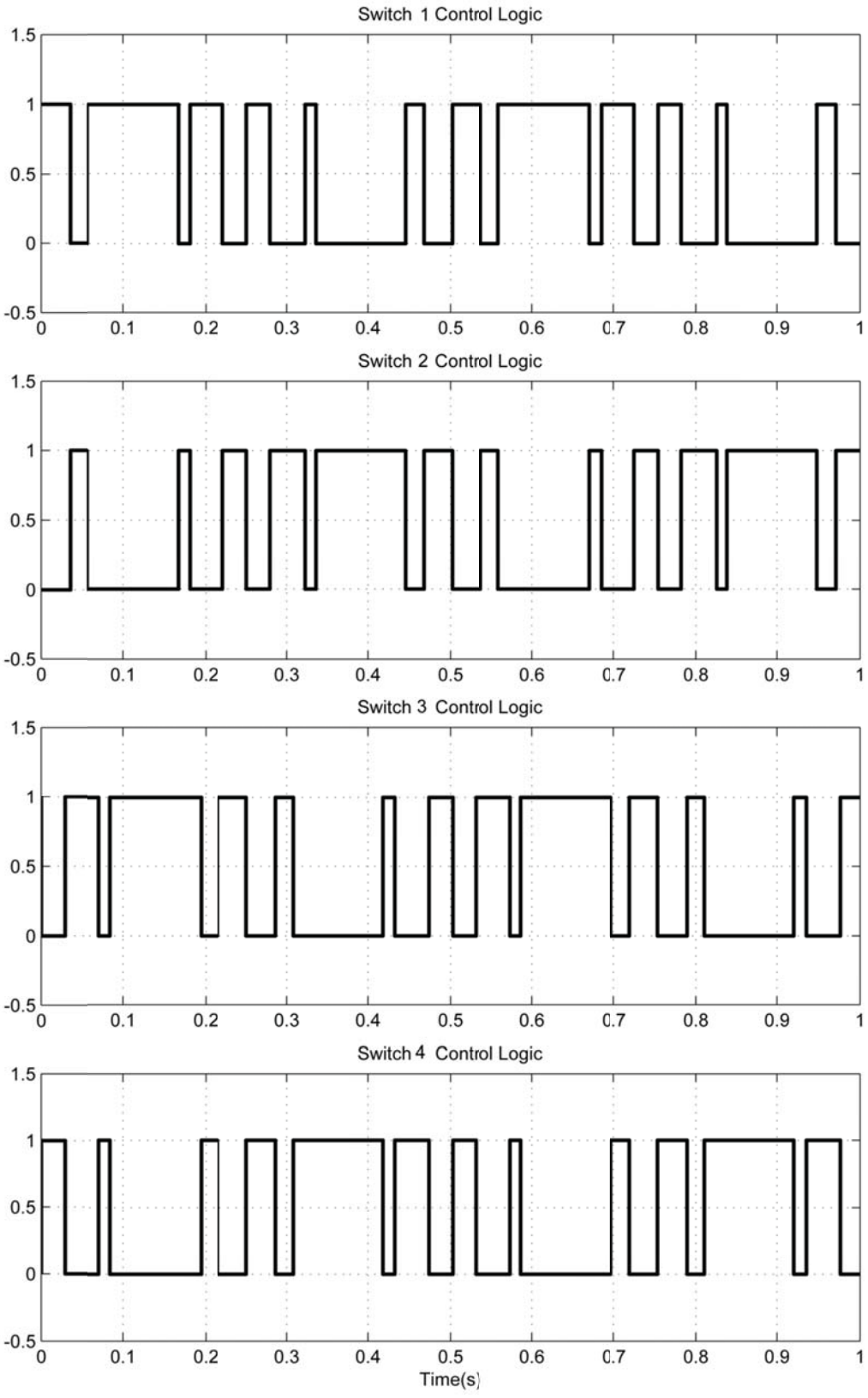


Figure 95 PWM control signals for switches SW1-SW4

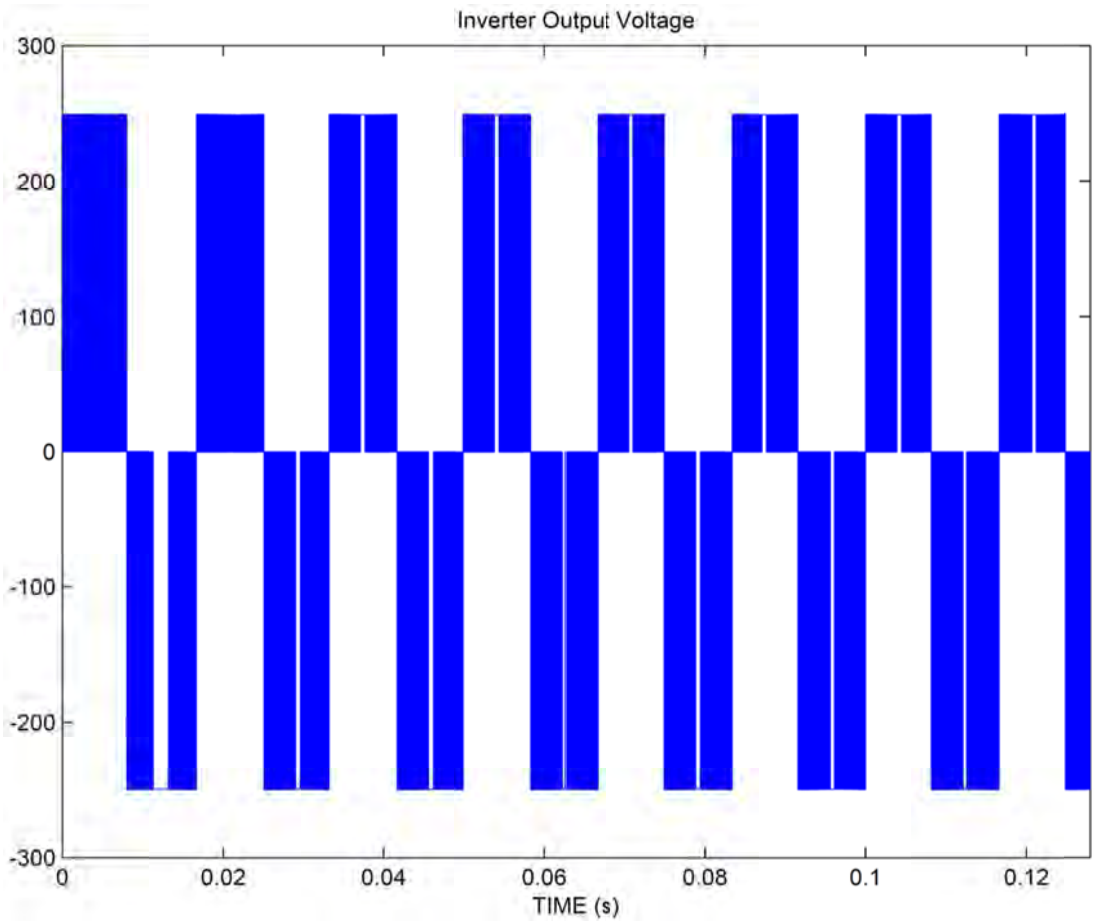


Figure 96 Inverter output voltage

SOGI-FLL with Gain Optimization

The inversion process is now complete. The next design element would be the reference signal generator used for synchronization with the utility waveform. This is one of the most important control blocks of the utility interactive inverter as it must accurately and quickly track the reference waveform obtained from the utility. Any variations in the waveform that exceed the voltage and frequency thresholds set forth by IEEE 1547 must be quickly realized so as to trip the inverter within the maximum trip times set forth by the standard. Based on the discussion earlier, a SOGI-FLL with gain optimization will be utilized to provide an accurate reference signal and a fast response to transients required by IEEE 1547. The main control block of the SOGI-FLL is shown in Figure 96. Remember that this control block is comprised of three separate sub-control blocks: the SOGI-QSG, FLL, and the Gain optimizer. The control diagrams of each subsystem are shown in the forthcoming figures.

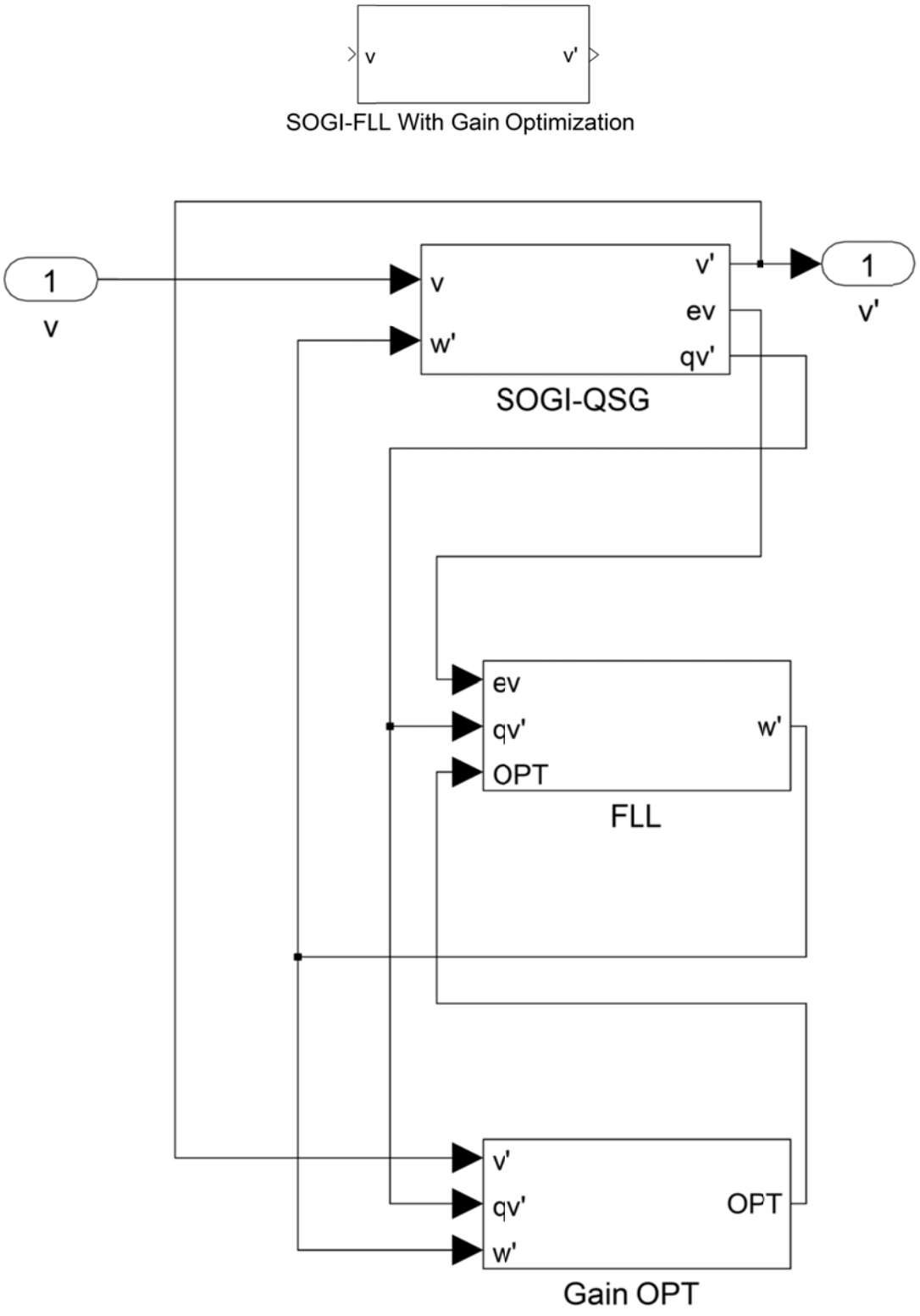


Figure 97 SOGI-FLL with Gain Optimization control block and equivalent circuit

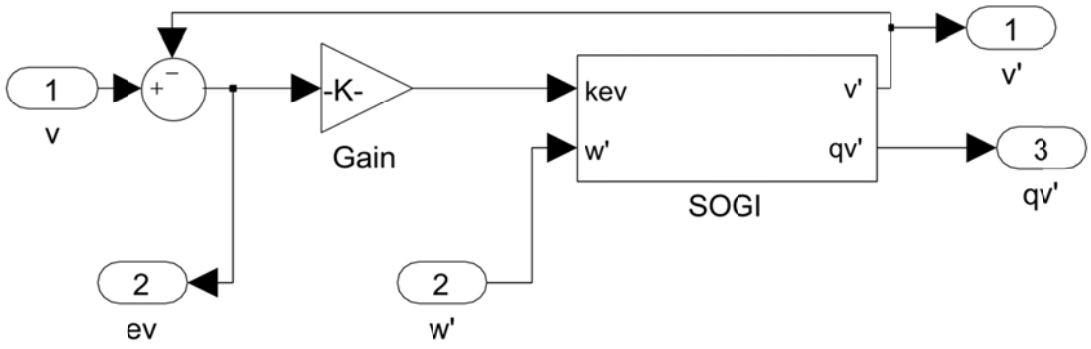


Figure 98 SOGI-QSG equivalent circuit

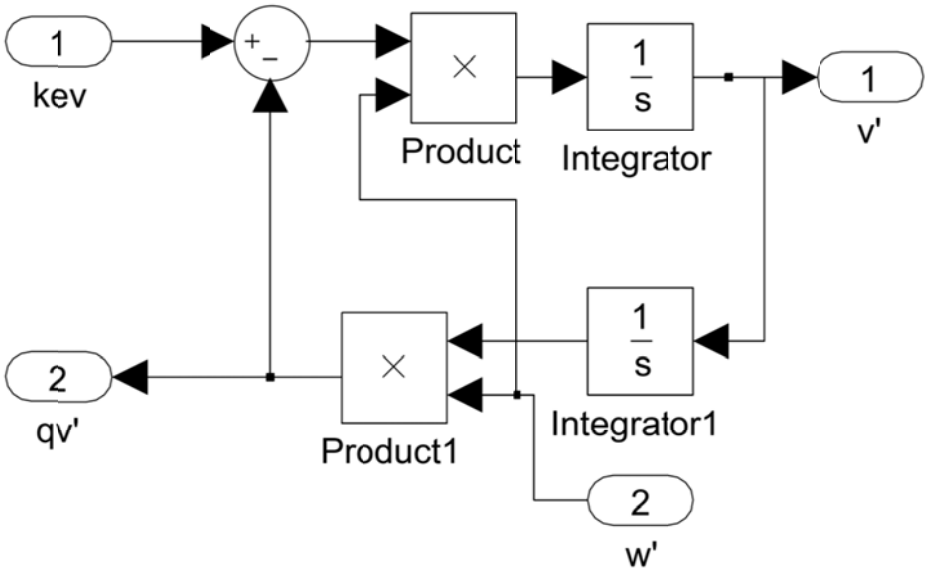


Figure 99 SOGI equivalent circuit

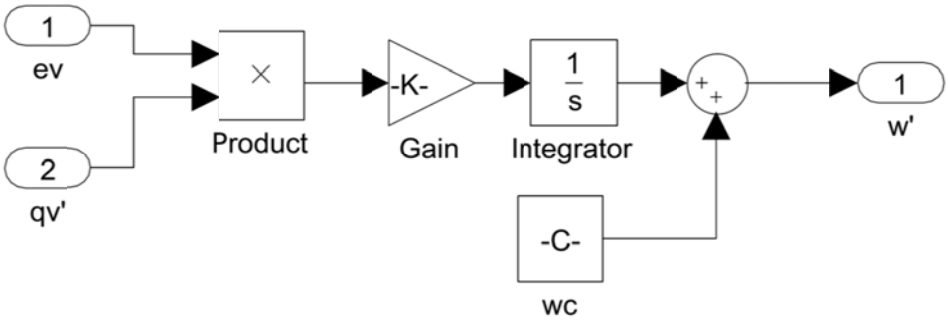


Figure 100 FLL equivalent circuit

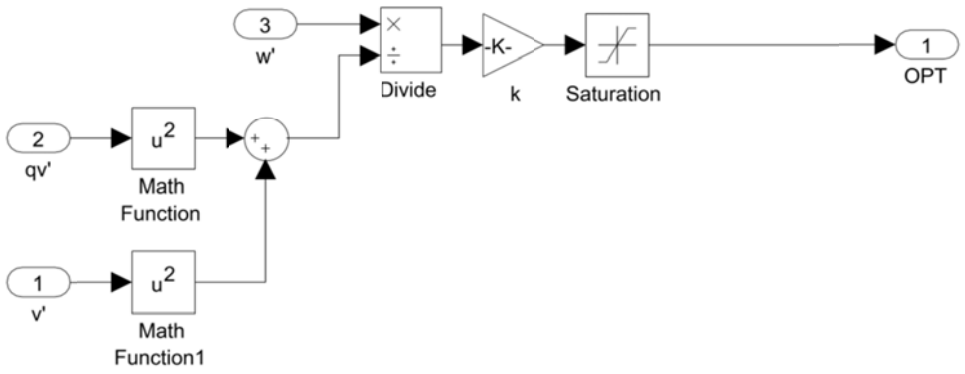


Figure 101 Gain Optimization equivalent circuit

To test the SOGI-FLL with gain optimization, a reference signal, *v*, will be applied at its input, and the output waveform *v'*, used for the PWM control block, will be analyzed to ensure a proper response to any changes. The figures below show these waveforms under various reference conditions. Please note that in the following figures, V_{REF} denotes the utility reference waveform, *v*¸ and V_{FLL} denotes the output waveform *v'*.

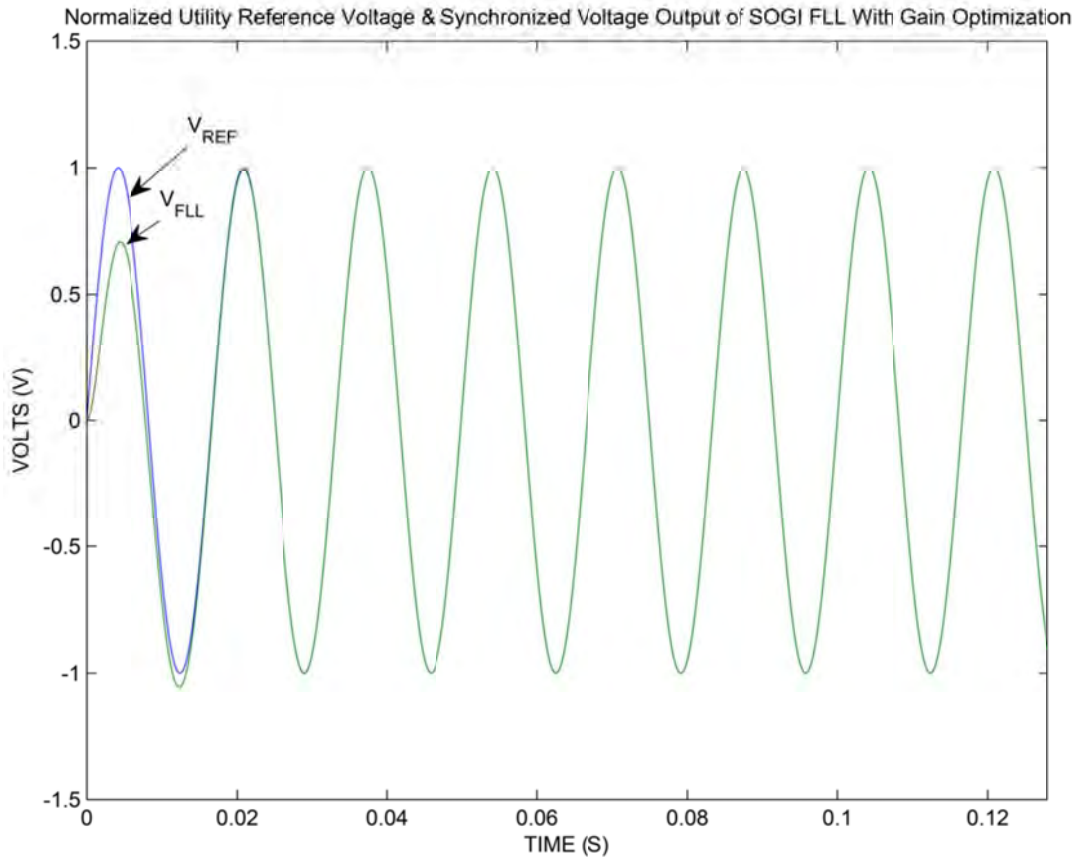


Figure 102 Input and output waveforms of the SOGI-FLL

As we can see in Figure 101, the SOGI-FLL provides a well synchronized output waveform within 0.02 seconds (1.25 cycles). This shows a great response time for the unchanging 60 Hz reference signal applied. However, the SOGI-FLL must be able to track waveforms that experience changes in frequency or phase. The figures following illustrate the response of the SOGI-FLL under varying conditions of the utility reference waveform.

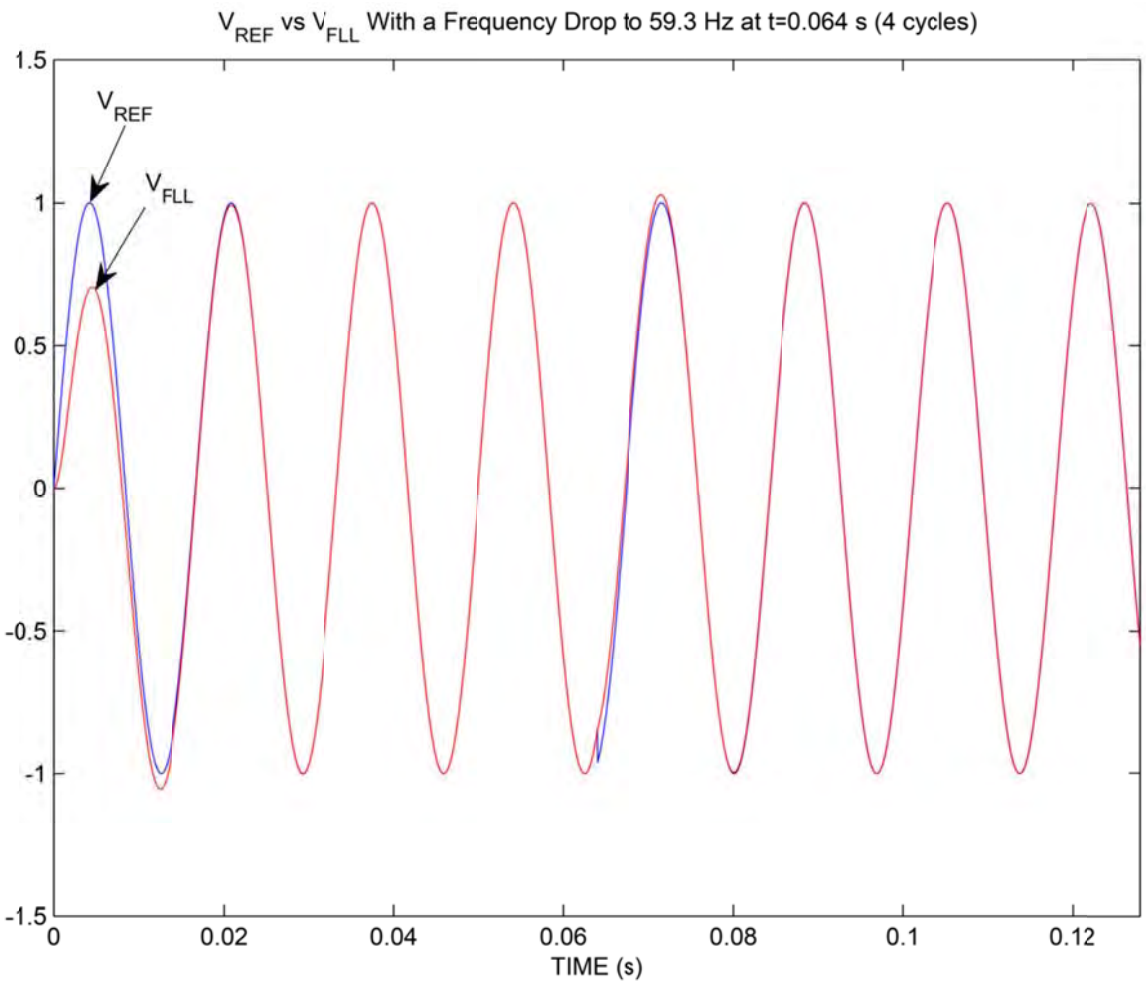


Figure 103 Input and output waveforms of the SOGI-FLL experiencing a frequency drop

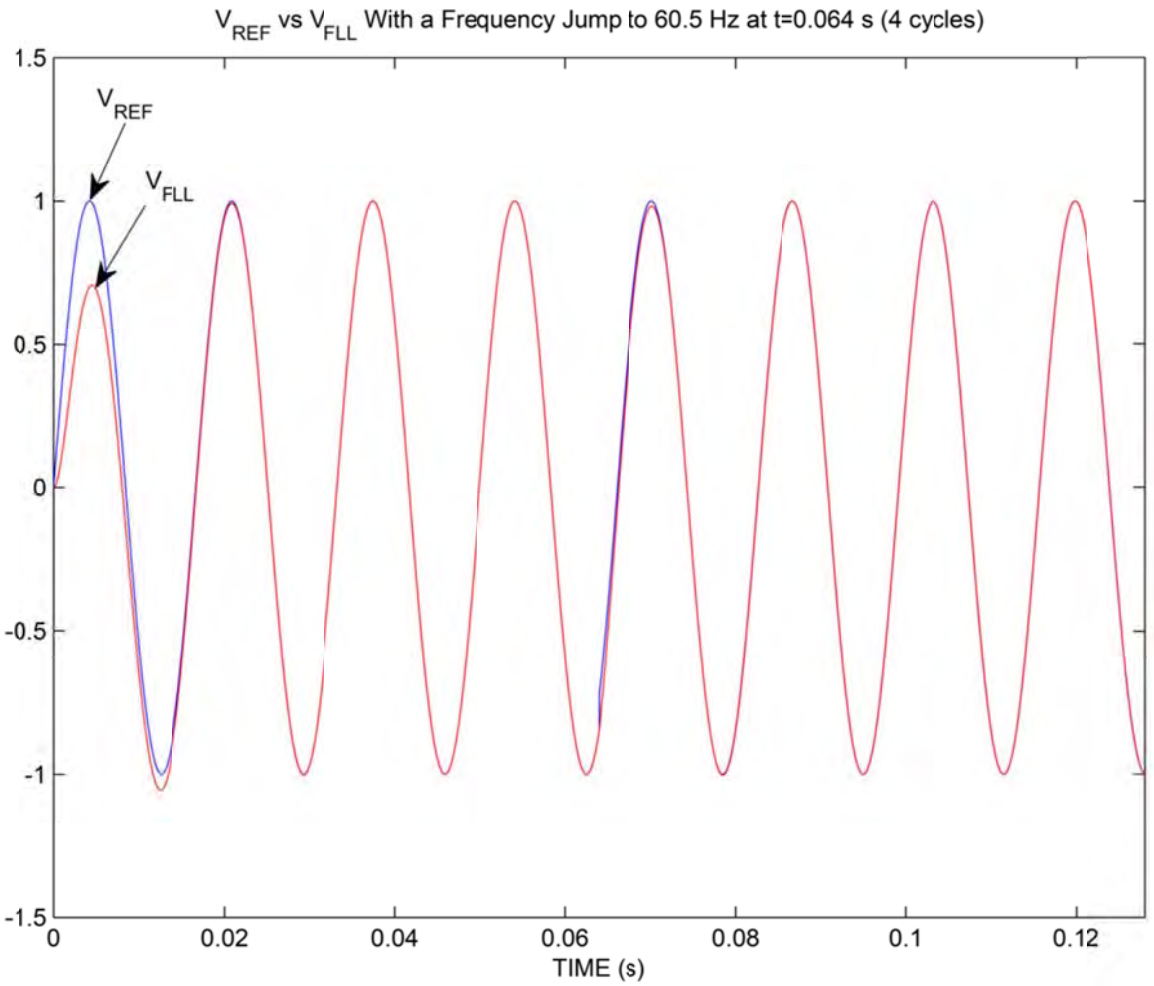


Figure 104 Input and output waveforms of the SOGI-FLL experiencing a frequency jump

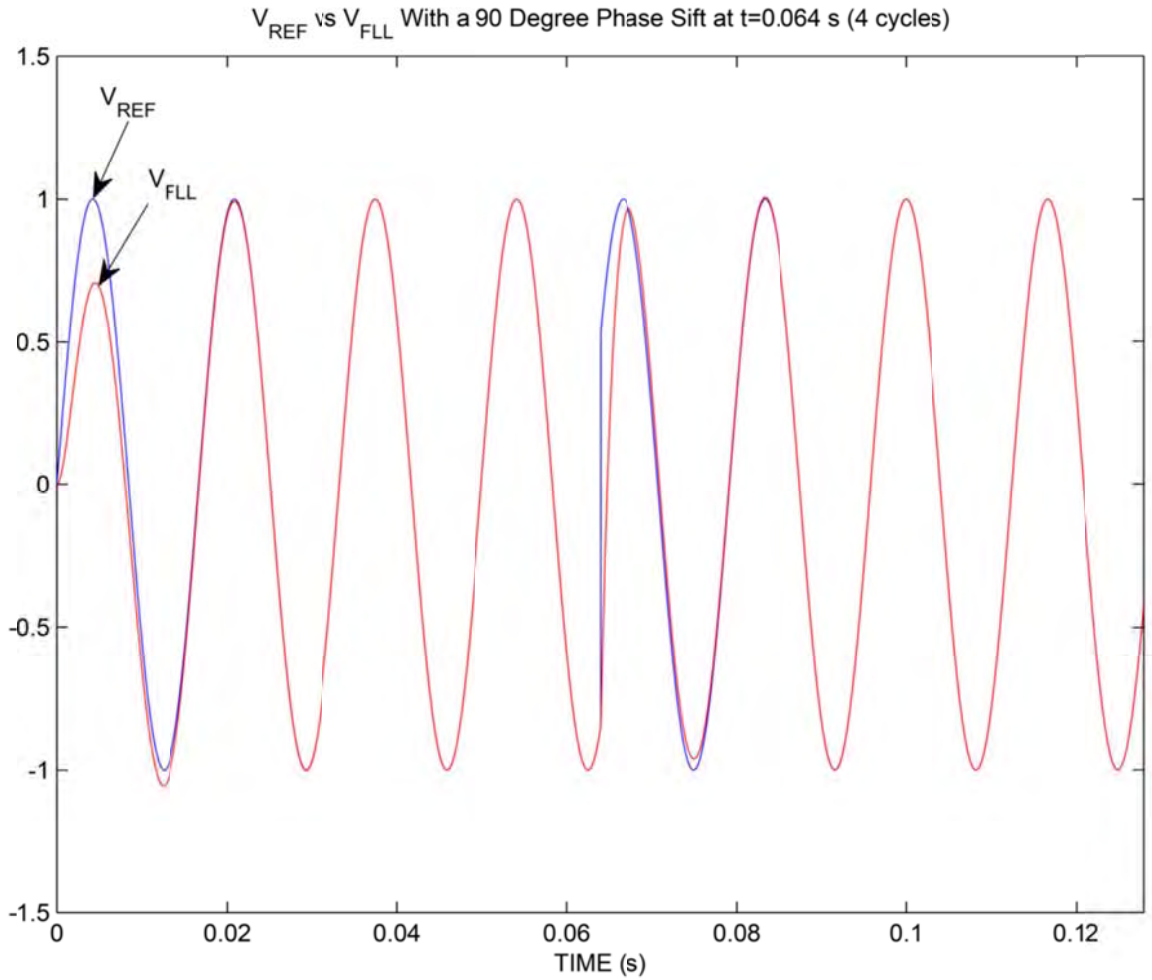


Figure 105 Input and output waveforms of the SOGI-FLL experiencing a phase shift

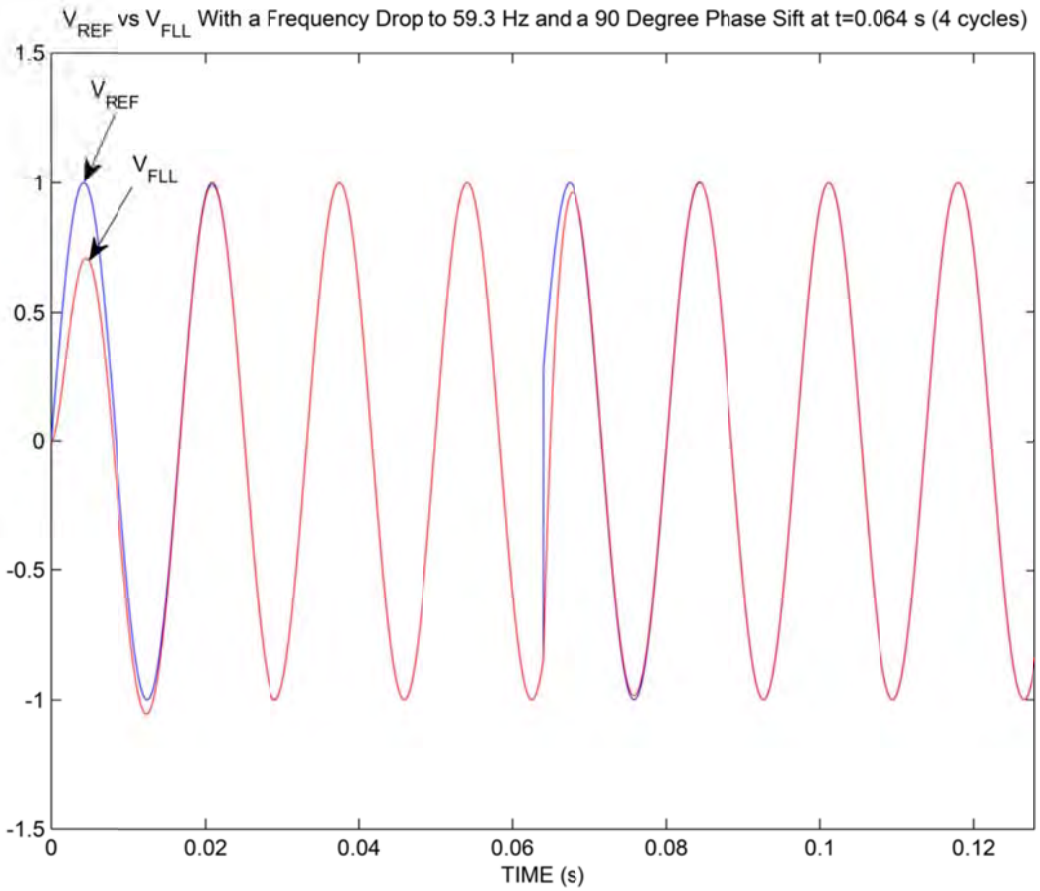


Figure 106 Input and output waveforms of the SOGI-FLL experiencing a frequency drop and phase shift

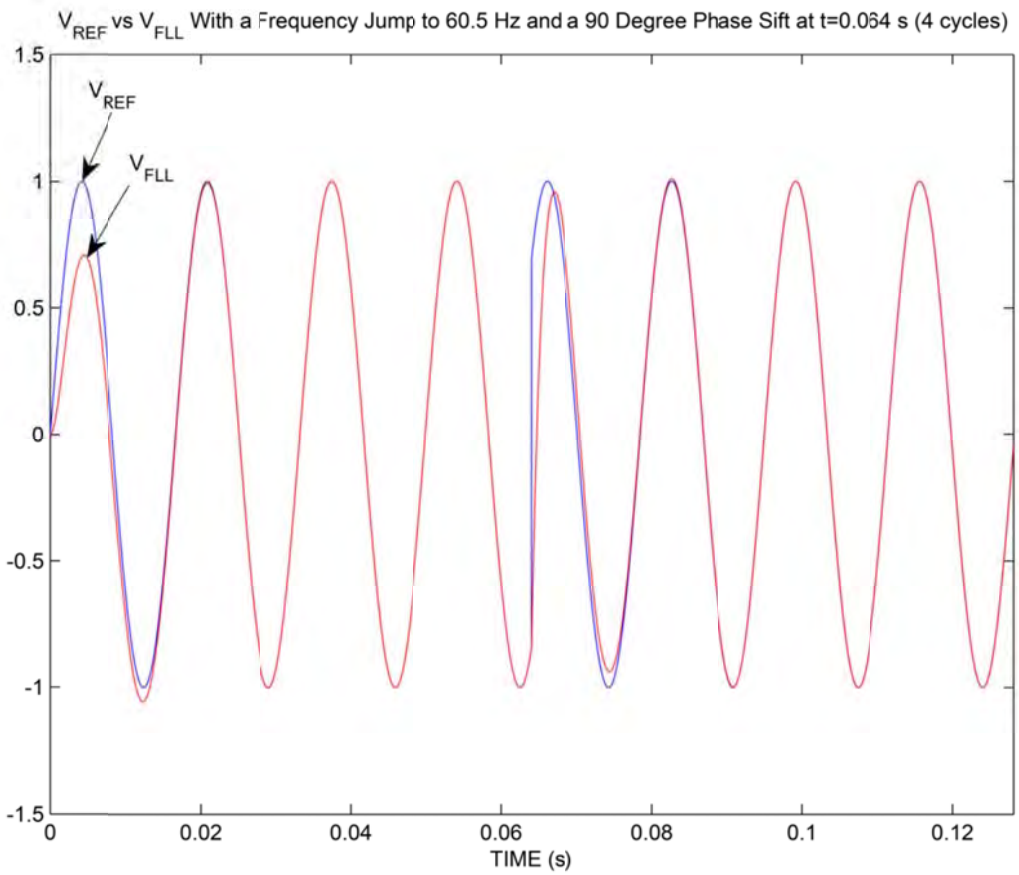


Figure 107 Input and output waveforms of the SOGI-FLL experiencing a frequency jump and phase shift

We can see in Figures 103 – 107 that the SOGI-FLL with gain optimization control block exhibits the same response time as in an unchanging input reference waveform. It is of note that the frequency values used in these simulations are the upper and lower frequency bounds set forth by IEEE 1547 (59.3 Hz < f < 60.5 Hz). With a response time of roughly 0.02 seconds (1.25 cycles), the inverter is well capable of detecting any out of bounds conditions and disconnecting from the utility within the maximum 0.16 seconds (10 cycles) required. A similar response is observed when the amplitude of the reference waveform changes. However, the results of those responses have been omitted to prevent redundancy.

Complete Circuit

So far we have determined through simulations that the Full-bridge inverter, the PWM control and the SOGI-FLL synchronization block have responded satisfactorily to our expectations. Our next set of simulations will employ these blocks in a semi-complete utility interactive photovoltaic inverter test scenario; semi-complete because we are not

utilizing an accurate model for the behavior of the utility. This is left to the reader to explore different methods and results from such a model.

Figure 108 illustrates the simulation set-up for our utility interactive inverter, along with the properly modeled PV array and DC-DC converter with MPPT control. A capacitor bank, known as a DC link, is connected at the output of the PV array to reduce the ripples caused by the switching of the DC-DC converter and inverter, thus creating as much of a DC source as possible.

This is then fed into the DC-DC converter employing the MPPT control method and algorithm. The output of the converter is then fed into the full bridge inverter to transform the signal into an AC signal.

After the inversion process, the inverted waveform is filtered utilizing a simple low pass LC filter. Other filtering techniques are also applicable, such as the LCL filter and adaptive filtering. However, for our verification purposes, the low pass characteristics the LC filter we are utilizing are adequate. At the output of the filter is a 10 Ω load.

We have applied a 200V 60 Hz reference signal at the input of the SOGI-FLL block to mimic the signal received from the utility source.

Two simulations were run to verify that the models work correctly and as expected when connected together. Both simulations kept the operating temperature of the array constant at 25 °C but varied the irradiance, once at 1000 W/m^2 and the other at 800 W/m^2 to verify that the MPPT control block is functioning properly.

Also, in order to observe compliance with IEEE 1547, harmonic analysis was done to ensure that the total harmonic distortion of the current waveform is below the maximum allowable levels.

Figures 109 - 116 are the results of the simulations.

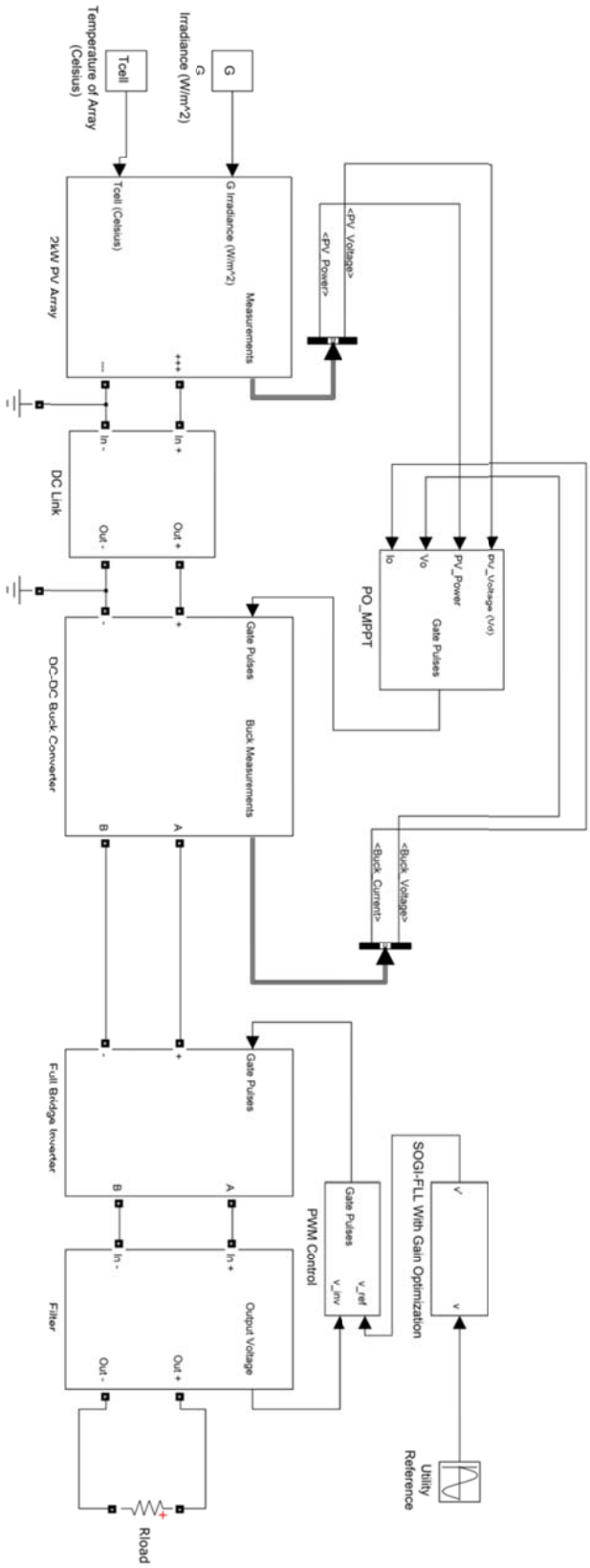


Figure 108 Complete schematic of simulation test set-up for the utility interactive inverter

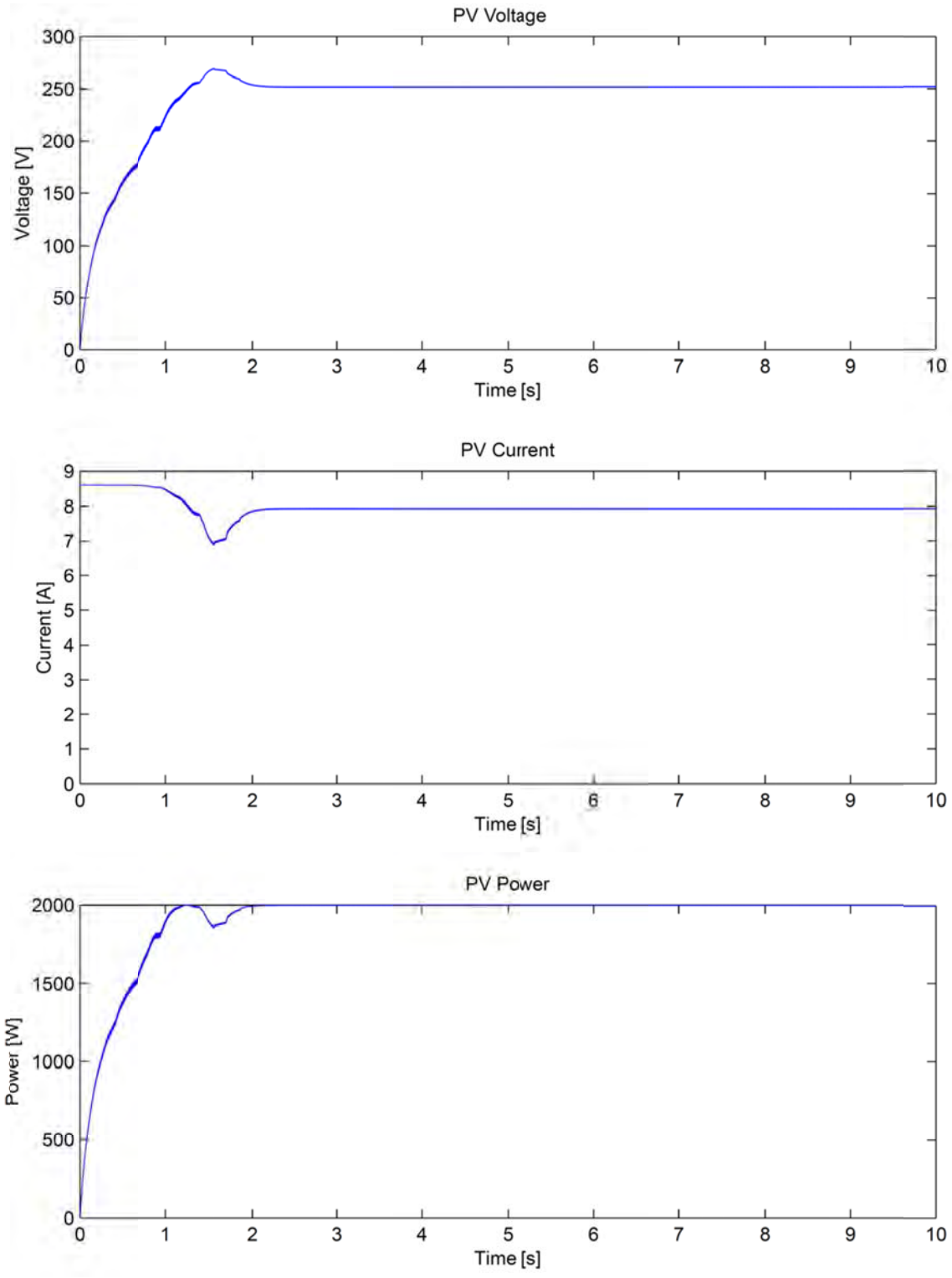


Figure 109 PV array output at G = 1000 W/m^2 of complete model simulation

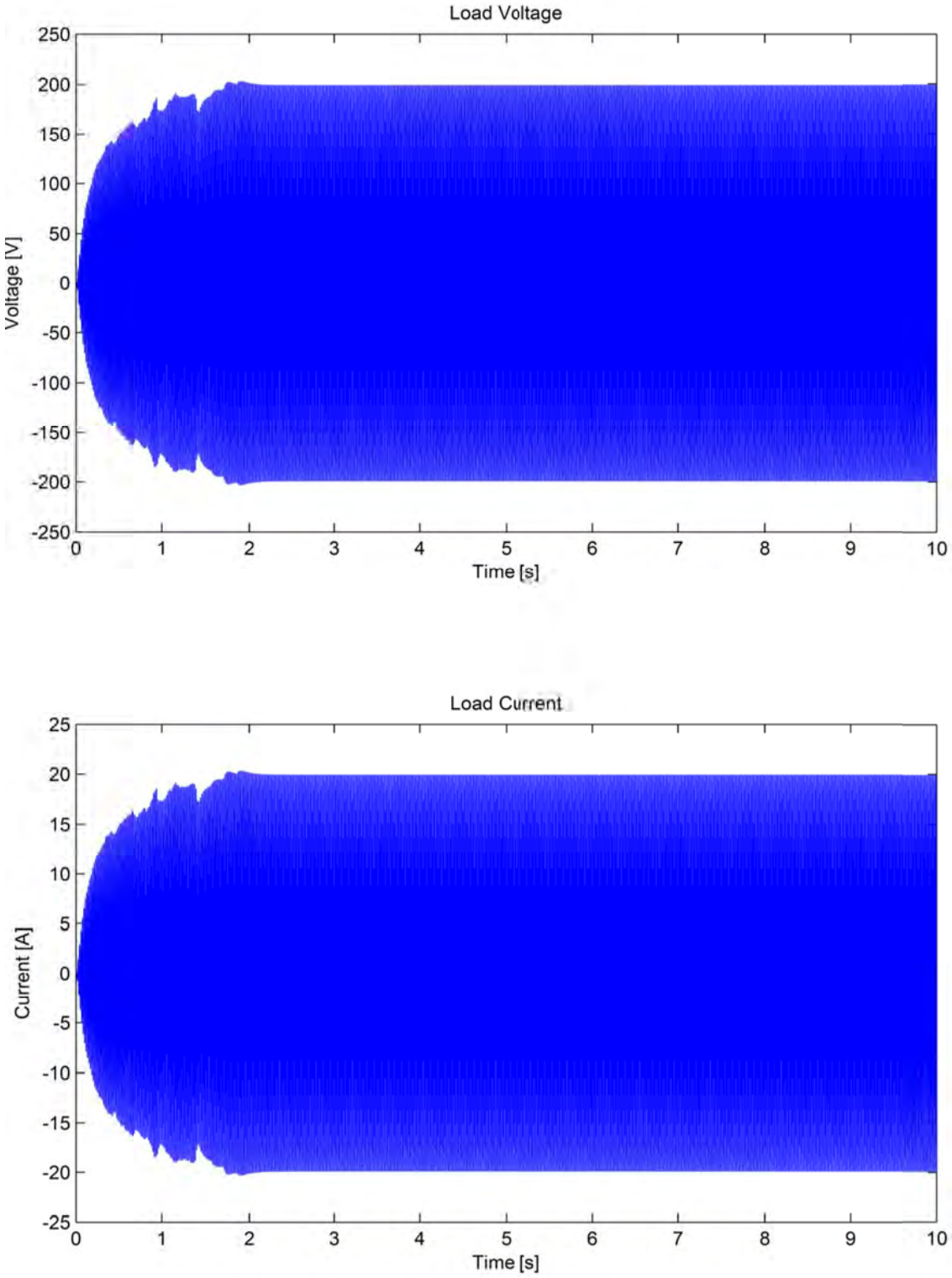


Figure 110 Load output at G = 1000 W/m^2 of complete model simulation

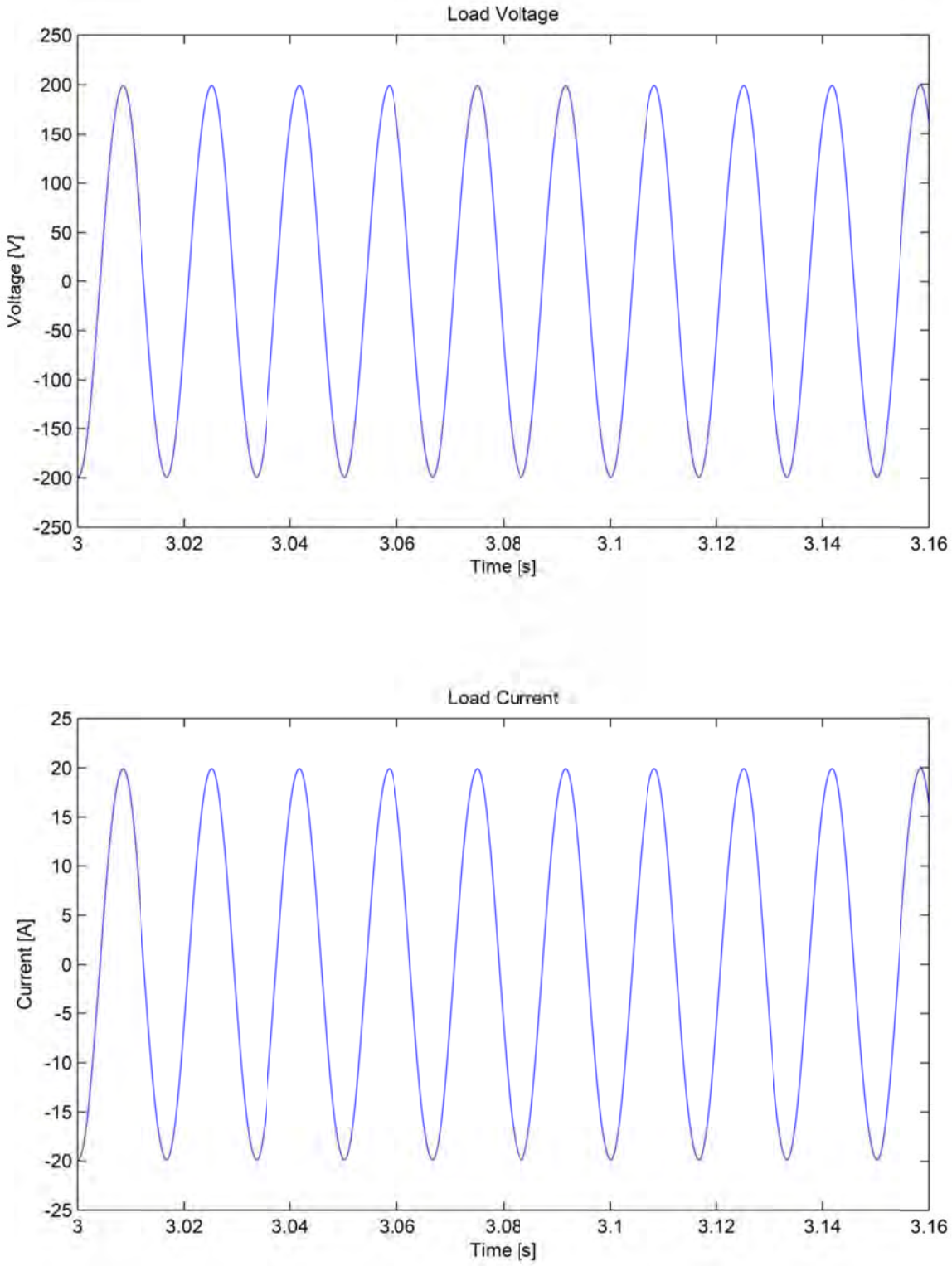


Figure 111 10 cycles of the load output at G = 1000 W/m^2 of complete model simulation

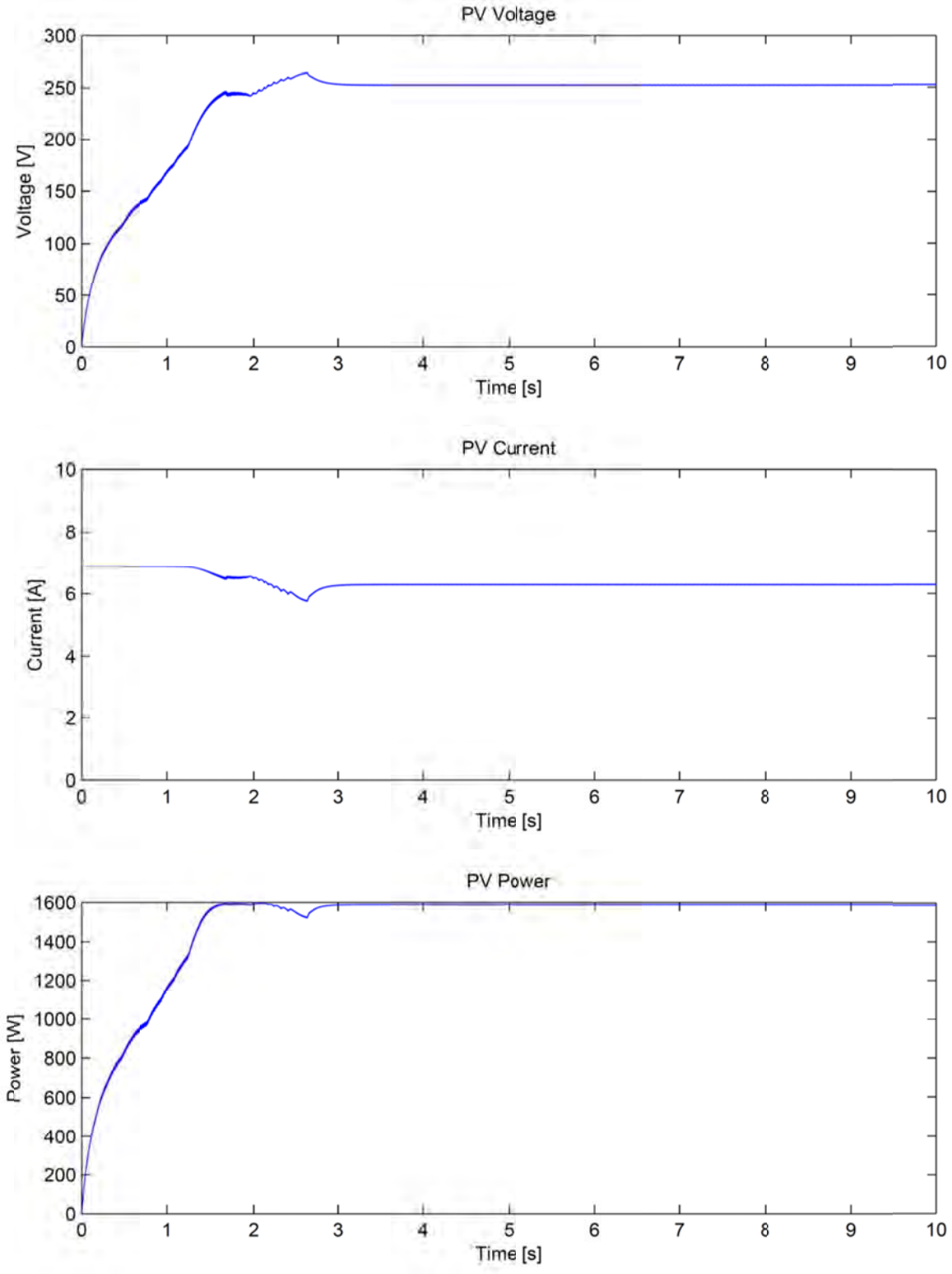


Figure 112 PV array output at G = 800 W/m^2 of complete model simulation

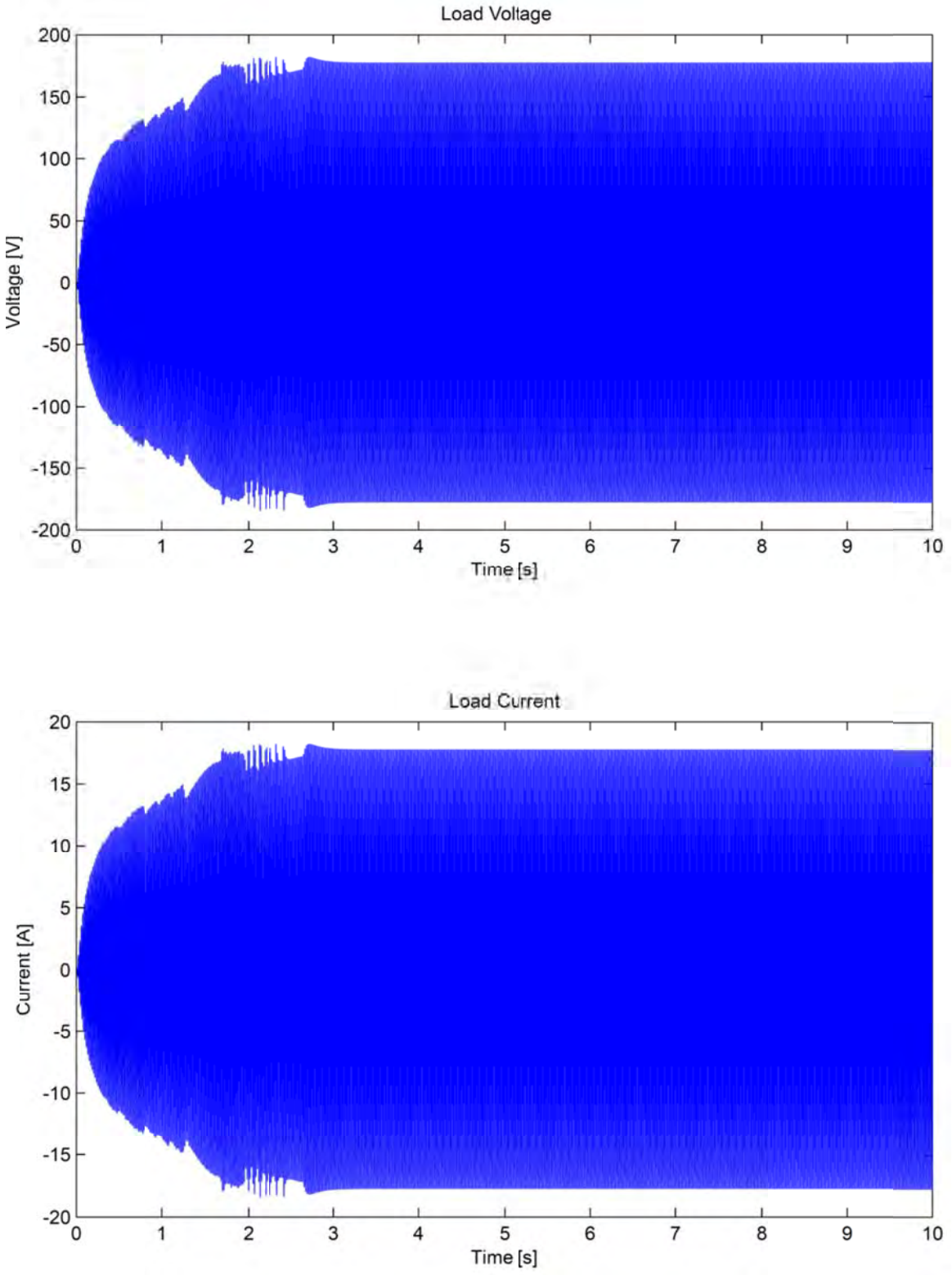


Figure 113 Load output at G = 800 W/m^2 of complete model simulation

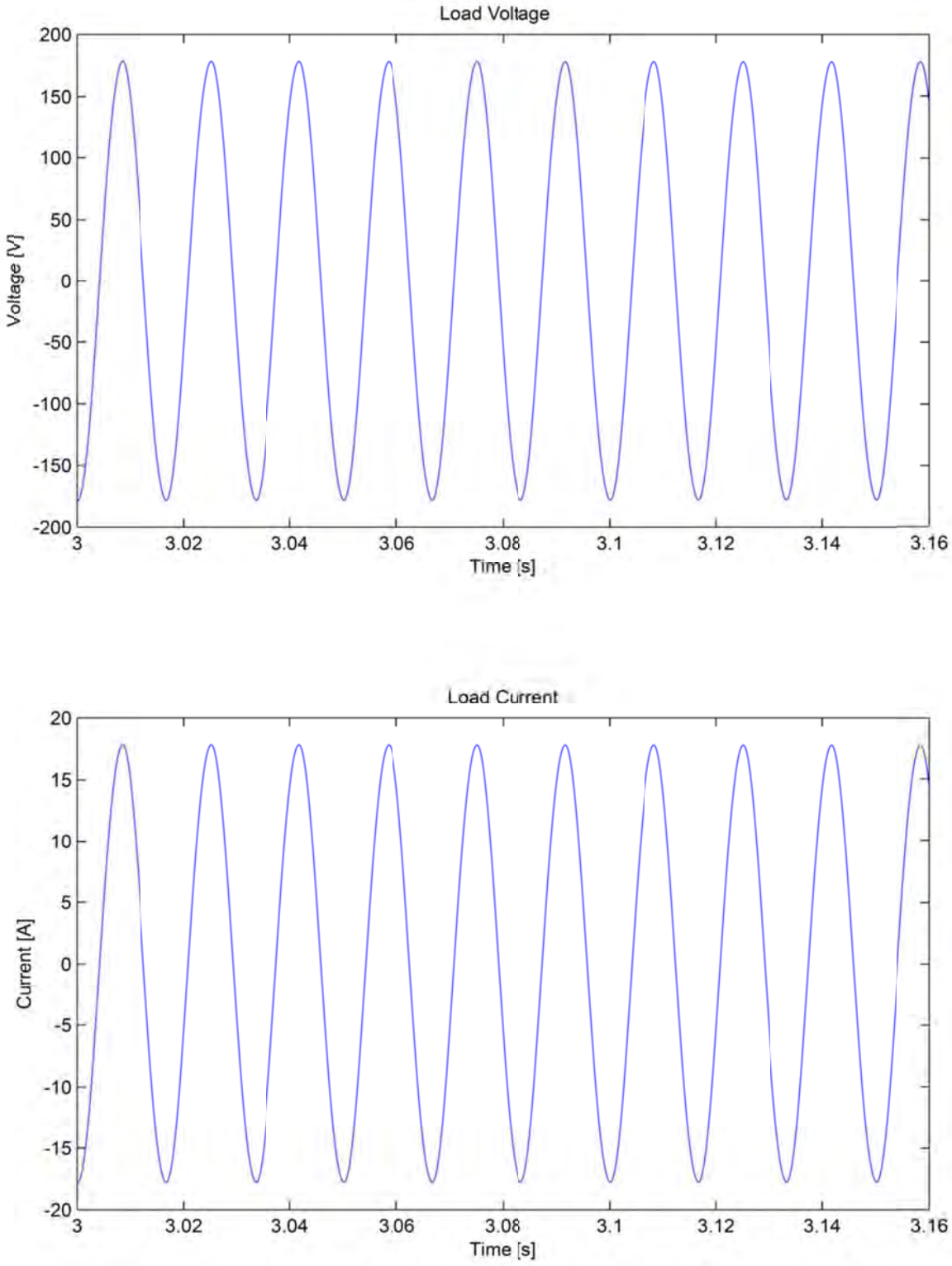


Figure 114 10 cycles of the load output at G = 800 W/m^2 of complete model simulation

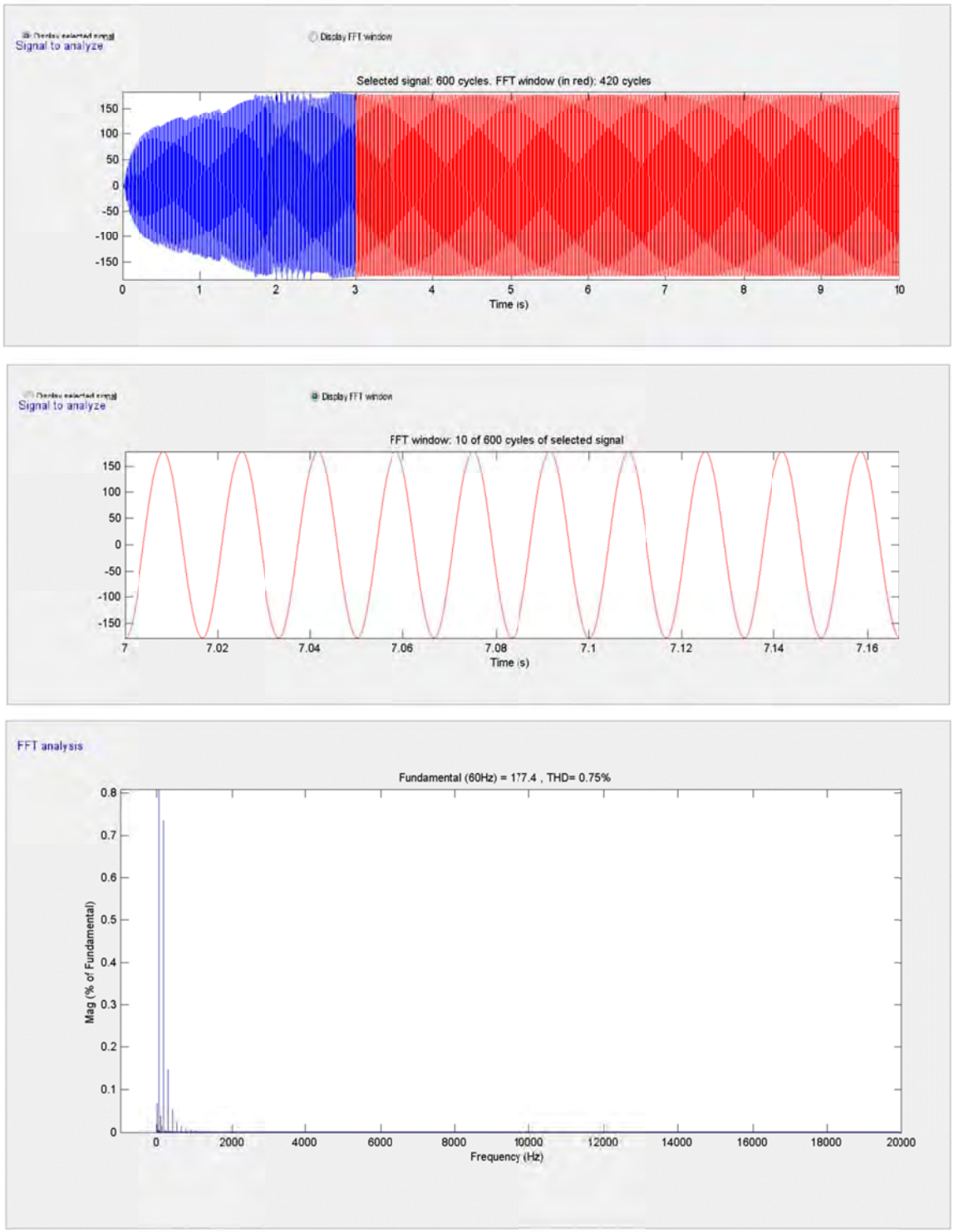


Figure 115 MATLAB® FFT analysis tool output of the voltage waveform at G = 800 W/m^2

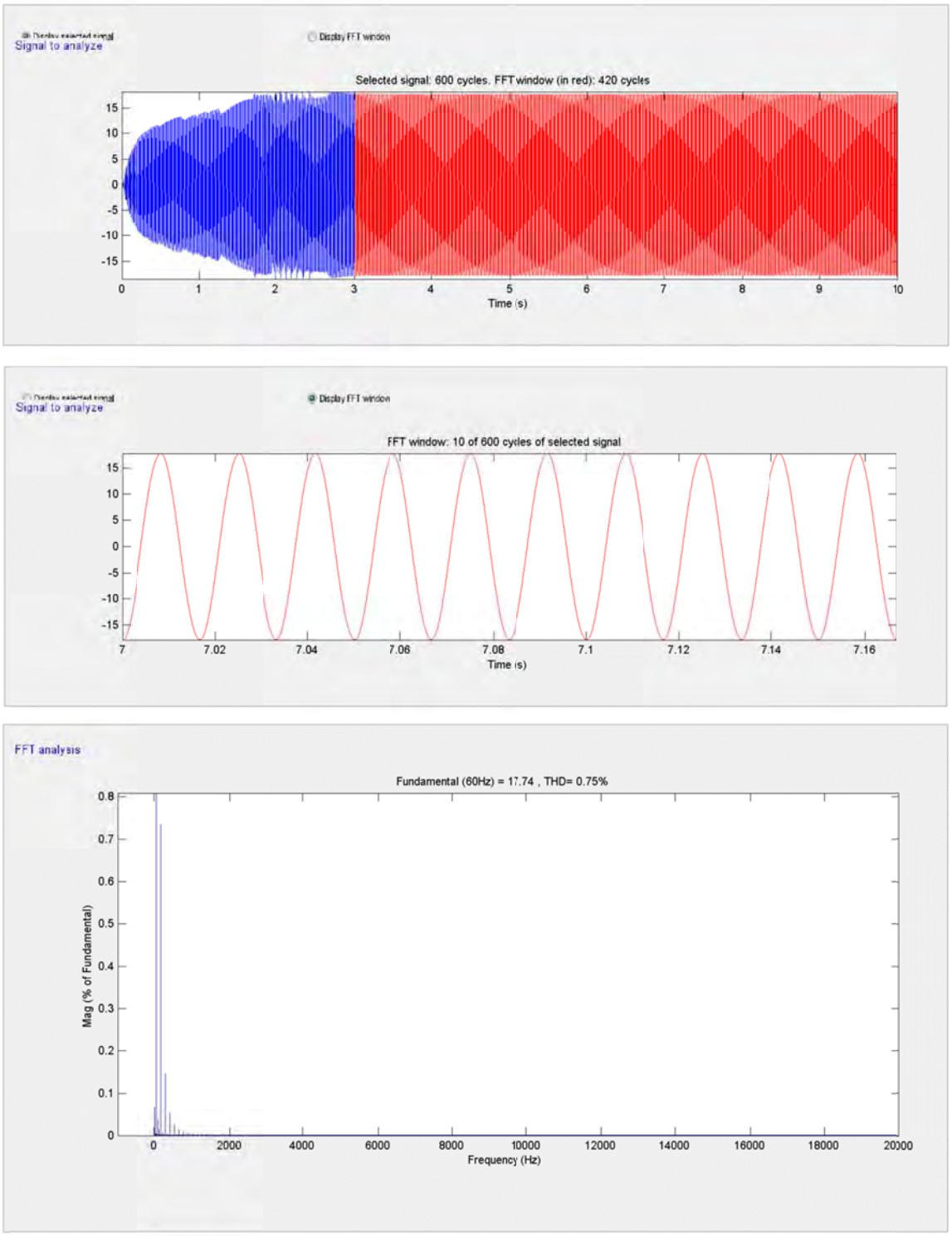


Figure 116 MATLAB® FFT analysis tool output of the current waveform at G = 800 W/m^2

We can see from the output waveforms of the simulations that the results obtained are within expectations. The MPPT control block does a great job of tracking the maximum power point of the PV array. The SOGI-FLL tracks the frequency of the reference signal and the resulting frequency of the output waveform is measured to be 59.9 Hz, well within the acceptable range for IEEE 1547.

The output voltage, however, dips below the reference signal value of 200V for G = 800 W/m^2, but still within the 88% lower limit outlined in IEEE 1547.

The total harmonic distortion of the current and voltage waveforms are an extraordinary 0.75%, also within the 5% limit imposed by IEEE 1547. This can be attributed to proper switching and filtering of the output signal.

These simulations have proven the models and theories discussed in this text to be accurate and satisfactory.

CONCLUSION

We began with a brief introduction to the theory of photovoltaics, to set a foundation regarding the use of sunlight to harvest renewable energy to provide the power we consume every day. Then the foundation of the inverter was set with the theory of power electronics. Understanding of the Fourier series, the inversion process and the various semiconductor switches used in the process. Different inverter topologies were discussed and the foundation for their control was established through the understanding of the PWM control scheme. The idea of utility interactivity, the heart of this project, was introduced, along with its nationwide standard for compliance, IEEE 1547. Utility synchronization was discussed, and it was shown through simulation that the SOGI-FLL with gain optimization control scheme provides a great response and accuracy for complying with IEEE 1547. Also in reference to IEEE 1547, anti-islanding detection methods were discussed and it was shown that at the present time only a few have the potential for standardization, such as the GE Voltage shift or the wavelet method. Maximum power point tracking algorithms were compared and determined that the P&O and IC algorithms provided the best efficiency. Finally, these concepts were put together in a simulation circuit and proven to function as a utility interactive inverter by showing the following:

1. The mathematical model of a photovoltaic cell/module/array is accurate, even when utilizing a simpler single diode model rather than the double diode model.
2. The MPPT control block and algorithm effectively output the maximum available power under any condition in coordination with the DC-DC converter.
3. The SOGI-FLL reference waveform generator provides accurate and quick responses to any changes in the utility reference, thus capable of disconnecting from the grid within the allowed maximum time set forth by IEEE 1547.
4. The output of the inverter provides an acceptable waveform with a total harmonic distortion well below the 5% limit imposed by IEEE 1547

Other considerations should be taken into account when designing a utility interactive inverter. Keep in mind that each requirement introduces different needs that the inverter must meet. There is no single type universal solution. Also, proper filtering techniques must be employed to ensure proper interaction with grid impedances.

REFERENCES

[1] U.S. Environmental Protection Agency, 'Inventory of U.S. Greenhouse Gas Emissions and Sinks: 1990 – 2010', EPA 430-R-11-005, April 2011.

[2] Luque, M. (Editor), Hegedus, S. (Editor), *Handbook of Photovoltaic Science and Engineering*, John Wiley & Sons, Ltd., Chichester, 2003, ISBN 0471491969.

[3] Kopp, G., Lean, J., 'A new, lower value of solar irradiance: Evidence and climate significance', *Geophysical Research Letters*, Volume 38, Issue 1, CiteID L01706, January 2011.

[4] USL Photovoltaics Pvt Ltd., 'High Performance Solar Cell' (Datasheet), *http://www.uslpv.com/pdf/UPL_PV_Cells/UPL_P5_P6_CELL_SPEC.pdf*, Retrieved August 14, 2011.

[5] Wenham, S., Green, M., Watt, M., Corkish, R., *Applied Photovoltaics*, Earthscan, London, 2007, ISBN 1844074013.

[6] Zweibel, K., *Basic Photovoltaic Principles and Methods*, Van Nostrand Reinhold Co., New York, 1984, ISBN 0442281269.

[7] Mitsubishi Electric Corporation, 'Photovoltaic Modules – MDT Series' (Datasheet), *http://www.mitsubishielectric.com/bu/solar/pv_modules/pdf/L-175-0-B8720-B.pdf*, Retrieved August 15, 2011.

[8] Mohan, N., Undeland, T., Robbins, W., *Power Electronics Converters Applications, and Design*, John Wiley & Sons, Inc., Hoboken, 2003, ISBN 0471429082.

[9] McMurray, W., 'Inverter Circuits', US Patent 3207974, September 1965.

[10] Teodorescu, R., Liserre, M., Rodriquez, P., *Grid Converters for Photovoltaic and Wind Power Systems*, John Wiley & Sons, Ltd., Chichester, 2011, ISBN 0470057513.

[11] Best, R.E., *Phase-Locked Loops: Design, Simulation, and Applications*, 5th edition, McGraw-Hill Professional, New York, 2003, ISBN 0071412018.

[12] Franklin, G.F., Powell, J.D., Emami-Naeini, A., *Feedback Control of Dynamic Systems*, 4th edition, Prentice Hall, 2002, ISBN 0130323934.

[13] Park, R.H., 'Two Reaction Theory of Synchronous Machines. Generalized Method of Analysis – Part I', *Proceedings of the Winter Convention of the AIEE*, 1929, pp. 716-730.

[14] Widrow, B., Glover Jr, J.R., McCool J.M., Kaunitz, J., Williams, C.S., Hearn, R.H., Zeidler Jr, J.R., Dong, E., Goodlin, R.C., 'Adaptive Noise Cancelling: Principles and Applications', *Proceedings of the IEEE*, **63**(12), December 1975, 1692-1716.

[15] Ciobotaru, M., Teodorescu, R., Blaabjerg, F., 'A New Single-Phase PLL Structure Based on Second Order Generalized Integrator', *Proceedings of the IEEE Power Electronics Special Conference (PESC'06)*, June 2006, pp.1-7.

[16] Bower, W., Ropp, M., 'Evaluation of Islanding Detection Methods for Utility-Interactive Inverters in Photovoltaic Systems', SANDIA Report SAND2002-3591, Albuquerque, NM: Sandia National Laboratories, November 2002, *http://prod.**sandia**.gov/techlib/access-control.cgi/2002/02**3591**.pdf*, Retrieved November 28, 2011.

[17] Lopes, L.A.C., Sun, H., 'Performance Assessment of Active Frequency Drifting Islanding Detection Methods', *IEEE Transactions on Energy Conversion*, **21**(1), March 2006, 171-180.

[18] Hohm, D.P., Ropp, M.E., 'Comparative Study of Maximum Power Point Tracking Algorithms', *Progress in Photovoltaics: Research and Applications*, **11**, November 2002, 47-62.

[19] Femia, N., Petrone, G., Spagnuolo, G., Vitelli, M., 'Optimization of Perturb and Observe Maximum Power Point Tracking Method', *IEEE Transactions on Power Electronics*, **20**(4), July 2005, 963-973.

[20] Hussein, K.H., Zhao, G., 'Maximum Photovoltaic Power Tracking: An Algorithm for Rapidly Changing Atmospheric Conditions', *IEEE Proceedings of Generation Transmission, Distribution*, **142**(1), 1995, 59-64.

[21] Villalva, M.G., Gazoli, J.R., Filho, E.R., 'Comprehensive Approach to Modeling and Simulation of Photovoltaic Array', *IEEE Transactions on Power Electronics*, **24**(5), May, 2009, 1198-1208.

[22] Bedford, B.D., Hoft, R.G., *Principles of Inverter Circuits*, John Wiley & Sons, Inc., New York, 1964, ISBN 0471061344.

[23] Trzynadlowski, A., *Introduction to Modern Power Electronics*, 2nd Edition, John Wiley & Sons, Inc., Hoboken, 2010, ISBN 0470401033.

[24] Fuchs, E.F., Masoum, M.A.S., *Power Conversion of Renewable Energy Systems*, Springer Science+Business Media, LLC, New York, ISBN 1441979780.