CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

Physics Based Analytical Model of Gallium Nitrate MESFET Microwave frequency applications

A graduate project submitted in partial fulfillment of the requirements
For the degree of Masters of Science
In Electrical Engineering.

By
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May 2013

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ACKNOWLEDGMENT

I would like to express my sincere gratitude and appreciation to everyone who made this thesis possible. Most of all, I would like to thank my project coordinator, Dr.Somnath Chattopadhyay for his guidance in achieving my thesis objective. It was an honor getting the privilege to work under his supervision. I would also like to thank my other committee members, Dr. Robert D Conner and Dr. Ramin Roosta for providing their valuable suggestions.

I would also like to thank the Department of Electrical and Computer Engineering for providing the facilities to complete this project.

Finally, I would like to express my love and gratitude to my parents; for their understanding & endless love, through the duration of my studies.

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ABSTRACT

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Masters of Science in Electrical Engineering.

In the previous many years, developing of wide band gap materials for example GaN in view of its lesser thermal generation rate and elevated breakdown field for its potential utilization for elevated power, elevated temperature and microwave frequency use. Military based applications have a great interest in GaN based high power and efficient semiconductor materials devices. GaN Metal Semiconductor Field Effect Transistors (MESFETs) have accepted much consideration as its structure is less difficult to examine than that of High Electron Mobility Transistors (HEMTs) and its epi-layers and the physical impacts are simpler to acknowledge and decipher. Simple physics based analytical models are required to be developed for various parameters of GaN in order to use it vast potential in semiconductor electronics. This will give a new dimension to computer–aided digital design of GaN ICs. In this thesis an effort has been made to demonstrate various qualities of GaN such as I-V, C-V and transconductance keeping in account the impact of parasitic resistances.

CHAPTER 1

Introduction:

In the developing era of semiconductor electronics electron tubes were regularly utilized as a part of the electronic frameworks, for example radio and TV, however they had certain genuine restrictions relating to their exhibition. At that point an improved revelation was made in 1947, when Bardeen and Brattain developed the transistor by utilizing a cut of germanium with a couple of precisely put wires. Since its commencement, the transistor carried an upset to the industry and in normal life through its utilization in various control RF and automation fields. The different modern demands led to the outcome of diverse sort of transistors available today in the business sector. MESFET stands for metal semiconductor field impact transistor. It is truly comparative to a JFET in development and terminology. The distinction is that in place of utilizing a p-n intersection for a gate, a Schottky (metal-semiconductor) intersection is utilized. MESFETs are typically developed in compound semiconductor advances needing high caliber surface passivation for example GaAs, InP, or SiC and are speedier yet more costly than silicon-based JFETs or MOSFETs. Handling MESFETs are worked up to roughly 45 GHz, and are ordinarily utilized for microwave frequency applications and radar. From a computerized circuit plan viewpoint, it is progressively troublesome to utilize MESFETs as the support for advanced incorporated circuits as the scale of coordination goes up, contrasted with CMOS silicon based design. The thought of Schottky barrier FET was presented by Schottky. He gave the thought of arrangement of a potential hindrance because of the distinction of work capacity between the metal and the semiconductor contacts. Thereafter, an analyst from Bell Laboratories William Shockley developed the junction transistor and Bell Laboratories announced this development in 1951. Schottky's thought was used by Mead in 1966 for the manufacture of Metal Semiconductor Field Effect Transistor (MESFET) and in this way it was created by Hooper in 1967 utilizing a Gallium Arsenide (GaAs) epitaxial layer on semi isolating GaAs substrate. A MESFET is a three-terminal apparatus like whatever viable transistor. Charge bearers (electrons) spill out of the source to the channel by means of a channel. The channel is described by doping the epitaxial layer developed on semiconductor and

offers great conduction. The rush of charge bearers in the channel is regulated by a Schottky restraint entryway. [1]

The principle preferences of a MESFET contrasted with its counterparts are:
(a) High electron velocity inside the channel.
(b) Smaller travel time accelerating quicker reaction.
(c) Fabrication of active layer on semi-insulating GaAs substrates to decrease the parasitic capacitances resulting in high switching speed.
(d) Majority carrier for channel conductance.
(e) Extremely low noise.

The crux preference of the MESFET is that because in the channel the electron mobility is huge contrasted with the MOSFET. Since the carriers found in MOSFET for inversion layer have a Wave capacity, which augments into the oxide, their portability likewise implied as surface mobility is less than 50% of the versatility of mass material. As the exhaustion locale splits the transporters from the surface their portability is near that of mass material. The mobility of the bulk material is prospectively cl;oser to carriers as they are separated by depletion region.[2].

The hindrance of the MESFET structure is the vicinity of the Schottky metal gate. It works as a constraint for the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. The turn-on voltage is commonly 0.7 V for GaAs Schottky diodes. As a result there is lesser threshold voltage compared to turn on voltage. Subsequently it is more troublesome to create circuits holding a hefty number of improvement modes MESFET [3]. The higher travel frequency of the MESFET makes it especially of investment for microwave circuits.

While the playing point of the MESFET furnishes a predominant microwave circuit and amplifier, the impediment by the diode turn-on is effortlessly tolerated. The higher current and transconductance provided by the depletion mode MESFETs makes them preferable. These circuits also limit the use of transistors and thus the control of threshold is no more a concern. The covered channel additionally yields an improved

commotion exhibition as trapping and discharge of transporters into and from surface states and imperfection is disposed of. [4]

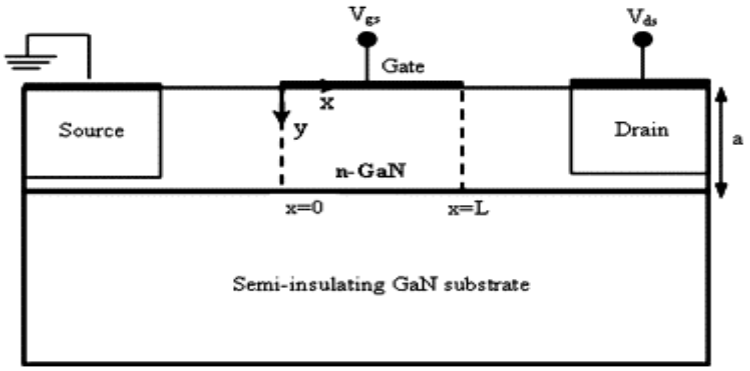


Figure 1.1a picture of MESFET Chips

This paper examines the microwave frequency applications of GaN MESFET. Starting from I-V characteristics, I analyzed the C-V characteristics and transconductance properties using physics based model for GaN. Various possible impacts of the parasitic resistances and capacitances are considered, with emphasis to discuss the potential applications of GaN MESFET and a better realizable design. [5]

GaN has incredible potential for utilization as a material for force gadgets owing to its predominant electrical properties. The differentiable property compared to counterfeits of GaN is that it has an elevated avalanche breakdown field. The device simulation and display of the analytical and physical models for various parameters of GaN is very important. This will help to not only explore the material but also help to emerge it as a market leader for highly significant electronic applications. [6]

In the displaying and configuration of GaN MESFET control apparatuses for wide band requisitions closed structure interpretations are created for the parameters displaying small signal of wide band GaN control MESFET's. Recognizing the power handling competence of GaN fabricated devices depict the different impediments in non-conducting and conducting states. The proposed models indicate that (SAGFET's) have an expansive band cutoff-frequency figure of benefit to the extent that twice that of routine MESFET's, granted that the voltage taking care of ability of the SACFET is markedly lower[7]. A totally low cost and fabrication friendly impact is considerably a

income of the high power, broad band, linear and efficient GaN devices. This is a new cost revolution for versatile RF framework (AMRFS) for military requisitions. GaN MESFETs have accepted much consideration as its structure is less complex to dissect than that of HEMTs [8].

The Gallium Nitride (GaN) material has excellent electrical properties that make it a viable alternative to SiC for microwave high-power and high temperature application. GaN HEMT's with output power of 9.8W/mm at 8 GHz [4],f_t =101GHz and f_{max}= 155 GHz, and operating temperature of 750°C have been reported [9]. There is much interest in nitride semiconductor material for a variety of applications. Growth technology is rapidly progressing and theoretical work is yielding material transport data. GaN also has potential for producing microwave power devices capable of high-temperature operation. For a doping concentration of 1×10^{17}, the theoretical low field electron mobility of GaN is about 1500cm^2/Vs, which is higher than the values for any of the SiC poly-types. [9]

The high frequency requisitions make GaN a very viable choice. This is basically due to an electron saturation velocity as high as 3×10^{17}cm/s and a definitely lower dielectric constant with a resulting lower capacitance. The integrated circuits are highly realizable and prefer (HBTs) due to their heat tolerance. Moreover some of the application requiring high speed and frequency can make use of the high temperature tolerance property of GaN devices and HBTs. These properties can be helpful for RADAR, satellite and aircraft applications. In harsh environments of elevated temperature and superior power demanding situation GaN based FETs are the potential devices due to their power amplification and switching properties. [10] There is an in number advancement undertaking on wide band gap devices, with lesser deliberations in GaN for attaining the higher stand-off voltages, which may as well have profits that Si-based or electromechanical power gadgets can't achieve. The higher stand-off voltages may as well dispose of the necessity for arrangement stacking of gadgets and the co-partnered bundling challenges. [11].

The sapphire and silicon wafers can be easily utilized as substrates to grow GaN devices compared to the usual SiC substrate for cost efficiency. GaN due to its properties such as higher breakdown can be operated at elevated temperatures. Over the time of development and research pertaining to GaN we can even now use it for many other

application except the military applications. Initially due to high cost for fabrication GaN was limited to RADAR, warfare and communication systems with high security. The reduced cost for development of substrate and wafer for GaN have made it a very considerable semiconductor material for wide commercial applications.[12]. Most of the work on GaN is generally based on Monte Carlo simulations or experimental. Another considerable model that is the semi empirical model of GaN based MESFET utilized for small signal environment, the MW transistors are generally simulated by admittance and scattering parameters. [13]

The DC attributes of GaN MESFETs with length of gate as 4m have been as of late reported, the gadget manufacture and microwave exhibition with length as small as 0.7μm GaN MESFETS where the engaged channel was developed on an exceptionally resistive GaN layer. GaN epi-layers are developed on orientation as (111) using crystal diamond substrate by NH_3source atomic beam epitaxy [14]. The GAN band edge is focused at 3.469 eV with a line width of 5 meV and the aforementioned effects exhibit that GaN hetero-epitaxially developed on jewel opens new spaces for heightened power electronic provisions [15].

1.1 Potential Factors that make GaN Highly Favorable for Microwave Frequency Applications:-

The GaN material has remarkable electronic properties. This material was broadly explored for utilization in elevated power RF transistors. The wide band property of this material permits heightened supply voltages and heightened temperature requisitions.

In the previous many years, developing of wide band gap materials for example GaN in view of its lesser thermal generation rate and elevated breakdown field for its potential utilization for elevated power, elevated temperature and microwave frequency use. Military based applications have a great interest in GaN based high power and efficient semiconductor materials devices. GaN Metal Semiconductor Field Effect Transistors (MESFETs) have accepted much consideration as its structure is less difficult to examine than that of High Electron Mobility Transistors (HEMTs) and its epi-layers and the physical impacts are simpler to acknowledge and decipher. Simple physics based

analytical models are required to be developed for various parameters of GaN in order to use it vast potential in semiconductor electronics. This will give a new dimension to computer–aided digital design of GaN ICs.[16]

Chapter 2
MOTIVATIONAL FACTORS FOR GaN POTENTIAL

2.1 Properties of GaN

Gallium nitride is a semiconductor material with various properties which make it very potential and preferable for high power and speed applications. It has a high avalanche and wide band gap which makes it even feasible for harsh environments. It is also very stable and has a good thermal conductivity which makes it suitable for high power, high temperature electronic device. A peak electron velocity of $2.4*10^7$cm/sec is predicted by Monte Carlo simulations which is suitable for high frequency devices. The fabrication simplicity and because of less dopant diffusion problems as compared to its counterparts makes MESFET a favorable device for very large IC's. Wide band gap semiconductors such as GaN/SiC offering larger electron mobility and thus increase in frequency operating rates makes them preferable over the still in use silicon in semiconductor industry. GaN offers integration with optical devices due to its direct band gap. This feature is the foremost reason for GaN to become one of the most favorable SC for modern industry and provides understanding of basic principles and operation. Boltzmann Transport equations are solved using the Monte Carlo simulations which help encountering hot electron effects that are present in GaN devices on a high scale. The comparable carrier motilities offered by SiC to GaN has made it suitable for fabrication of optical switches.[17]

Research is being conducted to develop power devices based on gallium nitride with minimum on resistance and higher breakdown voltage than silicon based devices. Since the specific on resistance is inversely proportional to third power of breakdown electric field therefore these devices have the specific on resistance which is three orders lower than the silicon devices.[17]

The fabrication of electronic devices based on GaN as for p-n junction diodes, schottky barrier diodes is done by growth of a hetero-epitaxial layer on substrate like SiC and sapphire. A good crystalline structure of gallium nitride cannot be realized. At a high density between 10^9 to 10^{10} cm^2 there will be lattice mismatch and a dislocation in GAs epitaxial layers due to difference in thermal expansion coefficients. So it can be presumed

epitaxial layers grown on GaN being used on a substrate are more pure and have lesser dislocation density. The main disadvantage of electronic devices from silicon, GaAs and their alloys is that they are incompatible at higher temperature and mordant environment. But the devices having a wide band gap are free from these short comings. [18]

2.2 Various Parameters of GaN

Parameters	Units	GaN
Symmetry	-	Wurtzite/ zinc blende
Density	g/cm	6.15
Static Dielectric Constant		8.9
High-Frequency Dielectric Constant		5.35
Energy Gap(Valley)	EV	3.39
Effective Mass(Valley)	M_e	0.20
Polar Optical Phonon Energy	MeV	91.2
Lattice Constant, a (c)	Å	3.189 (5.185)
Electron mobility	cm^2/Vs	1000

Hole mobility	cm^2/Vs	30
Saturation velocity	cm/s	$2.5x10^7$
Peak velocity	cm/s	$3.1x10^7$
Peak velocity field	kV/cm	150
Breakdown field	V/cm	$>5x10^6$
Light hole mass	M_e	0.259
Thermal Conductivity	W/cm-K	1.5
Melting Temperature	O_C	2530

The factor that made GaN very helpful for microwave applications are given below:-

1) High electron mobility– GaN has very high electron mobility which makes it most suitable for high frequency applications as compared to SiC and Si.

2) GaN has comparatively low dielectric constant and large thermal conductivity pathways.

3) The bond strengths are strong which makes melting point for GaN to be high .this gives high reliability.

4)Withstand harsh environment- Chemical etching have minimal effect on nitrides which allows GaN to be operated in harsh environment.[19]

2.3 Comparison between R_{on} and Breakdown Voltage of Different Materials

Specific-on-resistance, R_{on} is the total resistance that the current experiences while flowing from source to drain. Lower R_{on} is required for a MESFET to perform efficiently.

From Figure 2.1 we can see that GaN has the least R_{on} for higher breakdown voltage which is desirable for the operation. [20]

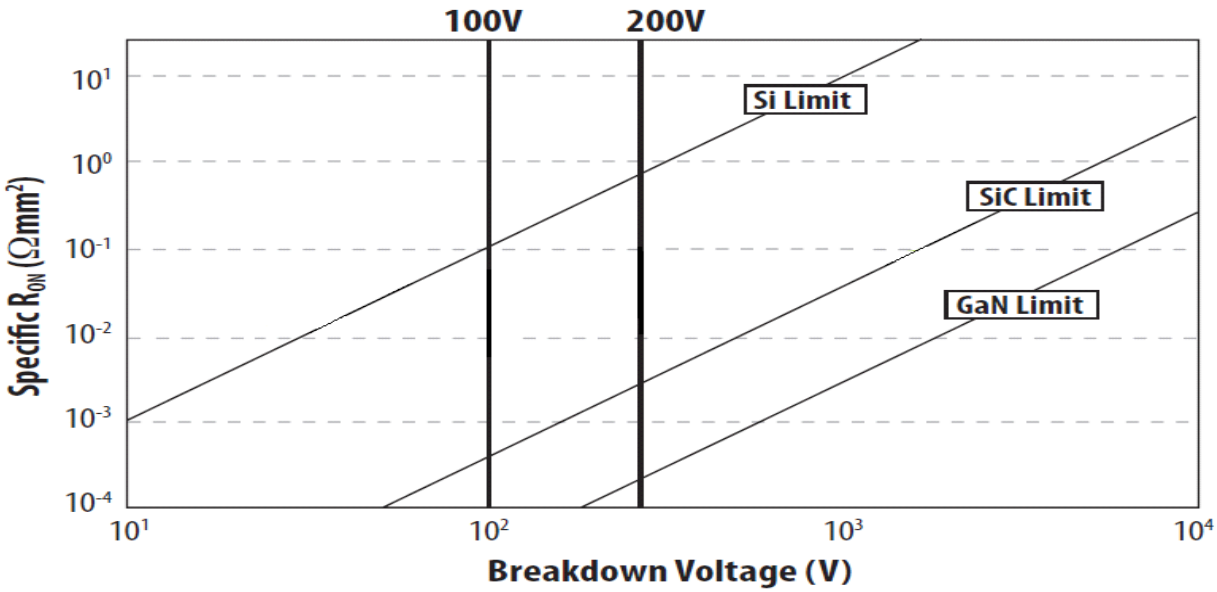


Figure2.1Specific resistance R_{on} vs. Breakdown voltage

2.4 Potential Performance of SiC and GaN based MESFETs

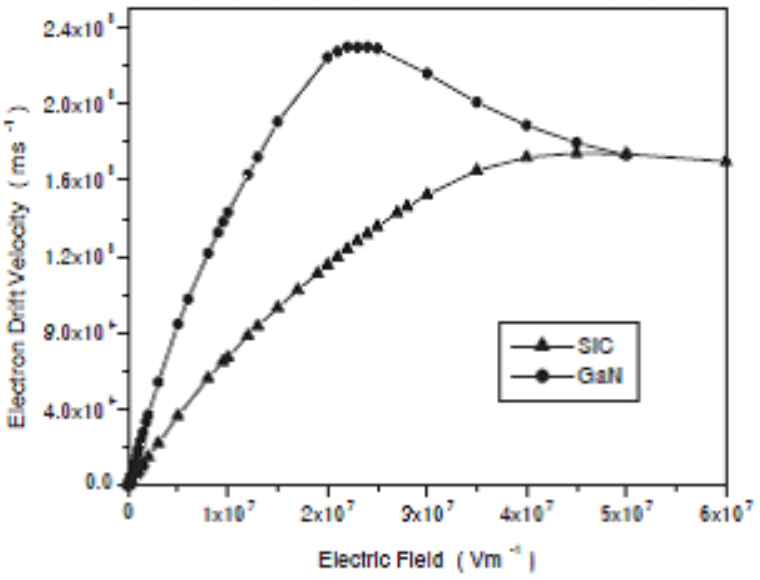


Fig2.2a depicts the graph between drift velocity and electric field for Sic and GaN

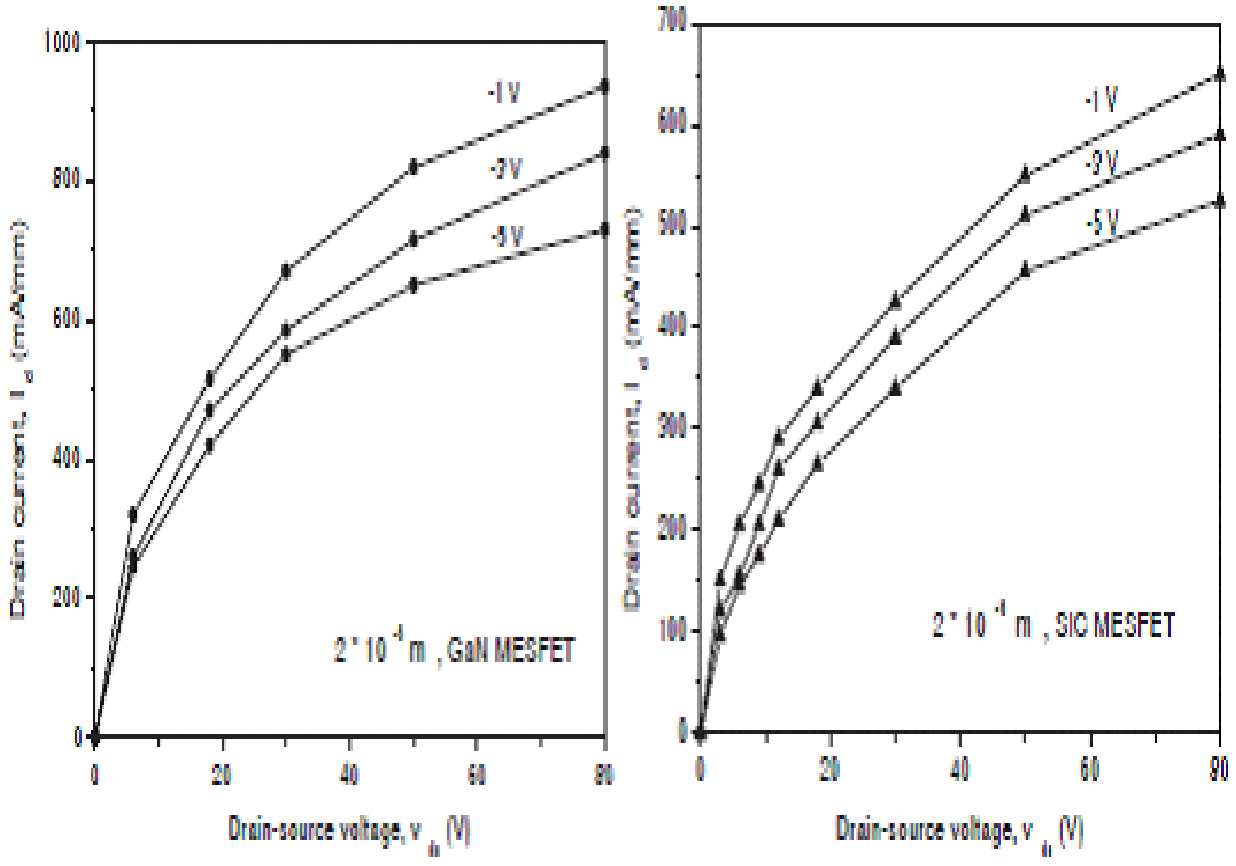
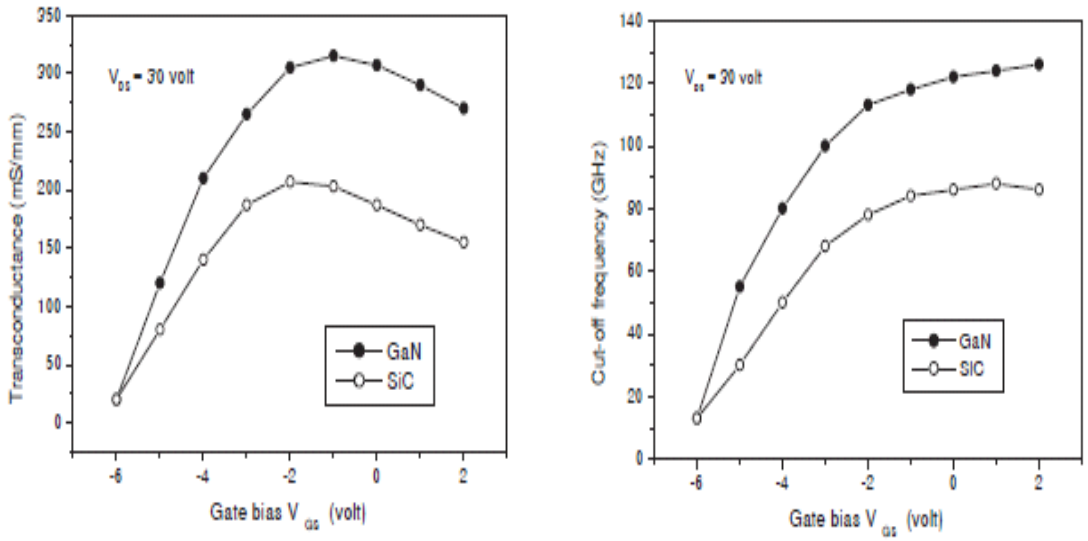


Figure2.2b Static I-V characteristics between 1V to -5V GaN and SiC MESFETs

In the Figure 2.2a and 2.2b the figured Ids (Vds, Vgs) attributes are introduced for both GaN and SiC MESFET. The procured aspects are generally indistinguishable fit as a fiddle. For both structures we can see that the yield conductance is generally heightened and even at a hefty negative gate bias the mechanism is not by any means squeezed off. The aforementioned two impacts happen because of the short channel impacts and solid electron infusion in the support layer. We can acquire towering I_d, drain current for both the structures which affirms us that GaN or SiC MESFETs are handy for heightened power provision. Besides, GaN has the preferred electronic transport lands over SiC. Subsequently the GaN based MESFET demonstrates 70% higher drain current density as contrasted to the SiC MESFET. Unmistakably it is viewed from the figure that, as the device length is lessened, higher drain currents are arrived at therefore of the expansion in longitudinal electric field and velocity overshoot effects [21].



Figures2.3a and Fig 2.2b above show us transconductance (g_m) and cut-off frequency (f_c) versus gate voltage V_{gs} at a constant V_{ds} for both structures

Figures2.3a and Fig 2.2b show us transconductance (g_m) and cut-off frequency (f_c) against gate voltage V_{gs} at a constant V_{ds} for both structures. It is demonstrated that a higher drain current density for GaN along with superior electronic properties. In this manner, GaN MESFETs displays 70% higher transconductance and cut-off recurrence. The aforementioned outcomes indicate that GaN MESFETs might perform well for heightened frequency and elevated power provisions [22].

2.5 Pulsed Measurements of GaN MESFETs

The GaN material has outstanding electronic properties. This material was widely investigated for use in high power RF transistors. The wide band gap of this material allows high supply voltages and high temperature applications. But till now all the electrical properties of the device were not entirely understood [23].

2.6 DC Measurements

Static I-V measurements are shown in Fig2.4 for two different lighting conditions. For a V_{gs} of 1V and a V_{ds} of 18V, the transistor exhibits a drain current of about 305 mA/mm with light and 270 mA/mm without light. This difference can be explained by

the existence of electrical traps located in the material or at the surface. Further measurements were underway in order to determine their location [24].

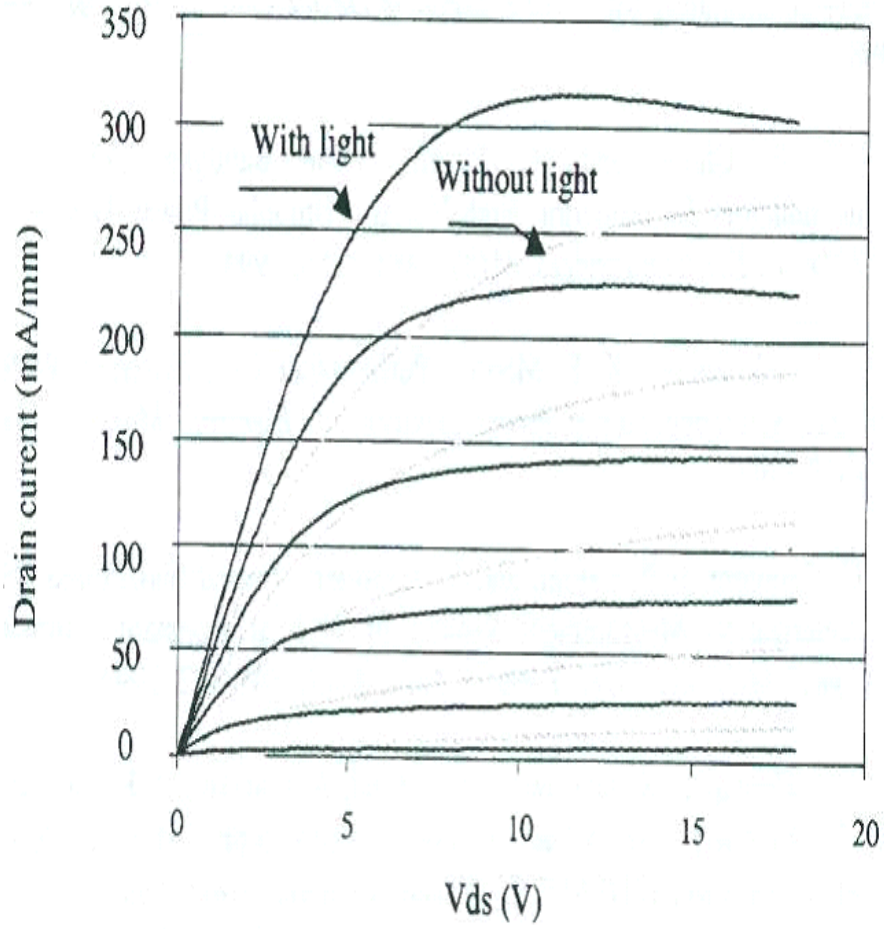


Fig 2.4 DC I-V characteristics of a 2x50x0.3µm2GaN MESFET with and without light

2.7 Static Pulsed Measurements

Pulsed measurements were also performed on the same device. Figure 2.5 shows the pulsed I-V characteristics with and without lighting for a dormant bias voltage of V_{ds} = 18 V and V_{gs} = -9V. From the figure 2.5 we can see that the maximum amount of drain current obtained without the presence of light is less than half of the current obtained under static conditions. As a result, this loss confirms us about the presence of electrical traps. [25]

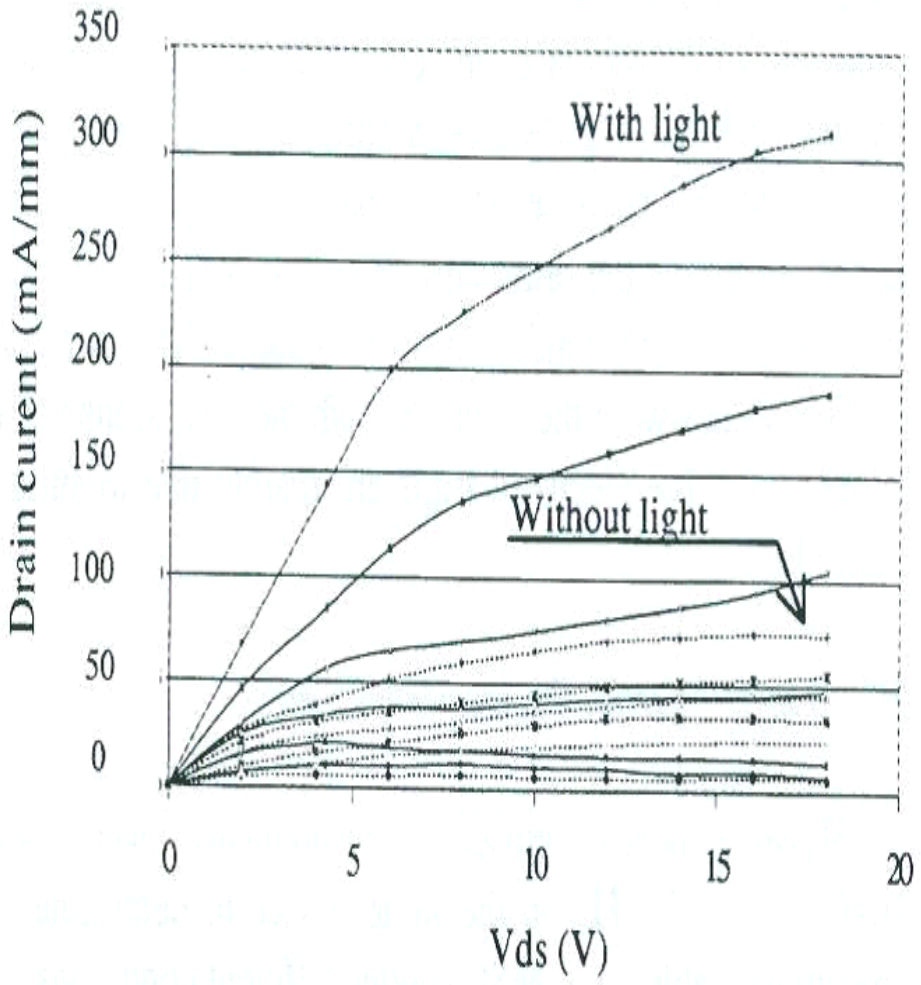


Figure2.5 Pulsed I-V characteristics of a 2x50x0.3µm2

2.8 Kelvin Probe Force Microscopy to demonstrate potential distribution of cross section for GaN FETs

Kelvin probe force microscopy is a powerful measurement technique that can be used to determine the two dimensional electrical potential distribution. It has been used to investigate the potential of GaN-based FET at an operating state. The investigation has been carried out on a cleaved surface of an AlGaN/GaN HFET without and with SiNX passivation layer by using KFM under several device operation conditions and influences of the passivation effect on the electric field distribution has been discussed [26]

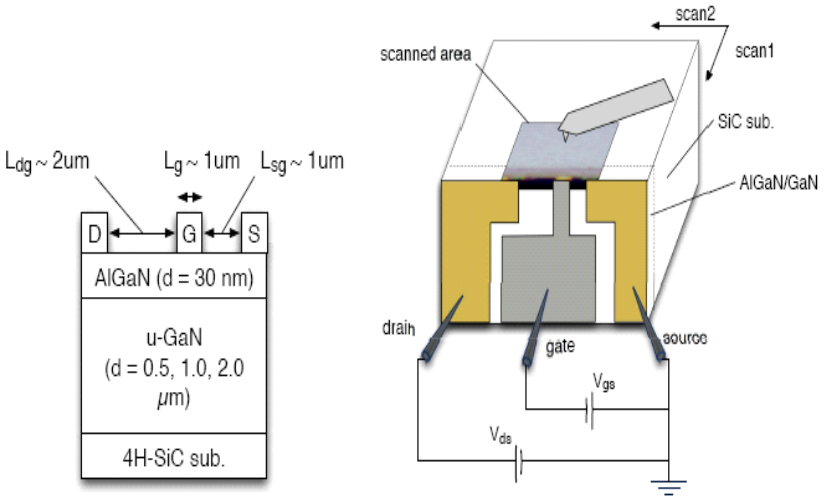


Figure: 2.6 Schematic cross section of (a) fabricated FET structure and (b) diagram of the KFM measurement system [26].

Figure2.6a and 2.6b show a created FET gadget structure and schematic outline of the KFM estimation framework utilized for the examination. It is viewed that source and channel ohmic contacts comprising of Ti/Al/Ti/Au layered structure and a gate Schottky contact comprising of a Ni/Au were structured on the example surface. The gate length Lg, was about 1µm. The source-gate separation, Lsg, and the gate channel separation, Ldg, were around the range of 1 um and 2 um, individually. FET structures with and without passivation by SixNy was ready further bolstering explore good fortune of surface passivation. [27]

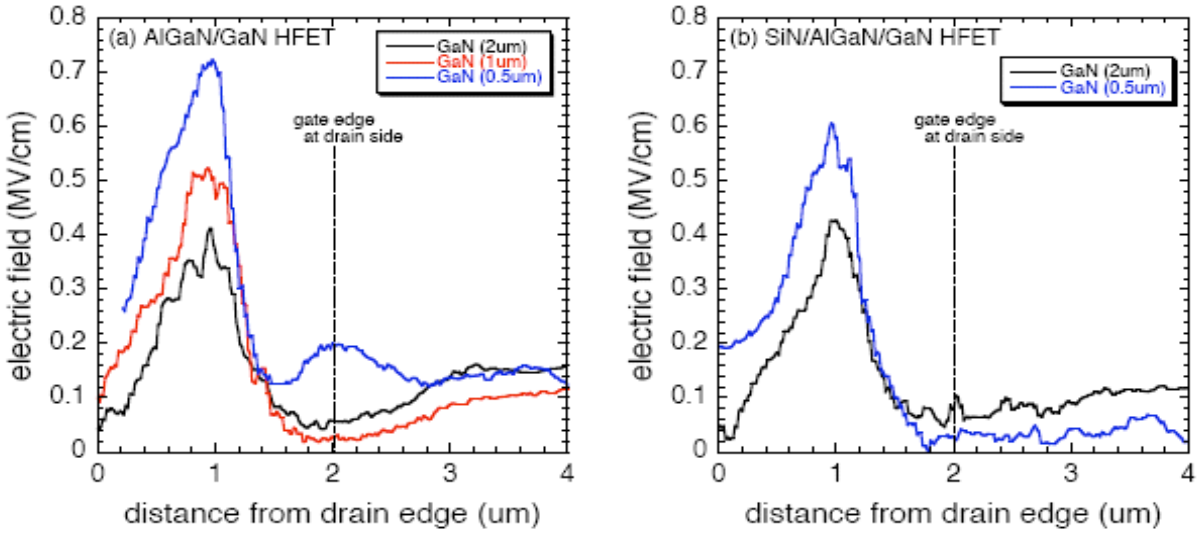


Figure2.7a and 2.7b Electric field distribution between the drain and source edges near the surface of AlGaN/GaN HFET (a) without and (b) with SiNx passivation layer.

Electric field is concentrated at the midpoint of the drain and gate electrodes. Figure 2.7 shows a comparison of a profile plot of distribution between the drain and source of electric field near the surface of AlGaN/GaN HFETs (a) without and (b) with the SiNx passivation layer. In both cases, the maximum intensity of the electric field at the surface is seen to be increasing with decreasing GaN buffer thickness. Also, the maximum electric fields in passivated AlGaN/GaN HFETs are the same or slightly lower than in the non-passivated AlGaN/GaN HFETs. However, the electric field distribution near the surface of the passivated AlGaN/GaN HFETs is weak compared to the non-passivated AlGaN/GaN HFETs [28].

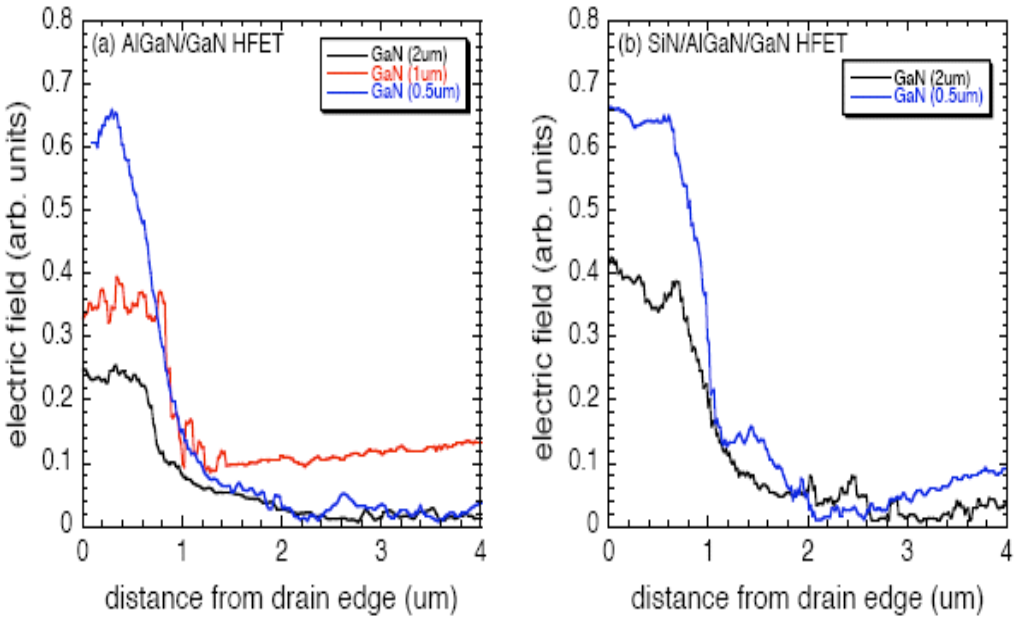


Figure:2.8a and 2.8bElectric field distribution between the drain and source edges at the mid-depth of GaN buffer of AlGaN/GaN HFET (a) without and (b) with SiNx passivation layer.

Figure2.8 shows an examination of the electric field conveyance at the mid-profundity of the GaN buffer layer from the channel edge to the source edge of AlGaN/GaN HFETs (a) without and (b) with the SiNx passivation layer. As perceived on account of the electric field close to the AlGaN/GaN surface, the electric field appropriation shows a tendency to build with diminishing GaN buffer layer. On account of a thick GaN bufferlayer

(GaN= 2um), the SiNx-passivated AlGaN/GaN HFET indicated a marginally stronger electric field concentration. [29]

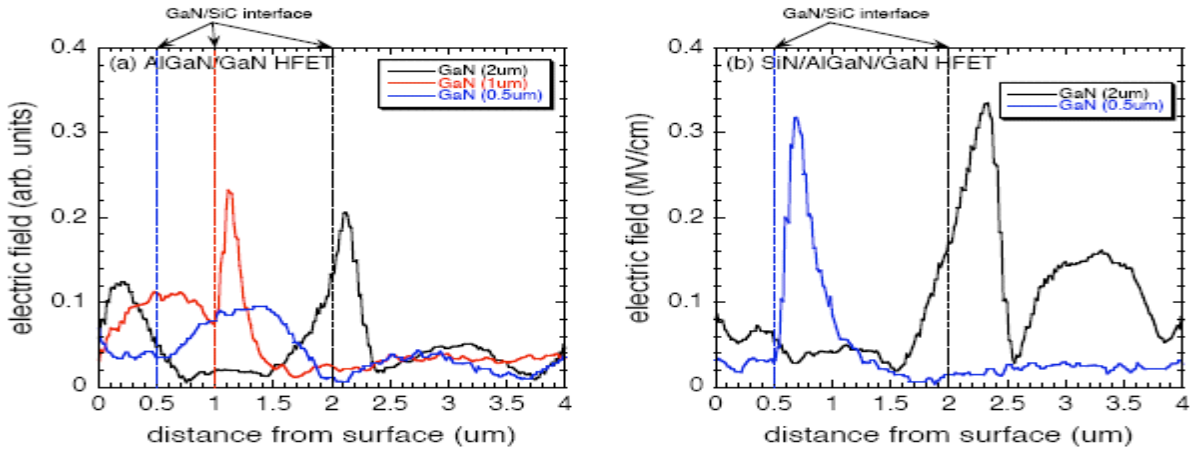


Figure2.8 Electric field distribution under the gate electrode of AlGaN/GaN HFET
(a) Without SiNx passivation layer. (b) With SiNx passivation layer.

Figure2.8 compares the profile plot of electric field distribution under the gate electrode of AlGaN/GaN HFETs (a) without and (b) with the SiNx passivation layer. In each sample, it is observed that the electric filed is concentrated on the SiC side near the interface between the SiC substrate and GaN buffer. It is demonstrated the highest intensity of the electric field is almost the same without being dependent on the GaN buffer thickness and slightly higher than that in the AlGaN/GaN HFETs without the SiNx passivation [30].

2.9 Double-Ion-Implanted GaN MESFETs with extremely low Source/Drain

Devices without ion implanted source/drain structure are conventionally used. Research with the aim to reduce the on-state resistance of MESFET so that the saturation drain current IDS and transconductance (g_m) can be enhanced, led to the finding of double-ion-implantation of GaN MESFETs. [31]

GaN FETs are known to be a wide bandgap semiconductor material with a high breakdown electric field, high saturation drift velocity and better thermal conductivity in

comparison with the more commonly used GaAs and SiC MESFETs. To increase the efficiency of such devices, some properties may be adjusted in order to obtain, much better results, one of such properties being the on-state resistance of the device. A reduction in the on-state resistance will result in increased saturation drain current and increased maximum transconductance. This can be achieved by producing high concentration layers below the source and drain contacts.

One of the processes for fabricating high concentration regions is known as ion implantation for impurity doping. The resulting structure of GaN MESFET is shown in Fig2.9 due to ion implantation of both the channel and drain/source [32].

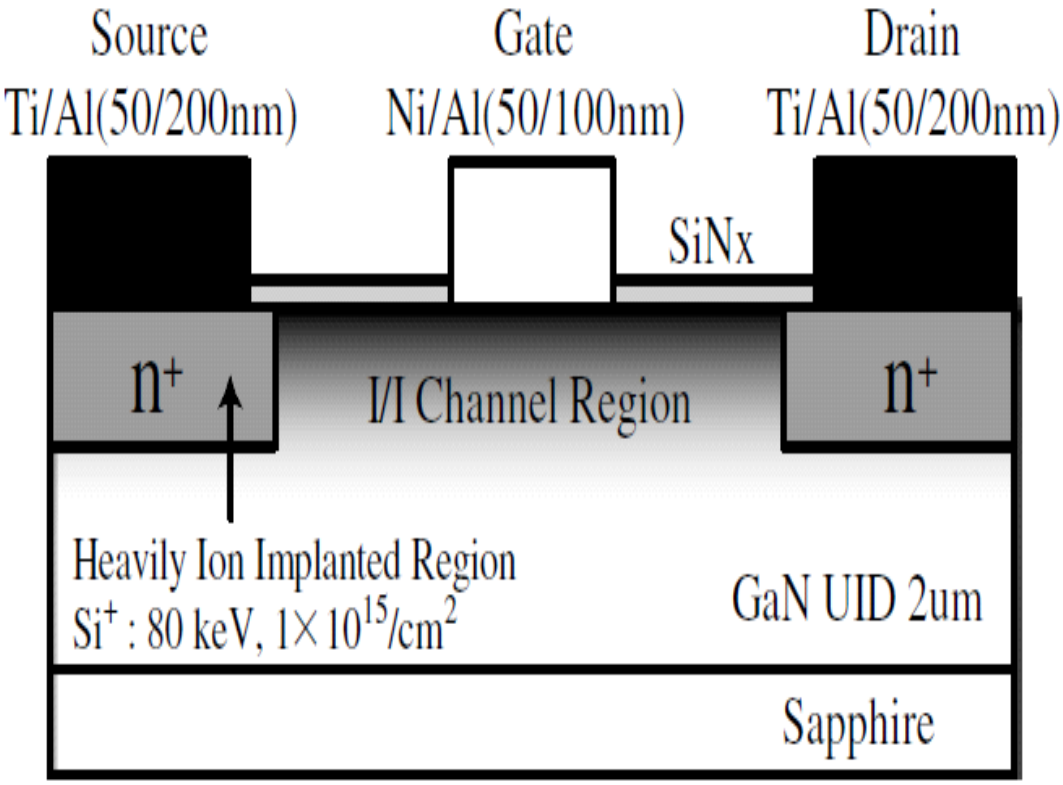
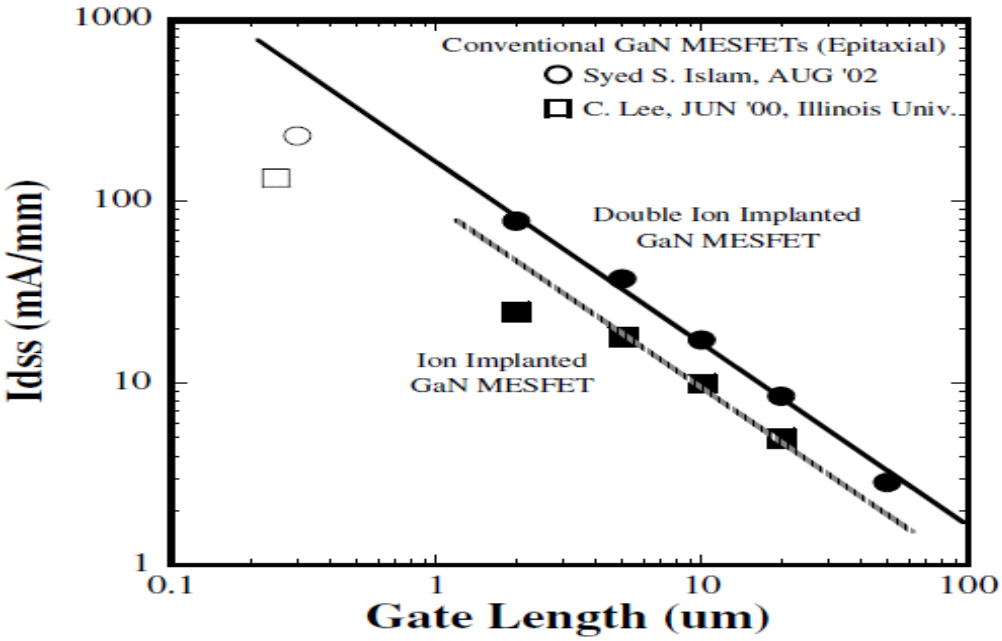


Figure2.9 GaN MESFET structure with ion implanted channel and source/drain regions (Double Ion Implanted GaN MESFET)

With disadvantages involved in this process, to minimize the damage caused by ion implantation, the process is carried out in very high temperatures. For instance, the

activation and crystal damage recovery of an implanted GaN will require annealing at temperatures above 1500 °C.



Experiments were carried out to study the changes of the on-state resistance by utilizing the circular transmission line (C-TLM) to analyze the outcome of ion implanted source/drain regions, or double-ion-implantation.

The following are the graphical results obtained from research and experiment. The results for double-ion-implanted (DII) MESFETs have been compared with that of ion-implanted-channel (IIC) MESFETs, where the drain/source regions are not as heavily doped [33].

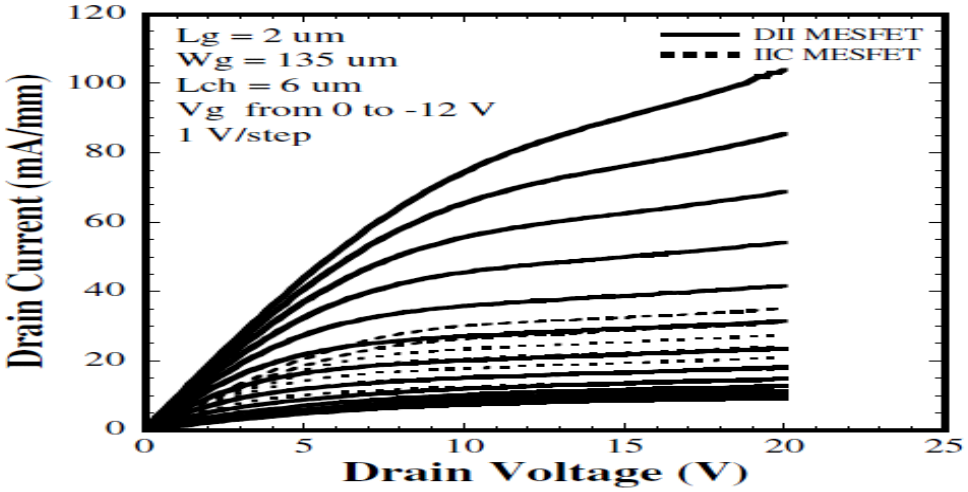


Figure2.10Ids-V_{ds} characteristics of DII MESFET and CII MESFET

Figure2.10 illustrates how drain current, I_d for DII MESFET is much greater than that obtained with IIC MESFET for a specific value of drain voltage, V_{ds}. An increase in drain voltage increases the drain current. The inverse of the slope of the I_d-V_{ds} characteristic curve in its linear region is defined as the source/drain resistance of the device. As seen from the figure, for a particular range of drain voltage and its corresponding drain current, the slope of the curve is greater for DII MESFET as compared to IIC MESFET, implying the drain/source resistance is much smaller for DII MESFETs. [34]

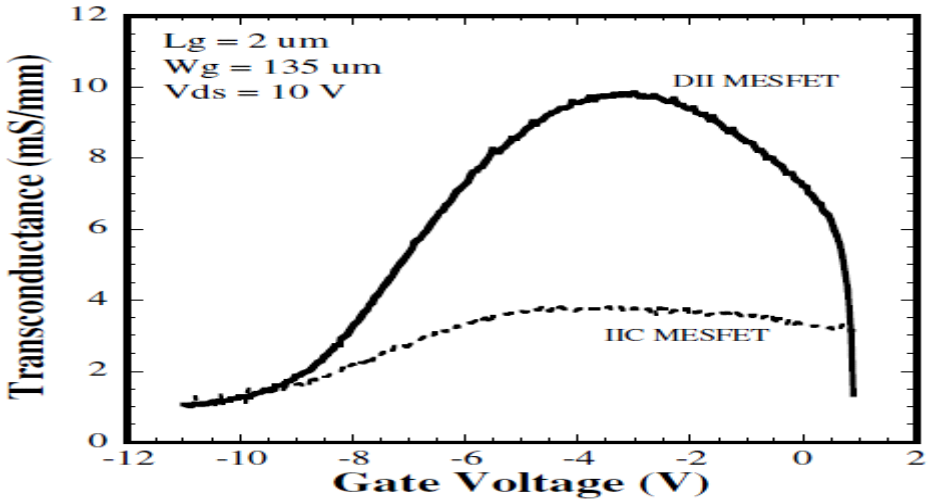


Figure2.11 Transconductance of DII MESFET and IIC MESFET

Figure 2.11 show that transconductance (g_m) is much greater for a DII MESFET than that for an IIC MESFET, with a variation in the gate voltage of the MESFETs.

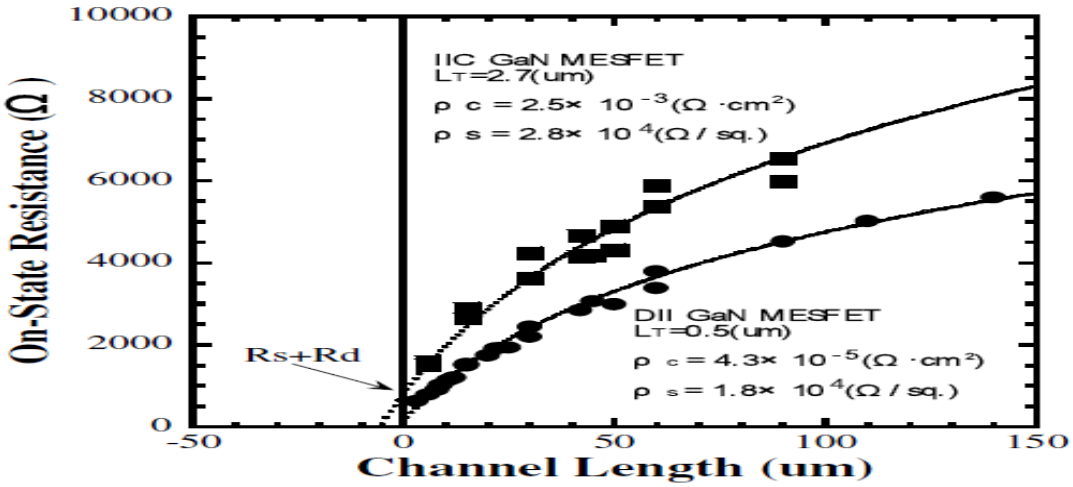


Figure2.12 Specific On-state resistance of ion implanted GaN MESFET

The illustration above involves the variation of the specific on-state resistance as a function of channel length. The on-state resistances in a MESFET involved are illustrated in Fig.2.13

Where,

R_{ch} = channel sheet resistance

R_s= parasitic source resistance

R_d= parasitic drain resistance

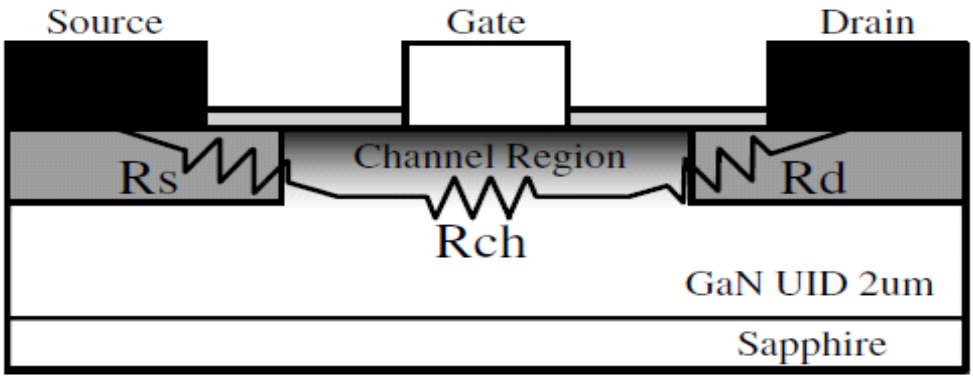
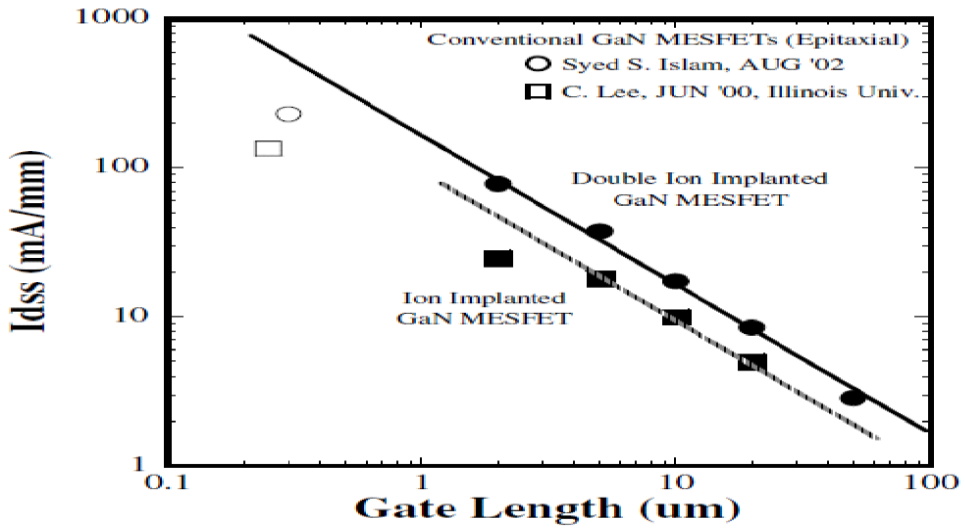


Figure2.12 On-state resistance components of ion implanted GaN MESFET [25].

R_{ch} was found to be of same value for both DII and IIC MESFETs, but with lower values of R_s and R_d. This shows that highly doped ion-implanted source/drain regions minimizes the resistance between the metal and source/drain regions, sheet resistance of highly-doped-regions, and the sheet resistance of implanted-channel-regions between the gate and heavily doped regions. [35]

Figures2.13 below represents curves showing the variation of I_{dss} and g_{mMAX} with changes in the gate length of the device. One way of increasing the values for I_{dss} and g_{mMAX} is reducing gate lengths to submicron order. For further improvements in these two parameters, a reduction in the on-state resistance is essential, especially when such devices are used for scaling purposes.



Figures2.13represents curves showing the variation of I_{dss} and g_mMAX

As a result of the mentioned adjustments made on a MESFET, the following conclusions have been drawn:

Increase in I_{dss} = 200%

Increase in g_m = 200%

Decrease in source/drain resistance = 94%

These were the figures obtained: Saturation drain current increases from 36 mA/mm to 78 mA/mm Maximum transconductance increases from 3.8 mS/mm to 10 mS/mm and On-state resistance reduces from 210 ohm-mm to 105 ohm-mm. [37]

2.10 Limitations in growth of GaN

One particular inconvenience in the advancement of GaN slim films is the unavailability of sufficiently endless (>1 cm) single valuable crystals for usage as substrate for homo-epitaxial advancement. In this way up to now, hetero-epitaxial improvement has been important need and the choice of substrate is essential. Viable substrate materials may besides have less thermal growth and the cross sectional part for the used crystal. Moreover, they should be unaffected by the improvement sciences (for instance NH_3 or H_3) at uplifted improvement temperatures (in richness of 1000 Degree Celsius in certain cases). Under the previously stated stipulations, sapphire Al_2O_3 and SiC are the most

exceedingly potential substrate materials used at this time. The focus when hexagonal GaN is improved on the (0001) basal plane of Al_2O_3, a grid confound of ~13% exists at the infrastructure temperatures. The extra strain is proportional to the matrix between 6H-SiC and GaN, and outcome is tantamount division densities observed.[38] Today, SiC substrates, notwithstanding all the more over the top, are of developing venture for hoisted temperature uplifted power electronic creations like transistors in light of their extraordinary thermal conductivity and feasibility of n-and p-sort doping. The materials with an adjacent grid match with GaN, were furthermore used for epitaxial substrates. Moreover, the improved GaN cannot offer the needed electronic properties as a result of either the pitiless infrastructure or unintentional contamination from the substrates. The ideal contender substrate is doubtlessly a GaN wafer. However industrially primed incredible zone GaN wafers have all the reserves of being in any case an away. The nitride aggregation is, thus, tested with growth of hetero-epitaxial films having incomprehensible MISFITs [39].

A variety of epitaxial thin film structures can be fabricated using a number of routine incorporations like molecular beam epitaxy (MBE), metal organic concoction vapor deposition, HVPE etc. In the past years, MOCVD has improved as a heading framework for readiness of III-V nitrides optoelectronic and microelectronic growth. A superior accomplishment is the formation of super shiny blue LEDs. Parts of this framework join the use of elevated immaculacy substance sources, a lifted level of synthesis control and uniformity, increased advancement rates, encroaching scale collecting potential and the proficiency to advance sharp intersections [40].

At the earlier stage of using GaN for its high potential there was a hindrance due to crystalline defects as the growth of the material was done on sapphire and SiC substrate. The main defect was that through the thin film there are few vertical threading from the substrate interface. The 3D – growth mode induces a rough surface on the wafer. An astonishing improvement was marked when Amano (1986) succeeded to develop GaN morphology by depositing a slim layer prior to high temperature growth on AlN buffer. This also improved the electrical and optical properties of the material. There is decrease in the interfacial free energy between the substrate and film. Thus, the serve as a template for growth and lateral growth of the GaN material is achieved. This buffer

has served the purpose for reducing lattice mismatch but still the defect is higher than other semiconductor materials on the order of one million times. These slender films developed still have a threading defect ranging from 10^9 to 10^{10} cm^2.The questionable part of these structures with defect the long term stability although it has minimal effect on the output optical and electronic devices. The defects of GaN structure need to be diminished in order to attain the full potential of GaN semiconductor material. [41]

There was further improvement achieved in 1994, by employing a technique known as Lateral epitaxial overgrowth (LEO). This technique reduced the structure defects to an extent. Further etching is used to make windows to the underlying layer of GAN. This is followed by re-growth of GaN film by attaining such condition that there is no growth on the mask. Instead an epitaxial growth on GaN windows is achieved. By this method the dislocation in threading are subsequently reduced on GaN on the mask. A range of 104 – 105 is achieved for the density of dislocations over the surface of LEO GaN. Furthermore, there is still a noticeable high level of threading defects over the window region.[42]

2.11 Defects in a bulk GaN

At high temperature range of 1500 – 1800 K under the high pressure conditions i.e. up to 20 Kbars a solution of atomic nitrogen is used in liquid gallium to grow GaN bulk crystals. The size parameter is 1-3 mm in lateral size and thickness is around 0.1 – 0.5 mm for platelet shape GaN. These structures are usually in elongated hexagon shape. The surface of the platelet is parallel to c-plane. Also, the longest dimension is along the axis. The roughness is the contrasting factor between two platelets. In one platelet there is atomic roughness while the other is atomically rough. The defect percentage was that between 70 – 90 percent of platelet was defect free. [43]

The defect density of the surface depends mainly on the roughness of the surface. Blank has clearly described the Wurzite structure with its basal and prismatic faults. The number of basal fault is almost equal to the local transitions between the hexagonal to cubic structure. This is very clear from the crystallography point of view and the former transition is within (0001) point of view. There are different orientations for GaN bonds. They have mirror symmetry for hexagonal GaN symmetry. On the other hand it is rotated

600 in cubic structure bond in relation to closest neighbor and there is a 2H to 3h change in crystal structure. [43]

The harsher the surface, the higher was the imperfection thickness watched. Arrangement of SFs is recognized as a development error. The structure of basal and kaleidoscopic blames in wurtzite has been portrayed by Blank. From a crystallography outlook the basal issues are identical to neighborhood moves from the hexagonal to the cubic structure inside a couple of (0001) nuclear planes. In hexagonal GaN the bonds have mirror symmetry while in the cubic structure bonds are turned 600 as for closest neighbors. The neighborhood change of gem symmetry is from 2H to 3C. The figure 2.14a underneath shows three sorts of (I1, I2 and E) of basal stacking blames watched in the mass GaN with one, two and three cubic bi-layers, individually. Every bi-layer of the cubic GaN is arranged in some sort of three conceivable positions relegated as A, B, C containing perfect stacking grouping of ... ABCABC ... rather in hexagonal GaN every double layer has just two conceivable positions, A and B, with the ideal succession being...ABABAB... [44]

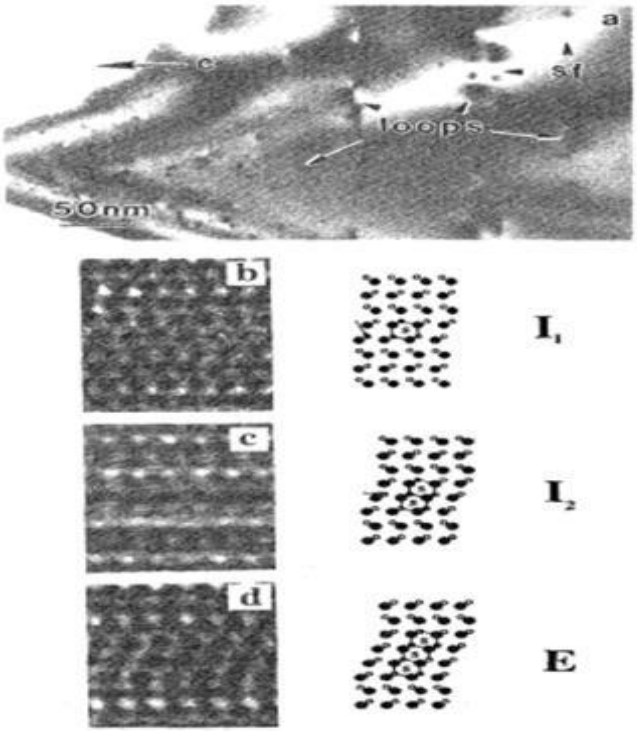


Fig 2.14a shows three types of basal stacking faults (b-d) observed in such a region

2.12 Defects in Epitaxial GaN Crystals

The most common defect in GaN crystal bulk is that there are dislocations parallel to c-axis. There are other defects such as stacking faults but the former is most prominent as shown in Figure.2.14b. A columnar structure is formed as such an arrangement of dislocations is formed in epitaxial layer of GaN. This arrangement is a network of many small angle boundaries. The growth conditions are responsible for the defects in epitaxial GaN as compared to its bulk. A high lattice mismatch is observed in epitaxial GaN as it grows on the substrate in the c- direction. Further, there is thermal mismatch as well. The propagation of most defects in the growth direction is followed by its origination at the interface. There is large number of vertical dislocations in the direction of c-axis. Due to these dislocations long distance propagation for SFs in the epi-layer is hindered. Thus the length of the SFs is very small in epitaxial GaN as compared to bulk. [45]

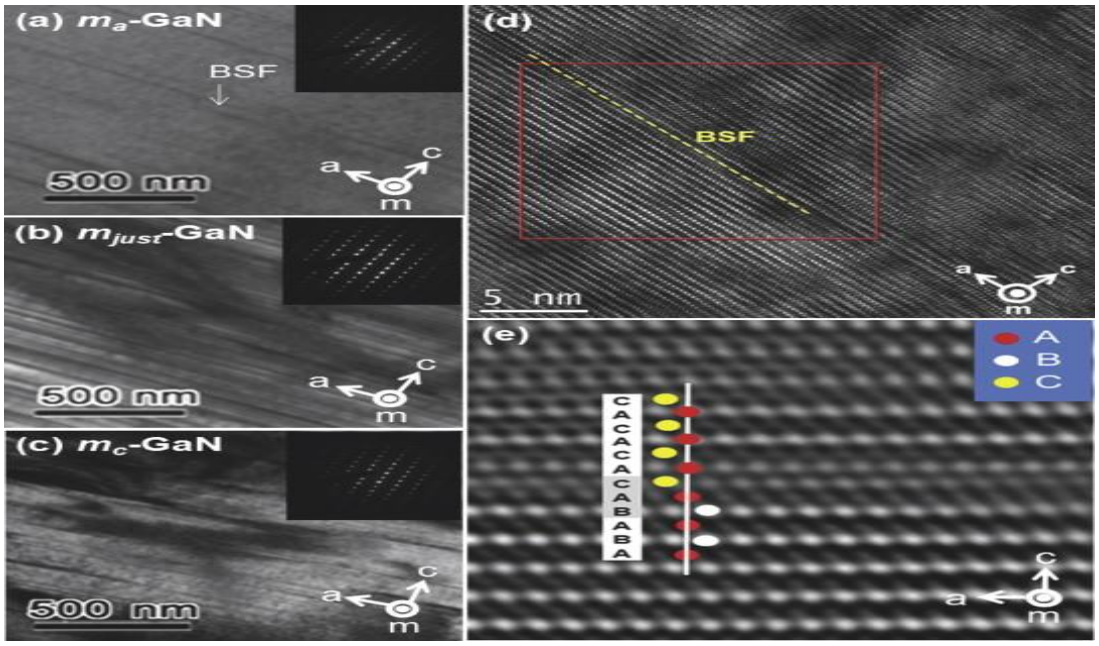


Fig 2.14b Depicting defects in GaN

Most of the dislocations are originated at the interface. Moreover, the number of dislocations is very large at the interface. The interaction of the dislocations results in annihilation. During the initial stages of GaN growth propagation of threading dislocation is possible. Such defects can be considerably reduced using a buffer layer due to which

the substrate roughness is reduced. The diffusion of nitrogen into the substrate due to the application of buffer layer can helps in reduction of disorientations at interface of GaN. A "mosaic" structure AlN buffer is very commonly used. There are perfect orientations in AlN buffer in c-plane. The structure of this buffer has disorientations around c-plane. These disorientations are small crystalline sub-grains. The usage of buffer impact the threading dislocations in GaN. The result is the formation of tilt and twist containing small angle boundary network. [46]

The Hall mobilities and carrier concentration directly affect the conductivity of GaN. A relatively high value of Hall mobilities is preferable for device applications. Figure 2.15 below is demonstrating the electron mobility for n-type GaN. These results are obtained from Monte Carlo simulation. The effect of defect and considerable impurities is clearly illustrated by the figure 2.15. [47]

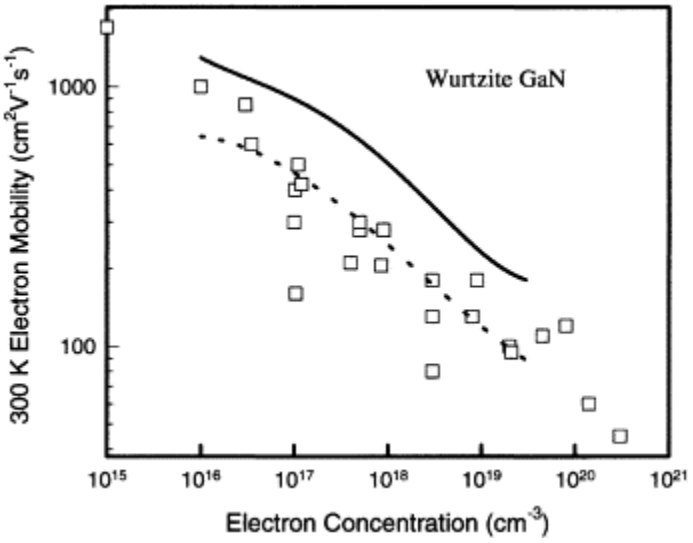


Fig 2.15 shows a survey of 300 K GaN electron Hall mobility values as reported by various groups

The strong line shows the figured comes about for uncompensated n-GaN. The III-V nitrides are needed to be made p-sort by substituting Column II components for example Zn, Mg Be and Ca on for Ga locales to shape single acceptors. Then again, all of the aforementioned divalent components shape profound acceptors, the shallowest being Mg with ionization level of 0.17 eV which is still numerous kTs above the valence band

edge of GaN. At this acceptor level, one might as well just need <10% of the Mg particles to be ionized at room temperature, which connotes the Mg focus ought to be roughly two-requests of size bigger than the coveted gap fixation. The point when MOCVD is utilized as the development technique, it has been challenging to get p-sort conductivity. It was later discovered that hydrogen plays a significant part in passivating the Mg acceptors, and makes an unbiased complex Mg-H that counteracts the establishment of gaps in GaN [48]. It was first demonstrated by Amano, that p-sort conductivity might be attained by initiating Mg-doped GaN utilizing flat vigor electron light. Nakamura showed accordingly that the actuation of Mg can likewise be acknowledged by thermal annealing at ~7000 C. Note that MBE developed GaN doped with Mg may be p-sort without a thermal actuation prepare, due to the nonappearance of hydrogen and H-N radicals throughout development. Also, p-sort doping was additionally accomplished by insert of Ca or Mg into GaN, emulated by elevated temperature annealing (~11000 C). The most noteworthy gap fixation reported so far is ~1018 cm3 , and the ordinary opening portability is exceptionally level, frequently 10 cm2/Vs or beneath, yet permitting the acknowledgement of p-n intersections. Accomplishing level safety Ohmic contacts to the GaN layers with unfortunate p-sort doping fixations has ended up being troublesome. As of late, Brandt considered that by repaying be with O, a 19 nonpartisan dipole is shaped that does not scramble the gaps. Henceforth record towering gap portability of 150 cm2/Vs was gotten. This may be the perfect contact layer for GaN based units needing a p-sort ohmic contact. [49]

2.13 Applications of GaN

1 Military Applications – Wireless communications is one potential field where demanding performance of MW frequencies is filled by GaN and SiC due to their wide band gap.

2 Also if we consider a transmitter the bottleneck is the PA development. GaN and SiC are most suitable here to fulfill wide band gap requirements.

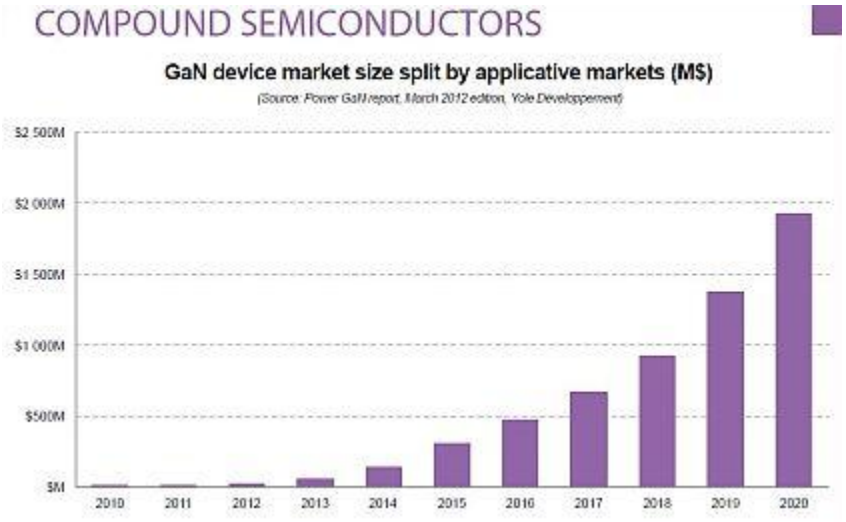
3 Telecommunication industry- Next generation mobiles satellite communications, broadcasting devices require very high efficiency and wider band width. To reduce the antenna size we need our systems to operate at a high power and frequency.

4 Broadband and Wireless industry – these high frequency and power applications require semiconductor devices with high electron mobility, thermal conductivity which makes GaN very suitable.

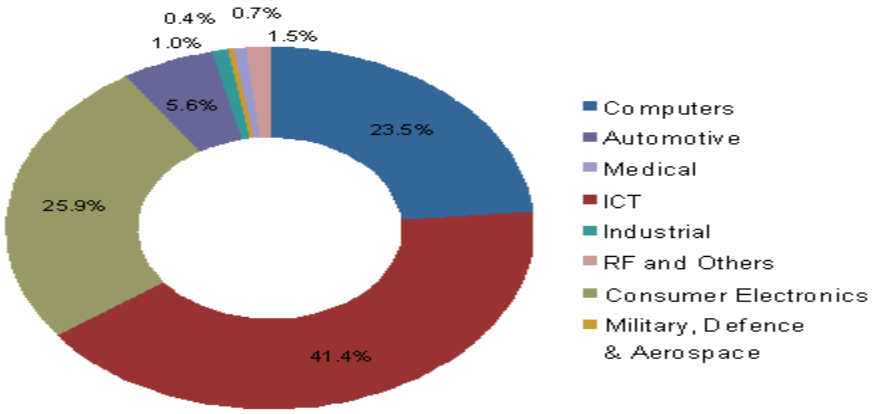
5 Another important advantages is because of it high breakdown voltage it is operatable at high voltage and thus reduces the need for voltage conversion. It increases the efficiency.

6 Semiconductors like GaN and SiC with wide band gap has high output power density which makes them highly potential for fabrication of small size devices.[50]

The bar chart below shows the GaN market size split in various applicable fields:-



The figure below shows the various market split of GaN :-


0.4%
0.7%
1.0%
1.5%
5.6%
23.5%
25.9%
41.4%
Computers
Automotive
Medical
ICT
Industrial
RF and Others
Consumer Electronics
Military, Defence & Aerospace

CHAPTER 3

MESFET Technology and its operation

3.1 MESFET Device

MESFET is an abbreviation for metal semiconductor effect transistor. It is a unipolar device where the current conduction occurs by flow of majority carriers only. An n-type MESFET involves current produced by flow of electrons, while in a p-type MESFET, holes cause the current conduction. MESFET consists of a conducting channel through which the device conducts electricity. This channel is positioned between source and drain contacts, as illustrated in Figure 3.1. The flow of free carrier, and hence the current through the channel is regulated by adjusting the gate voltage which causes the thickness of the depletion layer to be varied underneath the metal contact. The Schottky barrier is a potential formed at the metal-semiconductor junction, which exhibits rectifying characteristics that makes it suitable to be used as a diode as well [51].

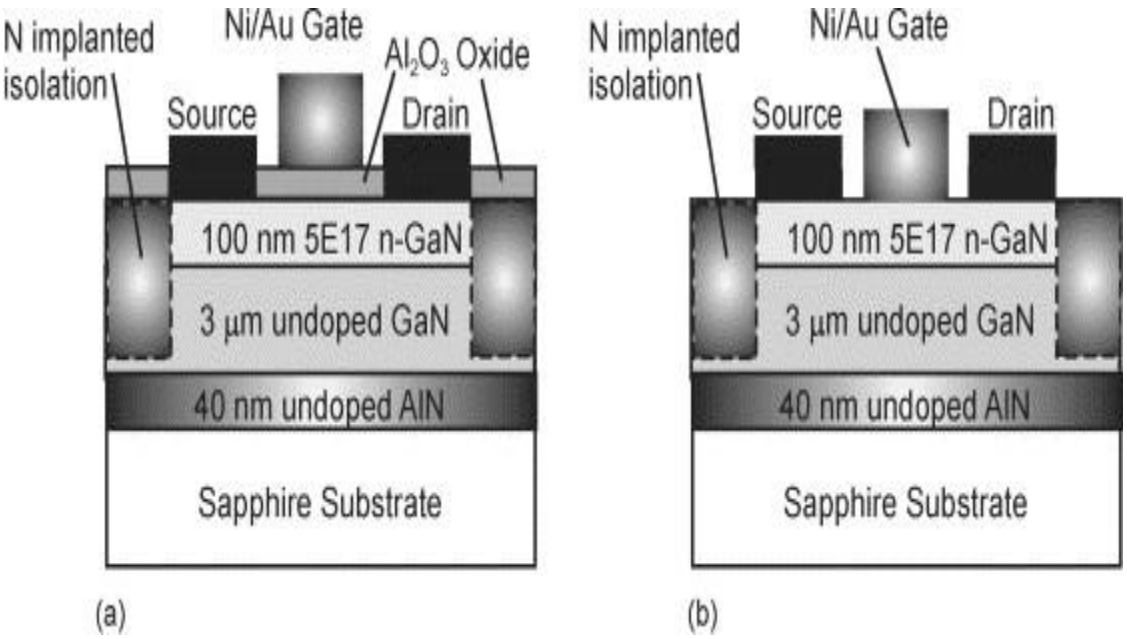


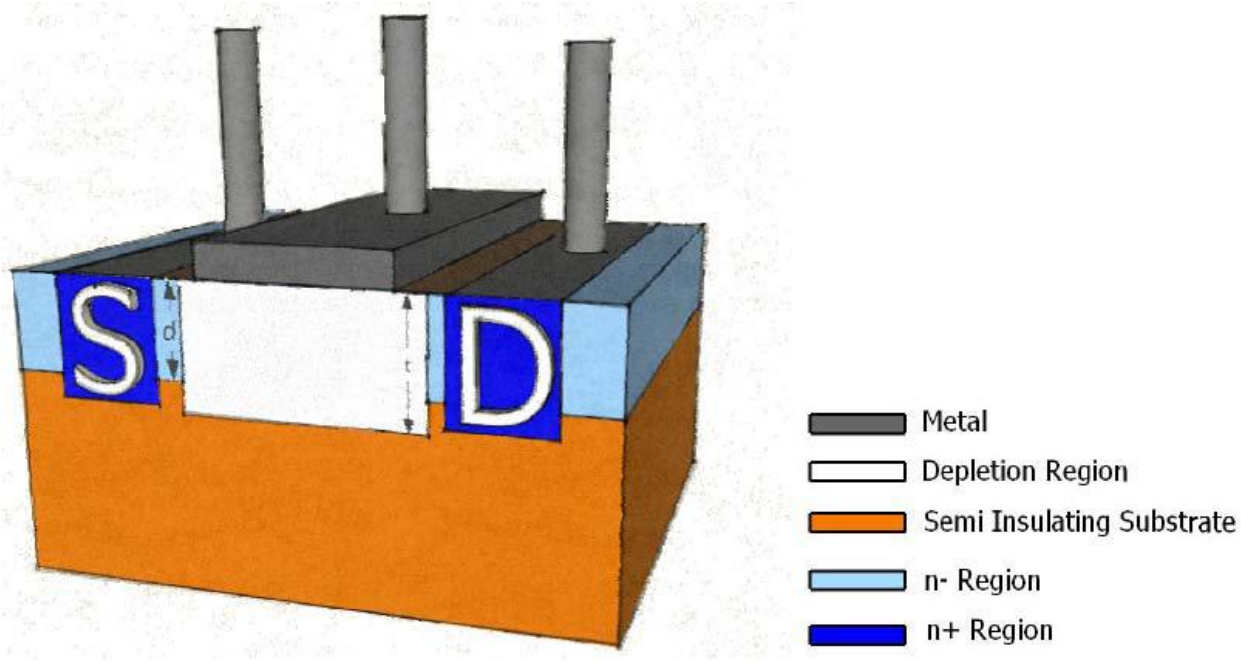
Fig 3.1 GaN mesfet Model

3.1.1 TYPES OF MESFETS

There are two types of MESFETs as explained below:

1) ENHANCEMENT MESFET

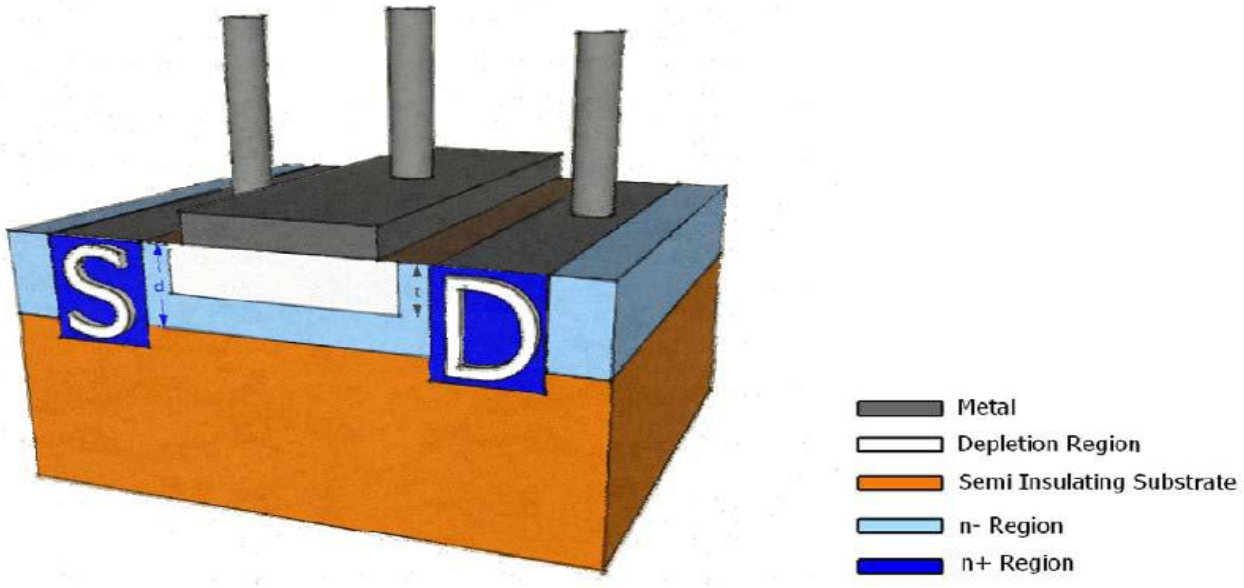
In an n channel MEFET the device remains switched off and the channel region is maturely covered by depletion region completely. This depletion region is narrowed so that the channel region gets expanded. This facilitates the flow of carriers. A junction between the channels is forward bias and gate is made by applying positive voltage to the gate terminal. The device conducts with the increase in channel width allowing the current to flow. [52]



2) DEPLETION MESFET

In an n-channel MESFET the voltage at the gate terminal is altered so that the width of the depletion region can be varied. The flow of carrier is obstructed if a negative voltage is applied at the gate- source. Thus the depletion region expands. A reverse biased junction is formed between gate and channel. At a point when pinch off is achieved i.e. channel gets completely blocked the MESFET behaves like a switch. The resistance between source and the drain is very high at this stage. [53]

Now in case of a vice versa situation if a positive potential is applied at gate source it will turn the MESFET on by minimizing the depletion width.

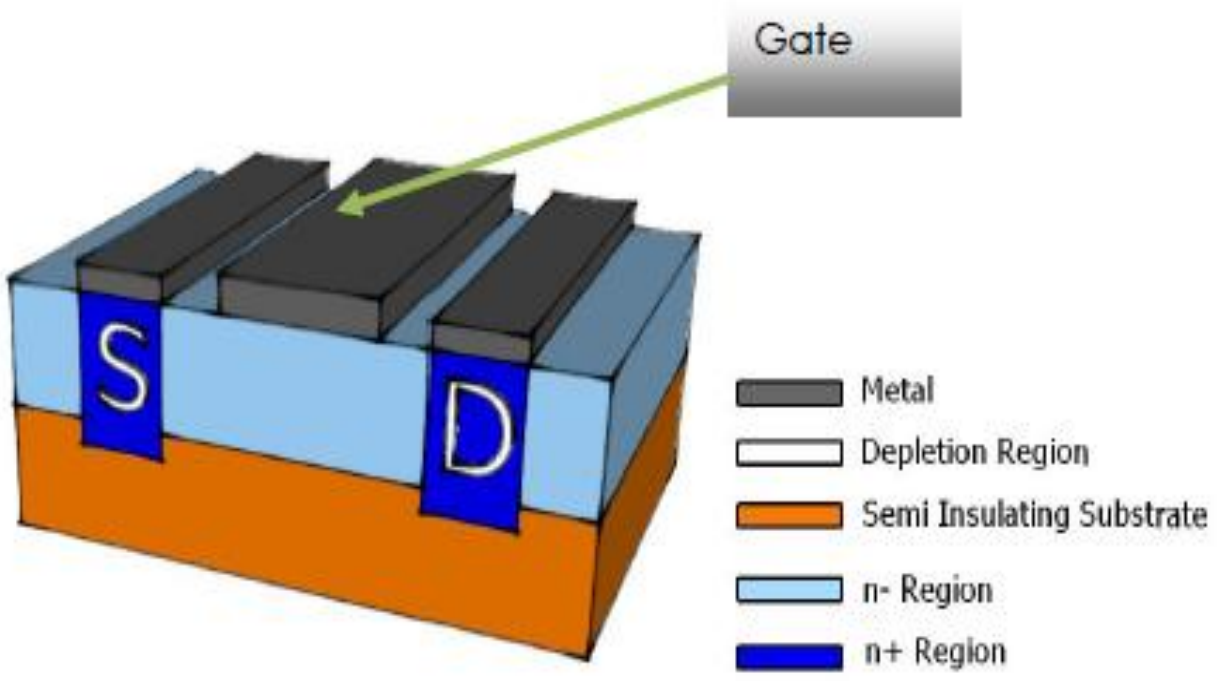


3.1.2 MESFET STRUCTURE

The MESFET has basically two structures as explained below:

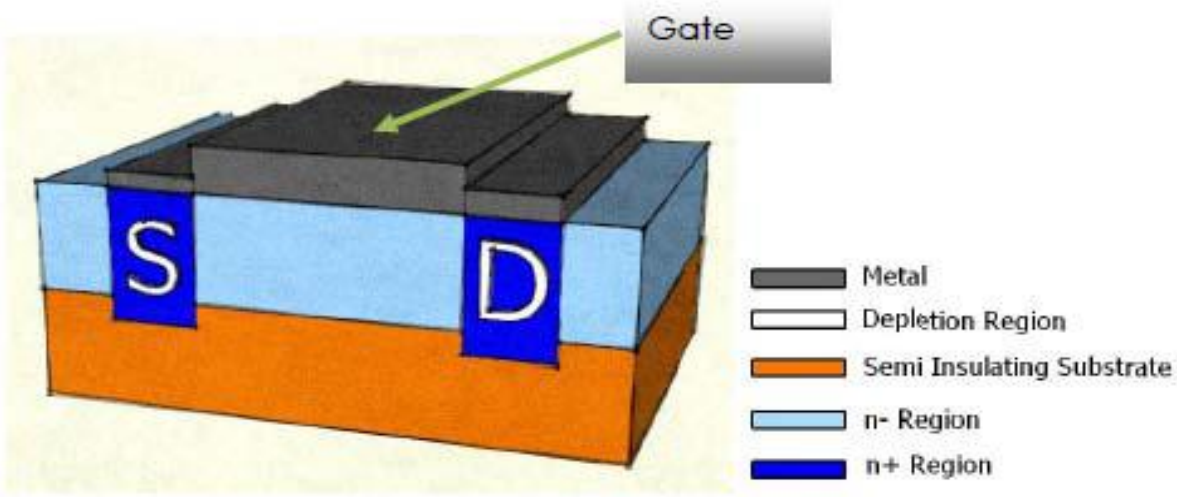
1) SOURCE AND DRAIN (NON SELF ALIGNED)

In this MESFET before the fabrication of gate a source and drain contact is formed. The channel section has a gate on top of it. The channel length is not completely covered by gate. [54]



2) SOURCE AND GATE (SELF ALIGNED)

In this structure the fabrication of gate is done as the first step. An annealing process is used for the fabrication of drain and source using ion implantation. The gate contact is comparatively larger to cover whole length of channel. The gate is capable of withstanding high temperature. [55]



3.2 MESFET Operation

3.2.1 I-V Characteristics of MESFET

There are great similarities in the I-V characteristics of a MOSFET and JFET with a typical MESFET. The current voltage (I-V) characteristics of a typical MESFET are shown in the Figure3.2

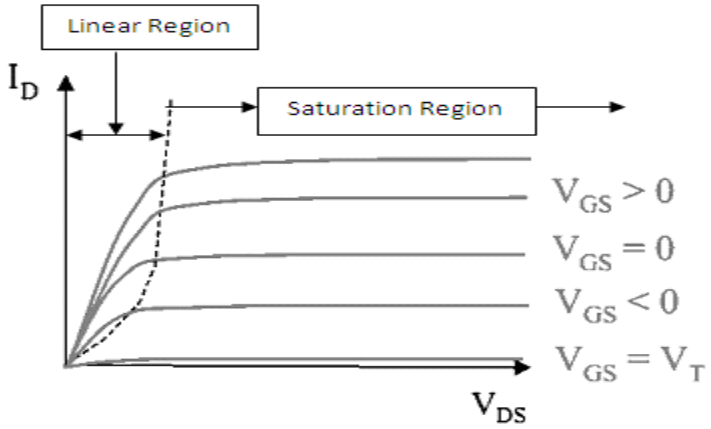


Figure3.2 I-V characteristics of a typical MESFET

In Figure 3.2, drain current (I_{ds}) is plotted against drain-source voltage (V_{ds}). As we know that the drain current is also a function of gate-source voltage (V_{gs}) so an individual curve in the figure represents the dependency of drain current (I_{ds}) in drain-source voltage (V_{ds}) for a particular value of gate-source voltage (V_{gs}). Figure 1.4 represents the I-V characteristics of a depletion type and an enhancement type MESFET. There is another mode of operation of MESFET which is known as the breakdown mode. In this mode excessive drain-source voltage is applied. [56]

To operate the MESFET in depletion mode, necessary voltage should be given at the gate electrode. The application of more negative voltage at the gate electrode makes the junction more reversed biased results in increase of the depletion region. The channel gets entirely depleted, if we keep increasing the negative voltage at gate electrodes. Therefore, no current flows. Here a new term is introduced named threshold voltage. Threshold voltage of a MESFET is the voltage required to fully deplete the doped channel layer. From Figure 3.2, we can see that the value of I_d is very low for lower V_{gs}. Further increase in the negative voltage on the gate will stop the channel. Therefore, we can say that the threshold voltage of the figure above is near the lowest V_{gs}curve. Denoting V_t as the threshold voltage, it can be said that current conducting region are valid for $V_{gs} > V_{t.}$ [57]

3.2.2 REGIONS OF OPERATION OF MESFET

There are different types of regions of operation as explained below:-

1 LINEAR REGION ($V_{dsat} > V_{ds} > 0$)

This region is also known as triode region. In this region the dependency of current and voltage is linear. This region is active when V_{ds} has lower values. The drain current I_d depends linearly on V_{ds} when V_{ds} is low.[58]

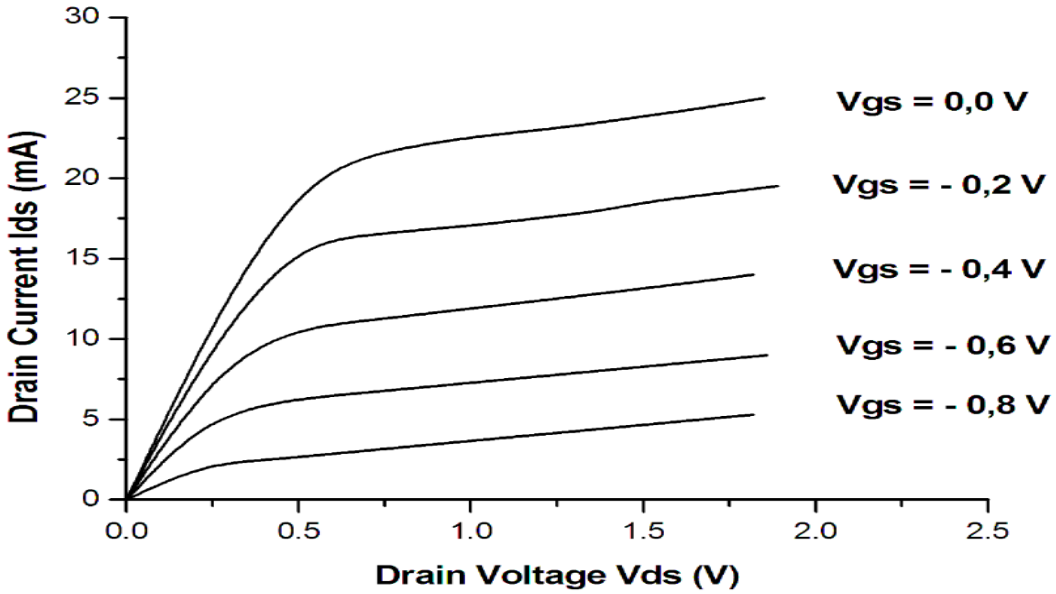


Fig 3.3 Drain current versus Drain voltage depicting active region

2 SATURATION REGION ($V_{dsat} > V_{ds}$)

I_d varies directly with V_{ds} in the linear region but with even further increase in V_{ds} after a certain value there is no significant increase in Id. A saturation current Id is achieved when $V_d = V_{ds}$. The shift in pinch-off point towards drain from source decreases the channel length. This will result in increase of current Id. [59]

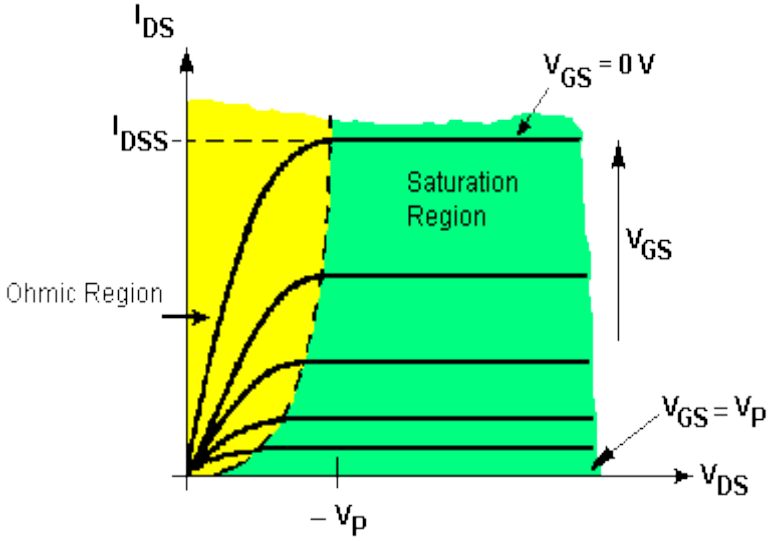


Fig 3.4 Drain current versus Drain voltage depicting saturation region

Depending upon the semiconductor material the saturation can occur in two ways:-

1) SATURATION (VELOCITYSATURATION)

For a semiconductor material like GaAs the drift velocity for a carrier saturate at a lower electric field. When an even higher V_{ds} is applied beyond saturation electric field is high. This results in saturation of carrier velocity in channel. As a result these is saturation in drain current Ids. [60]

2) PINCH OFF SATURATION

In semiconductor materials which have high electric field values the saturation occurs by pinch off. When drift velocity of carriers saturates at a higher value of electric field in channel the depletion on drain side keep increasing with V_{ds}.The result is the depletion region of the drain pinches off the channel. [60]

3.3.3 Fabrication steps in MESFET's

The GaN MESFET creation procedure is abridged in Fig. 3.5 and two silicon implantations are used, one to structure the n-channel area and a second to intensely doped n+ the source anddrain regions in order to form low resistance contacts.A gold-germanium metallization is incorporated to make an ohmic contacts for drain and source. Thicker metal pads are formed along with Schottky gate using aluminum as they are compatible for probing. Metal deposition is done using E-beam evaporation. Device fabrication is done using various processes such as photolithography, resist processing, dielectric deposition and etching, ion implantation, annealing, metal deposition, patterning and alloying. [61]

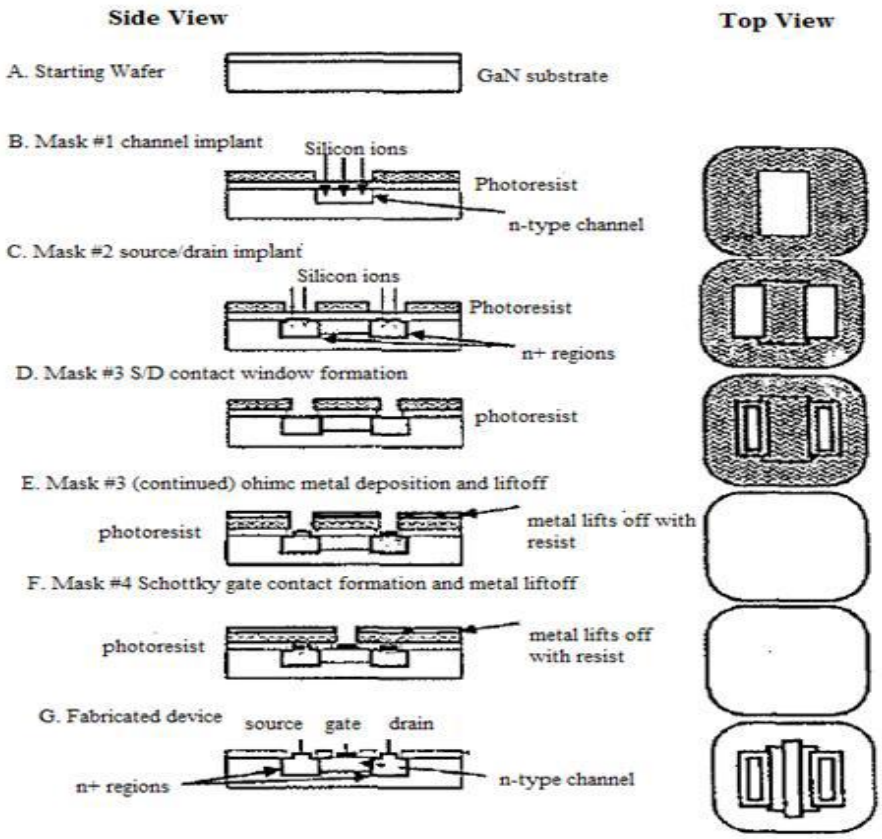


Figure 3.5 Fabrication process

The fabrication process steps are:

- Initial wafer cleaning.
- Silicon nitride cap deposition by reactive sputtering.
- Resist patterning for channel implant using positive resist
- Silicon ion implantation of device channel regions
- Shallow etching of silicon nitride for alignment registration purposes in buffered HF solution and plasma etching.
- Resist stripping and ashing in oxygen plasma.
- Resist patterning for source/drain implant using positive resist.
- Silicon ion implantation of device source and drain regions.
- Resist stripping and ashing in oxygen plasma.
- Annealing of ion implants using rapid thermal annealing

- Resist patterning for ohmic contact formations
- Silicon nitride etching for ohmic contacts
- Deposition of AuGe/Ni metal for ohmic contacts to source and drain using e-beam evaporation and patterning by liftoff technique.
- Ohmic contact alloying by rapid thermal heating.
- Resist patterning for nitride etch for Schottky gate formation
- Silicon nitride etching for Schottky gate formation.
- Aluminum metal deposition for Schottky gate formation using e-beam lift off technique [62].

3.4 APPLICATION OF MESFETS

1 MESFET is potentially used in high frequency low noise RF amplifiers, microwave power amplifiers and oscillators. This is basically due to is high electron mobility and limited stray capacitances.

2 BLUE Ray disk technologies: For high density optical storage systems GaN is used. It is also used in fabrication of blue LASER diodes.

3 MESFETS have a potential application in telecommunication and aerospace industry. The high frequency applications such as RADAR, satellite systems, cellular application's make MESFET a very potential electronic component.

4 The automotive industry makes use of MESFETS for high power electronic applications. Nano-electronics make use of nano tubes fabricated from GaN. [63]

CHAPTER 4

Theory and Calculation of a GaN MESFET

A schematic cross-section of a GaN MESFET is illustrated in Fig.4.1.An offset gate structure in the device has-been considered in order to improve high power performance as described in the results and discussions section. Considering impurity diffusion due to annealing, the impurity distribution can be represented by a symmetric Gaussian distribution as follows. [64]

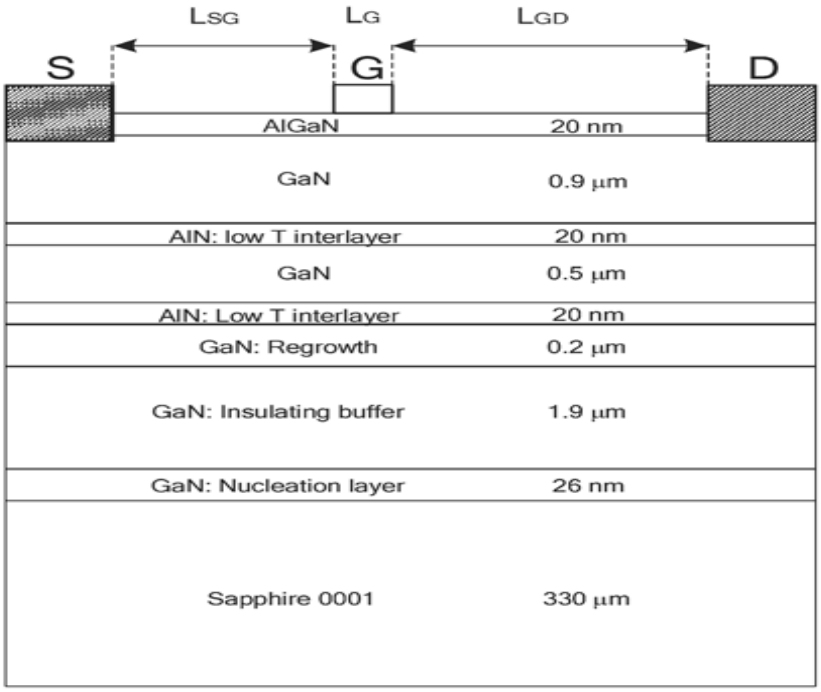


Fig 4.1 Schematic diagram of GaN MESFET

4.1 I-V Characteristics of a MESFET

The drain-source current in the linear region including the parasitic source and drain resistances is evaluated as given below:-

$$\int_0^L I_{ds}\,dx = qZ\int_{I_{ds}\,Rs}^{V_{ds}-I_{ds}\,Rd} N_d\,(a-h)dV$$

Equation 4.1a

$$I_{ds} = \frac{qZ\square aN_d}{L}(V_{ds} - I_{ds}(R_s + R_d) - \frac{2}{3V_p^{\frac{1}{2}}}[(V_{bi} - V_{gs} + V_{ds} - I_{ds}R_d)^{\frac{3}{2}} - (V_{bi} - V_{gs} + I_{ds}R_d)^{3/2}$$

Where:-

I_{ds}= drain-source current

μ =electron mobility

L= gate length

A= active channel thickness

V_p= pinch-off voltage

Rs= parasitic source

Z = gate width

R_d= drain resistances

V_{ds}= applied drain-source voltage [65, 66, 67]

4.2 C-V Characteristic of GaN MESFET

It is very important to have an accurate model of capacitance for the simulation of high speed analogue and digital circuits.

4.2.1 Gate Source Capacitance

The simplified charge distributions are used to calculate internal device capacitances. For microwave applications the internal gate-source capacitance C_{gs} plays a significant impact on frequency performance and input impedance.[68]

Simplified charge distributions under the gate are used to calculate the internal device capacitance. Mathematically it can be written as:-

Eqn 1:-

$$C_{gs} = \frac{\partial Q_1}{\partial V_S} + \frac{\partial Q_2}{\partial V_S} + \frac{\partial Q_3}{\partial V_S}$$

Where

V_{gd}=gate-drain potential

Q_1, Q_2, Q_3=Internal Charge distribution

$$Q_1 = \frac{ZqN_d a^2}{2}\left(\left(\frac{V_{bi} - V_g + V_s}{V_p}\right)^{1/2} + \left(\frac{V_{bi} - V_g + V_d}{V_p}\right)^{1/2}\right)$$

$$Q_2 = \frac{\text{III}qN_d a^2}{4}\left(\left(\frac{V_{bi} - V_g + V_s}{V_p}\right)\right)$$

$$Q_3 = \frac{\text{III}qN_d a^2}{4}\left(\left(\frac{V_{bi} - V_g + V_d}{V_p}\right)\right)$$

V_s=Source Potential

V_g=Gate Potential

V_d =Drain Potential

Substituting the above equations in 1 we obtain gate source capacitance:-

Equation 4.2.1a

$$C_{gs} = \frac{ZL}{2\sqrt{2}}\left(\frac{q\mathcal{E}_s N_d}{V_{bi} - V_{gs}}\right)^{1/2} + \frac{\text{III}}{2}\mathcal{E}_s Z$$

Where,

C_{gs} =gate source capacitance

N_d =doping density in channel

V_{bi}=built in potential

V_{gs}=gate source voltage

q=electron charge

L=gate length

4.2.2 Gate Drain Capacitance

Similarly we obtain internal gate-drain capacitance:-[69]

Equation 4.2.1b

$$C_{gd} = \frac{ZL}{2\sqrt{2}}\left(\frac{q\mathcal{E}_s N_d}{V_{bi} - V_{gd}}\right)^{1/2} + \frac{\mathbb{III}}{2}\mathcal{E}_s Z$$

Where,

C_{gd}=gate drain capacitance

N_d=doping density in channel

V_{bi}=built in potential

V_{gs}=gate source voltage

q=electron charge

L=gate length

4.3 Transconductance of a MESFET

The device quality for microwave applications is mainly determined by its transconductance (g_m).The channel material and device dimensions significantly affect the tansconductance. Basically g_m is the slope of I_{ds}-V_{gs} with V_{ds} constant. [70]

Equation 4.3a

$$g_m' = \frac{g_m}{1 + g_m R_s}$$

Where

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$$

Chapter 5

Result and Discussion

5.1 Synthesis of I-V Characteristics of GaN MESFET

This research work has been conducted by the physics based analytical model. So far, many analytical model has been developed to evaluate the I-V characteristics, where the model for I-V characteristics cannot combine the non-saturation and saturation region (linearity and non-linearity regime). The present work shows an tremendous impact of numerical iterative to find the I-V characteristics of GaN MESFET in linear and non-linear regions.

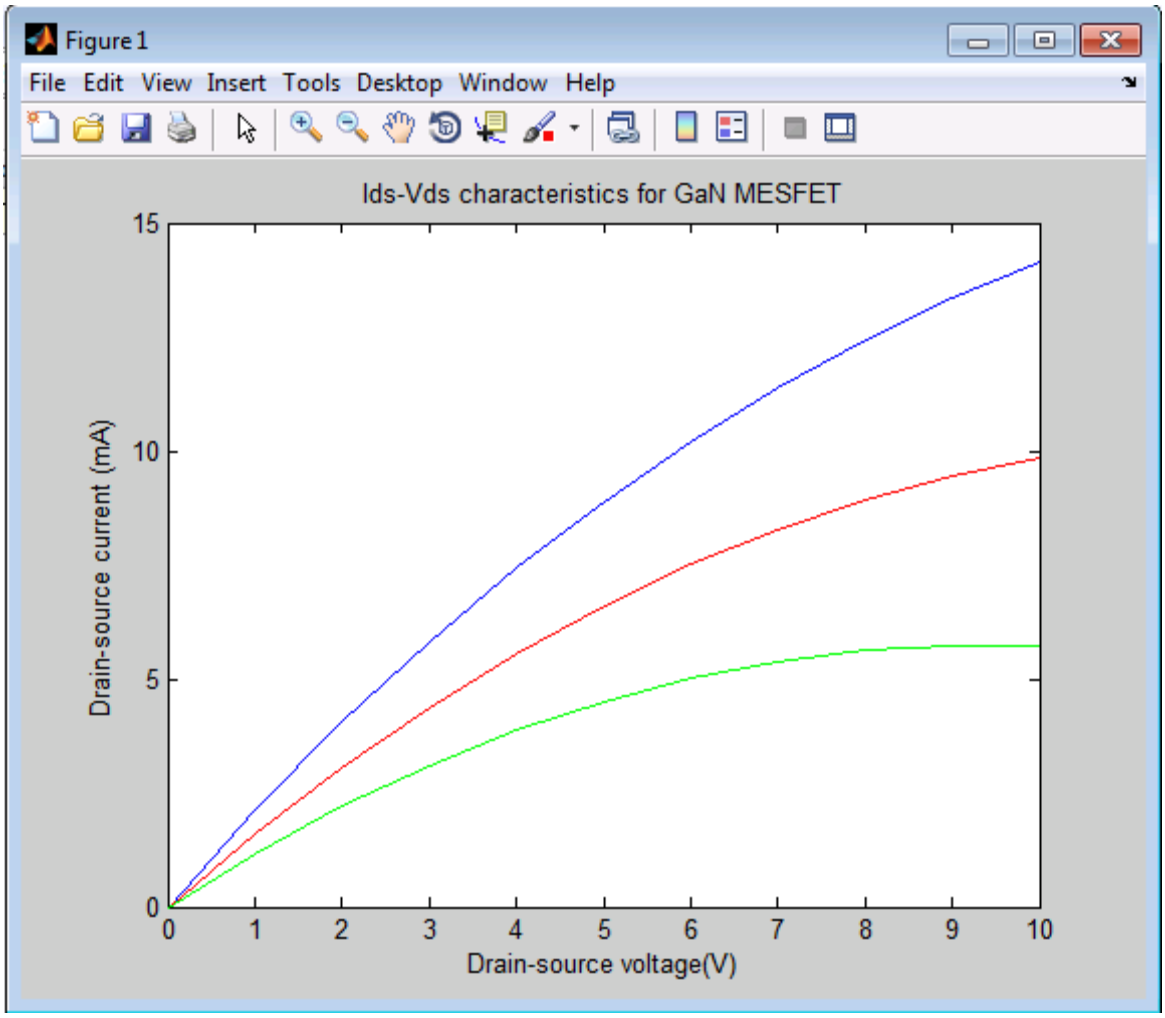


Figure 5.1 Drain-source current versus drain-source voltage for different gate-source voltages.

The figure 5.2 present a plot of drain-source current (I_{DS}) versus drain-source voltage (V_{ds}) for different gate-source voltage (V_{gs}) of 0V, -3V and -6V with channel doping concentration (Nd) of 10^{17} cm^{-3} and substrate concentration (Na) of 10^{17} cm^{-3}. The I-V characteristics for gate-source voltage (V_{gs}) of 0V shows a linearity properties and non-linearity (saturation region) may be observed beyond drain-source voltage (V_{ds}) more than 10V. The drain current at gate-source voltage (V_{gs}) = -3V shows linearity from drain-source voltage V_{ds} = 0V to V_{ds} =7V and the current starts saturation from V_{ds}= 7V and onwards. Further, the drain with v_{gs} = -3V clearly indicates the linearity and non-linearity properties. The linearity of drain current shows from vds = 6V and non-linearity properties is observed from Vds = 6V and onwards. This iterative method can present the linearity and non-linearity properties of I-V characteristics till up to the breakdown point. This plot has been generated by using the Equation 4.1a

5.2 Synthesis of Transconductance Characteristics of GaN MESFET

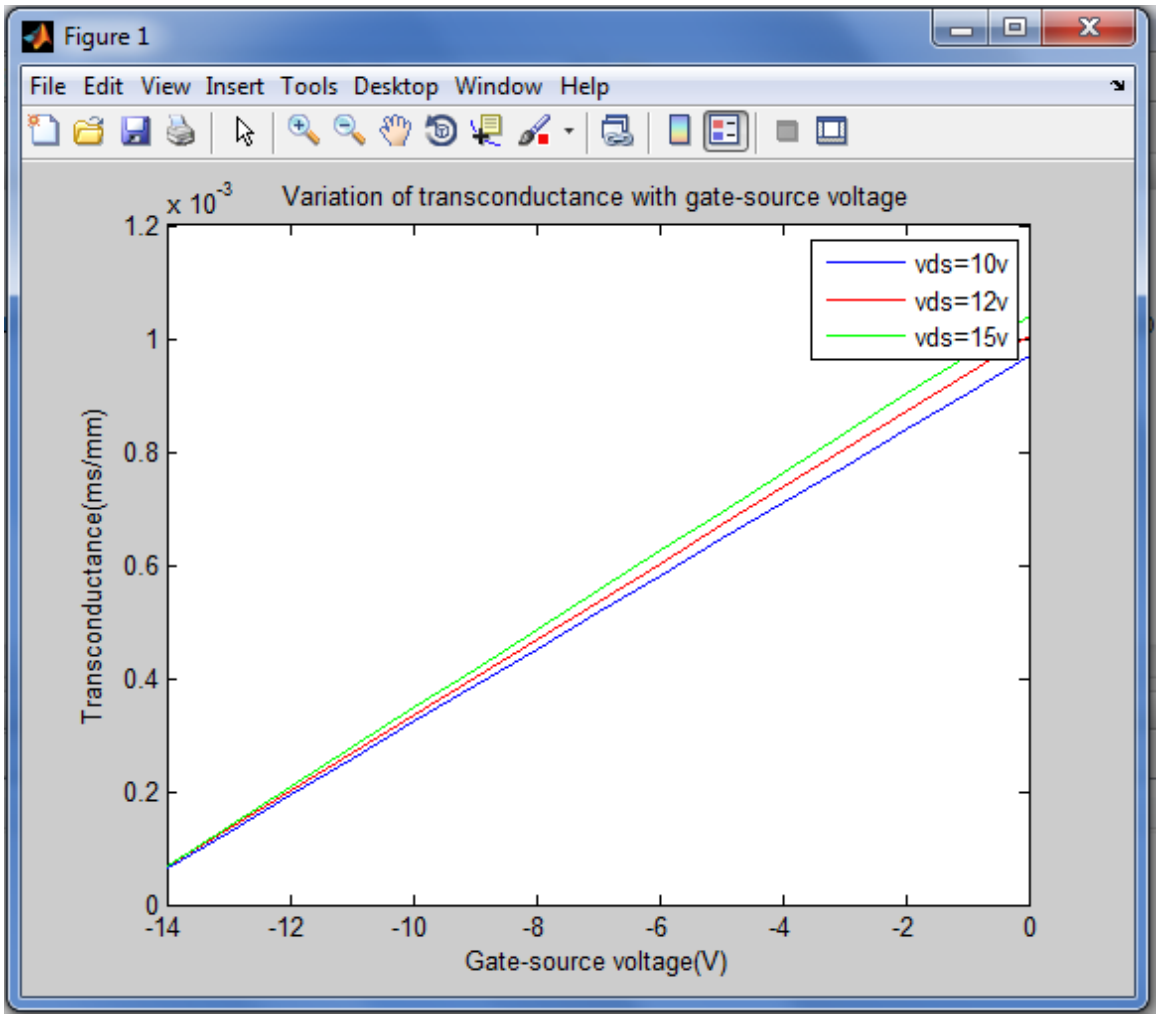


Figure 5.2 Transconductance (g_m) versus gate-source voltage (V_{gs}) for different drain-source voltage V_{ds}

The figure 5.2 shows the plot of transconductance (g_m) versus gate-source voltage (V_{gs}) for different drain-source voltage V_{ds} = 5V, 10V and 15V. The transconductance gm linearly increases with the increment of gate-source voltage V_{gs} from 0V to -9V. The transconductance shows a higher value at high drain-source voltage V_{ds} = 15V compared to other drain-source voltage V_{ds} for 5V and 10V, because the GaN MESFET enters into the saturation regime. The transconductance at lower V_{ds} for 5V and 10V shows small value due the linearity and the transition between non-saturation and saturation. From the

intersection of gate voltage axis, the threshold voltage is found to be approximately in the range of -9V to 9.5V. The plot has formed by using the Equation 4.3a.

5.3 Synthesis of C-V Characteristics of GaN MESFET

5.3.1 Variation of Gate Source Capacitance with Drain Source Voltage

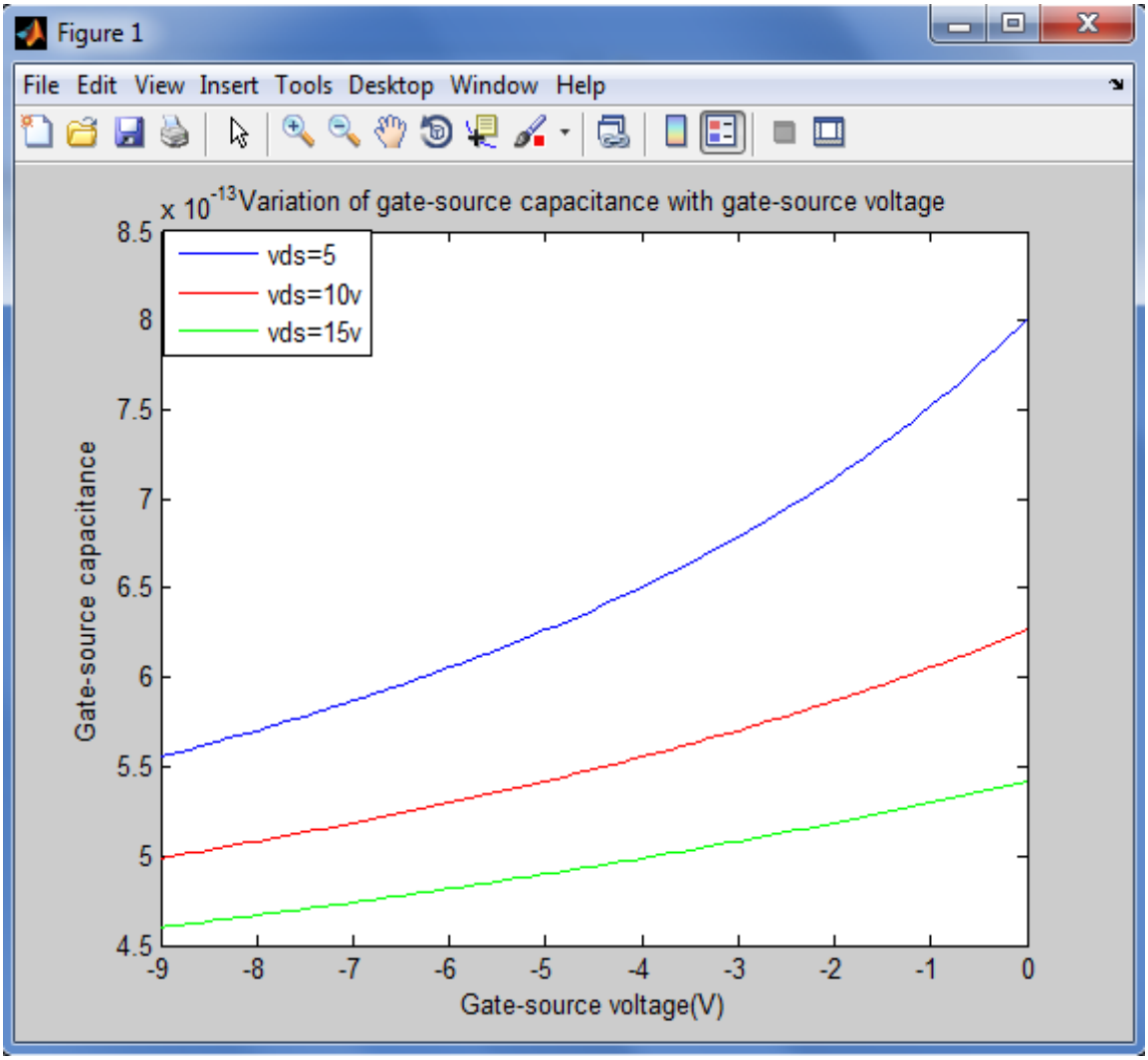


Figure 5.3 Gate-source capacitance (C_{gs}) versus gate-source voltage (V_{gs}) for different drain-source voltage (V_{ds})

The figure 5.3 exhibits a plot of gate-source capacitance C_{gs} versus gate-source voltage V_{gs} for different drain-source voltage V_{ds}. The gate-source capacitance exponentially

increases with the increment of gate-source voltage from -9V to 0V. The gate capacitance is comparatively higher for the drain-source voltage V_{ds} = 5 and the nature curves of other V_{ds} = 10V and 15V are similar to the C_{gs} curve for V_{ds} = 5V. As the gate-source voltage becomes more positive, the charge in the gate depletion layer increases, which –in turn increase the gate-source capacitance. The plot has been developed by computing the equation 4.2.1a.

5.3.1 Variation of Gate Source Capacitance with Drain Source Voltage

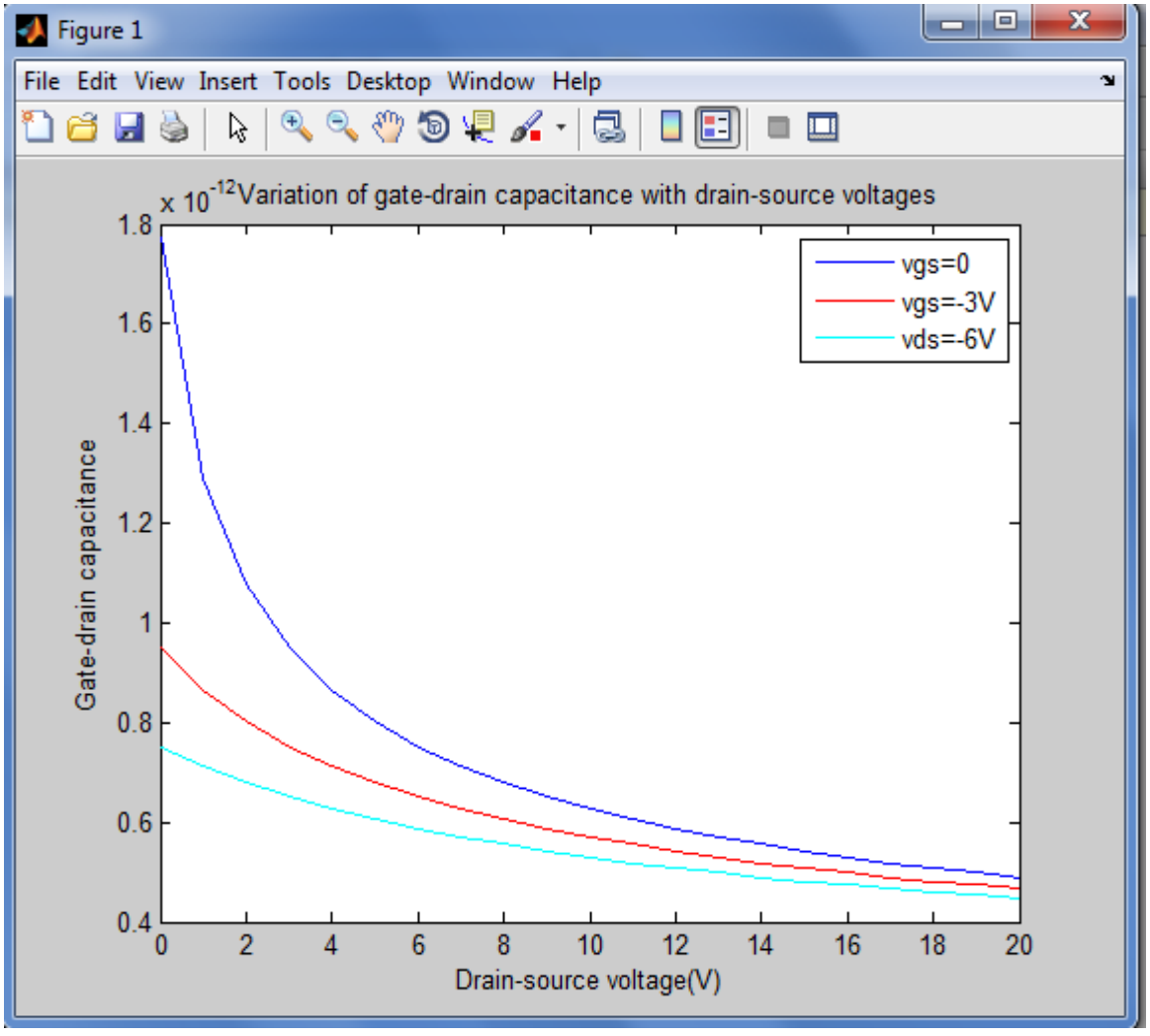


Figure 5.4 gate-drain capacitance C_{gd} versus drain-source voltage V_{ds}

Figure 5.4 gate-drain capacitance C_{gd} versus drain-source voltage V_{ds} for different gate-source voltage V_{gs} of 0V, -3V and -6V. The plot presents the exponential increment of

gate-drain capacitance $C_{gd}$with increase of drain-source voltage. The maximum gate-drain capacitance is obtained for V_{gs} = 0V due to large charge confined in the gate depletion region. The gate drain capacitance for V_{gs} = 0V, -3V and -6V becomes saturated at higher drain voltage in the range of V_{ds} = 16 to 20V. This plot has been drawn using the Equation 4.2.1b

CHAPTER 6
CONCLUSIONS

In this thesis, I have attempted to demonstrate the effects of parasitic resistances on GaN MESFET parameters such as the transconductance, total internal capacitance. The drain-source current in the linear region including the parasitic source and drain resistances is demonstrated and it shows both linearity and non-linearity. The gate source voltage, V_{gs} is varied in order to demonstrate the I-V characteristics of MESFET.

The variation of transconductance with gate-source voltage shows there is a linear increase in the transconductance with increase in gate-source voltage, and for a fixed drain-source voltage the MESFET with lowest parasitic resistance gives the highest transconductance.

The variation of gate source capacitance with gate source voltage shows there is an exponential increase in gate source capacitance given drain source voltage is constant. The variation of gate drain capacitance with drain source voltage shows there is an exponential decrease in gate drain capacitance given gate source voltage is constant. These results have been formulated considering the effect of parasitic resistances.

The parameters have shown the desired trends with variation and can be said to have good agreement with the expected results.

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Appendix A

C_{gs}=gate source capacitance

C_{gd}=gate drain capacitance

N_d=doping density in channel

V_{bi}=built in potential

V_{gs}=gate source voltage

q=electron charge

L=gate length

I_{ds}= drain-source current

μ =electron mobility

L= gate length

V_p= pinch-off voltage

A= active channel thickness

Rs= parasitic source

Z = gate width

R_d= drain resistances

V_{ds}= applied drain-source voltage

Appendix B

Matlab Code

Variation of Drain-Source Current with Drain-Source Voltage

```
clc;
clear all;
close all;
%variable
u = 0.15;
eps = 9.5*8.8542e-14;
max_iter= 100;
tol =.000000001;
a = 7.5*(10^-6);
d = 0.15e-4;
Vp = 16;
%fixed
q = 1.6*(10^-19);
Z = 100*(10^-4);
Nd = 1*(10^17);
L = 4*(10^-4);
Rs = 75;
Rd = 75;
Vbi = 1;
Vgs = 0;
%Vds = 5;
Vds = [0:1:10];
Ids(1) = 0;
for i=1:length(Vds)
```

```
for k = 1:max_iter
Ids (k+1)= ((q*Z*u*Nd*a)/L)*(Vds(i)-Ids(k)*(Rs+Rd)-(2/(3*sqrt(Vp)))*((Vbi-
Vgs+Vds(i)-Ids(k)*Rd)^(3/2) -
(Vbi-Vgs+Ids(k)*Rs)^(3/2) ));
err = abs((Ids(k+1)-Ids(k))/Ids(k+1));
if(err<tol)
sol(i) = Ids(k+1);
break;
end
end
sol(i) = (Ids(k+1))*1000;
end
plot (Vds, sol),ylabel('Drain-source current (mA)'), xlabel('Drain-source voltage(V)'),
title('Ids-Vds characteristics
for GaN MESFET')
hold on;
Vgs = -3;
Vds = [0:1:10];
Ids(1) = 0;
for i=1:length(Vds)
for k = 1:max_iter
Ids(k+1) = ((q*Z*u*Nd*a)/L)*(Vds(i)-Ids(k)*(Rs+Rd)-(2/(3*(sqrt(Vp))))*((Vbi-
Vgs+Vds(i)-(Ids(k)*Rd))^(3/2)-
(Vbi-Vgs+( Ids(k)*Rs))^(3/2)));
err = abs((Ids(k+1)-Ids(k))/Ids(k+1));
if(err<tol)
sol(i) = Ids(k+1);
break;
end
end
sol(i) = (Ids(k+1))*1000;
```

```
end
plot (Vds, sol, 'r')
hold on;
Vgs = -6;
%Vds = 5;
Vds = [0:1:10];
Ids(1) = 0;
for i=1:length(Vds)
for k = 1:max_iter
Ids(k+1) = ((q*Z*u*Nd*a)/L)*(Vds(i)-Ids(k)*(Rs+Rd)-(2/(3*(sqrt(Vp))))*((Vbi-
Vgs+Vds(i)-(Ids(k)*Rd))^(3/2)-
(Vbi-Vgs+( Ids(k)*Rs))^(3/2)));
err = abs((Ids(k+1)-Ids(k))/Ids(k+1));
if(err<tol)
sol(i) = Ids(k+1);
break;
end
end
sol(i) = (Ids(k+1))*1000;
end
plot (Vds, sol, 'g')
hold on;
Vgs = -9;
%Vds = 5;
Vds = [0:1:10];
Ids(1) = 0;
for i=1:length(Vds)
for k = 1:max_iter
Ids(k+1) = ((q*Z*u*Nd*a)/L)*(Vds(i)-Ids(k)*(Rs+Rd)-(2/(3*(sqrt(Vp))))*((Vbi-
Vgs+Vds(i)-(Ids(k)*Rd))^(3/2)-
(Vbi-Vgs+( Ids(k)*Rs))^(3/2)));
```

```
err = abs((Ids(k+1)-Ids(k))/Ids(k+1));
if(err<tol)
sol(i) = Ids(k+1);
break;
end
end
sol(i) = (Ids(k+1))*1000;
end
plot (Vds, sol, 'c')
hold on;
```

Variation of Gate-Drain Capacitance with Drain-Source Voltage

```
clear all;
clc;
close all;
Z = 100*10^-4;
L = 4*10^-4;
q = 1.6*10^-19;
Eo = 8.85*10^-14;
E = 9.5*Eo;
Nd = 10^17;
Vbi = 1;
Vds = [0:1:20];
Vgs = 0;
Cgd = (((Z*L)./(2*2^0.5)).*sqrt((q*E*Nd)./(Vbi-(Vgs-Vds))) + (pi./2)*E*Z)*10;
plot(Vds,Cgd), xlabel('Drain-source voltage(V)'),ylabel('Gate-drain
capacitance'),title('Variation of gate-drain capacitance with drain-source voltages')
hold on;
Vgs = -3;
Cgd = (((Z*L)./(2*2^0.5)).*sqrt((q*E*Nd)./(Vbi-(Vgs-Vds))) + (pi./2)*E*Z)*10;
plot(Vds,Cgd,'r')
hold on;
Vgs = -6;
Cgd = (((Z*L)./(2*2^0.5)).*sqrt((q*E*Nd)./(Vbi-(Vgs-Vds))) + (pi./2)*E*Z)*10;
plot(Vds,Cgd,'c')
hleg1=legend('vds=0','vds=-3v','vds=-6v');
```

Variation of Gate-Source Capacitance with respect to Gate-Source Voltage

```
clear all;
clc;
close all;
Z = 100*10^-4;
L = 4*10^-4;
q = 1.6*10^-19;
Eo = 8.85*10^-14;
E = 9.5*Eo;
Nd = 10^17;
Vbi = 1;
Vgs = [-9:0.1:0];
Vds=5;
Cgs = (((Z*L)./(2*2^0.5)).*sqrt((q*E*Nd)./(Vbi-Vgs+Vds)) + (pi./2)*E*Z)*10;
plot(Vgs,Cgs), xlabel('Gate-source voltage(V)'),ylabel('Gate-source
capacitance'),title('Variation of gate-source capacitance with gate-source voltage')
hold on;
Vds=10;
Cgs = (((Z*L)./(2*2^0.5)).*sqrt((q*E*Nd)./(Vbi-Vgs+Vds)) + (pi./2)*E*Z)*10;
plot(Vgs,Cgs), xlabel('Gate-source voltage(V)'),ylabel('Gate-source
capacitance'),title('Variation of gate-source capacitance with gate-source voltage')
hold on;
Vds=15 ;
Cgs = (((Z*L)./(2*2^0.5)).*sqrt((q*E*Nd)./(Vbi-Vgs+Vds)) + (pi./2)*E*Z)*10;
plot(Vgs,Cgs), xlabel('Gate-source voltage(V)'),ylabel('Gate-source
capacitance'),title('Variation of gate-source capacitance with gate-source voltage')
hold on;
hleg1=legend('vds=5','vds=10v','vds=15v');
```

Variation of Transconductance with Gate-Source Voltage

```
clc;
close all;
clear all;
a = 7.5*(10^-6);
Kd = 0.6;
Vsat = 0.27*10^4;
u = 0.15;
Es = Vsat/u;
L = 4*(10^-4);
Vbi = 1;
Vp = 16;
Vt = Vbi-Vp;
eps = 9.5*8.8542*10^-14;
Rs = 75;
Z = 100*(10^-4);
Vds = 10;
gm = zeros(1,15);
syms Vgs
gyb=diff((((1+2*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-
((Es*L*(Vgs-Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs*(Vgs-Vt)-
sqrt(1+4*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs*(Vgs-
Vt)))/(2*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs^2))*(1+((L-((2*a)/pi)*asinh((pi*Kd*(Vds-
((Es*L*(Vgs-Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es)))+(((1-Kd)*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(Es*cosh((pi*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))/(2*a)))))/L)));
```

```
gy = gyb/(1+gyb*Rs)
gm(1)=(subs(gy,Vgs,-14))*1000/(Z*10^3);
gm(2)=(subs(gy,Vgs,-13))*1000/(Z*10^3);
gm(3)=(subs(gy,Vgs,-12))*1000/(Z*10^3);
gm(4)=(subs(gy,Vgs,-11))*1000/(Z*10^3);
gm(5)=(subs(gy,Vgs,-10))*1000/(Z*10^3);
gm(6)=(subs(gy,Vgs,-9))*1000/(Z*10^3);
gm(7)=(subs(gy,Vgs,-8))*1000/(Z*10^3);
gm(8)=(subs(gy,Vgs,-7))*1000/(Z*10^3);
gm(9)=(subs(gy,Vgs,-6))*1000/(Z*10^3);
gm(10)=(subs(gy,Vgs,-5))*1000/(Z*10^3);
gm(11)=(subs(gy,Vgs,-4))*1000/(Z*10^3);
gm(12)=(subs(gy,Vgs,-3))*1000/(Z*10^3);
gm(13)=(subs(gy,Vgs,-2))*1000/(Z*10^3);
gm(14)=(subs(gy,Vgs,-1))*1000/(Z*10^3);
gm(15)=(subs(gy,Vgs,0))*1000/(Z*10^3);
Vgs = [-14:1:0];
plot(Vgs,gm),xlabel('Gate-source
voltage(V)'),ylabel('Transconductance(ms/mm)'),title('Variation of transconductance with
gate-source voltage')
hold on;
Vsat = 0.28*10^4;
Vds = 12;
gm = zeros(1,15);
syms Vgs
gyb=diff((((1+2*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-
((Es*L*(Vgs-Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs*(Vgs-Vt)-
sqrt(1+4*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs*(Vgs-
Vt)))/(2*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs^2))*(1+((L-((2*a)/pi)*asinh((pi*Kd*(Vds-
```

```
((Es*L*(Vgs-Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es)))+(((1-Kd)*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(Es*cosh((pi*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))/(2*a)))))/L)));
gy = gyb/(1+gyb*Rs);
gm(1)=(subs(gy,Vgs,-14))*1000/(Z*10^3);
gm(2)=(subs(gy,Vgs,-13))*1000/(Z*10^3);
gm(3)=(subs(gy,Vgs,-12))*1000/(Z*10^3);
gm(4)=(subs(gy,Vgs,-11))*1000/(Z*10^3);
gm(5)=(subs(gy,Vgs,-10))*1000/(Z*10^3);
gm(6)=(subs(gy,Vgs,-9))*1000/(Z*10^3);
gm(7)=(subs(gy,Vgs,-8))*1000/(Z*10^3);
gm(8)=(subs(gy,Vgs,-7))*1000/(Z*10^3);
gm(9)=(subs(gy,Vgs,-6))*1000/(Z*10^3);
gm(10)=(subs(gy,Vgs,-5))*1000/(Z*10^3);
gm(11)=(subs(gy,Vgs,-4))*1000/(Z*10^3);
gm(12)=(subs(gy,Vgs,-3))*1000/(Z*10^3);
gm(13)=(subs(gy,Vgs,-2))*1000/(Z*10^3);
gm(14)=(subs(gy,Vgs,-1))*1000/(Z*10^3);
gm(15)=(subs(gy,Vgs,0))*1000/(Z*10^3);
Vgs = [-14:1:0];
plot(Vgs,gm,'r')
hold on;
Vsat = 0.29*10^4;
Vds = 15;
gm = zeros(1,15);
syms Vgs
gyb=diff((((1+2*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-
((Es*L*(Vgs-Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs*(Vgs-Vt)-
sqrt(1+4*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs*(Vgs-
Vt)))/(2*((2*eps*Vsat*Z)/(a*(Vp+3*Es*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
```

```
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))) )*Rs^2))*(1+((L-((2*a)/pi)*asinh((pi*Kd*(Vds-
((Es*L*(Vgs-Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es)))+(((1-Kd)*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(Es*cosh((pi*(L-((2*a)/pi)*asinh((pi*Kd*(Vds-((Es*L*(Vgs-
Vt))/(Es*L+(Vgs-Vt)))))/(2*a*Es))))/(2*a)))))/L)));
gy = gyb/(1+gyb*Rs);
gm(1)=(subs(gy,Vgs,-14))*1000/(Z*10^3);
gm(2)=(subs(gy,Vgs,-13))*1000/(Z*10^3);
gm(3)=(subs(gy,Vgs,-12))*1000/(Z*10^3);
gm(4)=(subs(gy,Vgs,-11))*1000/(Z*10^3);
gm(5)=(subs(gy,Vgs,-10))*1000/(Z*10^3);
gm(6)=(subs(gy,Vgs,-9))*1000/(Z*10^3);
gm(7)=(subs(gy,Vgs,-8))*1000/(Z*10^3);
gm(8)=(subs(gy,Vgs,-7))*1000/(Z*10^3);
gm(9)=(subs(gy,Vgs,-6))*1000/(Z*10^3);
gm(10)=(subs(gy,Vgs,-5))*1000/(Z*10^3);
gm(11)=(subs(gy,Vgs,-4))*1000/(Z*10^3);
gm(12)=(subs(gy,Vgs,-3))*1000/(Z*10^3);
gm(13)=(subs(gy,Vgs,-2))*1000/(Z*10^3);
gm(14)=(subs(gy,Vgs,-1))*1000/(Z*10^3);
gm(15)=(subs(gy,Vgs,0))*1000/(Z*10^3);
Vgs = [-14:1:0];
plot(Vgs,gm,'g')
hleg1=legend('vds=10','vds=12v','vds=15v');
```