CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

ANALYTICAL MODEL OF GALLIUM NITRIDE MESFET’S

A graduate project submitted in partial fulfillment of the requirements

For the degree of Masters of Science in

Electrical Engineering

By

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ABSTRACT

ANALYTICAL MODEL OF GALLIUM NITRIDE MESFET’S

By

Uttam Raj Sali

Master of Science in Electrical Engineering

This project presents an analytical model of Gallium Nitride (GaN) MESFETs (metal-semiconductor field effect transistors). There are two band structures modeled for GaN: a Zinc Blende crystal structure and a Wurtzite crystal structure. This model is based on the parameters chosen for the Wurtzite crystal structure. The channel conductance, saturation current, transconductance, charge under the gate, drain-to-gate and gate-to-source capacitance, cutoff frequency, characteristic switching time, power-delay product, and breakdown voltage are calculated in the analysis of this model. These results are verified by two-dimensional computer calculations that agree with the results of the computer analysis and experimental data for a 1-µm gate GaN MESFET. A stray gate-to-drain and gate-to-source capacitance defined a limitation on the gate length as greater than 0.1 µm for a GaN MESFET.

In this project, computer analysis is compared with experimental data for GaN. A MATLAB tool is used to obtain the computer analysis. The simulation shows computer analysis for GaN in agreement with the experimental data for a GaN MESFET.
Chapter 1 Introduction

1.1 GaN MESFET

Silicon has been a popular material for power management since the 19th century. The advantages of silicon over earlier available semiconductors such as selenium or germanium are reliability, ease of use, and low cost. Future semiconductors wishing to replace silicon in power transistors will obviously need to supersede silicon in those categories. The following table shows a few electrical properties of three major semiconductor materials (Gallium Nitride [GaN], Silicon [Si], and Silicon Carbide [SiC]) in the power management market.

Table 1.1: Material Properties of GaN, Si, and SiC [1]

<table>
<thead>
<tr>
<th>Properties</th>
<th>Description</th>
<th>GaN</th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g (\text{ev})$</td>
<td>Bandgap energy</td>
<td>3.4</td>
<td>1.12</td>
<td>3.2</td>
</tr>
<tr>
<td>$E_{BR} (\text{MV/cm})$</td>
<td>Crystal electric field for break down in crystal</td>
<td>3.3</td>
<td>0.3</td>
<td>3.5</td>
</tr>
<tr>
<td>$\mu (\text{cm}^2/\text{Vs})$</td>
<td>Mobility of electrons</td>
<td>990–2000</td>
<td>1500</td>
<td>650</td>
</tr>
</tbody>
</table>

Translating these basic crystal parameters to compare device performance in a power transistor is to calculate the best theoretical performance that could be achieved from these three candidates. There are many characteristics available today that can impact performance in a power device, but the five most important characteristics are
conduction efficiency, switching efficiency, breakdown voltage, cost, and size. These characteristics determine power density and achievable system frequency. In the above Table 1.1, by adjusting GaN mobility, the theoretical device conductivity (inverse of on-resistance) is found as a function of material and breakdown voltage.

In reference to Table 1.1, SiC and GaN are comparable in breakdown voltage and on-resistance due to their high electric field strength. GaN allows for even better mobility of electrons.

Gallium Nitride (GaN) is the next important semiconductor after Silicon which is used in huge range of applications for electronic and optoelectronic devices of high power, it’s the key material for next generation of high frequency and high power transistors. GaN is one type of semiconductor which has ability for use in large usage of high frequency devices. GaN has properties like breakdown of electric field and high electron drift velocity, it can be operated at high temperatures. GaN has a wide band-gap energy material (~3.4 eV at 300K) related to Si 1.12 eV and GaN 1.42 eV. This property of GaN is a good benefit for high temperature conditions. Since valence electrons jumps into the conduction band, the possibility of this occurrence during these operations will be much lower. Large bandgap semiconductors generates less noise, as a result GaN is a suitable one for making such high sensitive detectors in UV range [1].

GaN MESFET offers good device performance for the next generation of commercial use. Simultaneously, a SiC MESFET continues to mature in performance and manufacturing process stability. These devices now achieve a power density of approximately 4.0 W/mm and power-added efficiencies greater than 50% on a regular basis. The progress in GaN epitaxy has also led to rapid improvement in both GaN device
performance and reliability characteristics over the last 24 months. GaN power densities greater than 10 W/mm have been reported for HEMTs (high-electron-mobility transistors) using new epitaxial barrier layers and doped buffers. These new epi structures have also been combined with device field-plate structures to produce record-power density and efficiency. Extremely high efficiencies can be obtained from GaN HEMT devices [2]. Recently, there has been considerable interest in the growth of GaN and related alloys on Si substrates for the fabrication of light-emitting diodes, photodetectors, and the high-electron mobility AlGaN/GaN heterostructure because Si substrates have the advantages of low cost and huge size [3]. Previous studies showed that GaN-based materials on Si are of lesser quality than such materials grown on sapphire and on SiC, mainly due to the large lattice and thermal mismatches between GaN and Si. The mobility for a GaN MESFET is determined by the nucleation layer thickness. Therefore, the contribution of ionized impurity scattering in GaN film grown with GaN buffer layers is much smaller than that in GaN film grown with AlN buffer layers.

1.2 Why Gallium Nitride (GaN)

In comparison with other semiconductors GaN has taken over the superiority in temperature, speed, and power handling. The technology of GaN allows to implement essential future innovations where key requirement is efficiency.

GaN has its unique electronic properties. GaN offers five important characteristics like high dielectric strength, high current density, high operating temperature, low on-resistance, and high speed switching. These characteristics of GaN which compared to other silicon materials offers high exceptional carrier mobility, electrical breakdown characteristics and three times the bandgap [4].
Advantages of GaN

Figure 1.1: Advantages of GaN [4]

Figure 1.1 shows the advantages of GaN over GaAs. GaN also offers technical advantages like low voltage drop for increased output power, the possibility of unipolar devices, improved transient characteristics, improved switching speed, ability to handle high temperatures, and reduced electrical noise from its smaller system package.

1.3 Objective

The main objective of this project is to develop an analytical model of GaN based MESFET device. The parameters chosen for this model are based on the Wurtzite structure of GaN MESFET’s. The device performance for high power aided efficiency ($P_{AH}$) is observed by changing the active layer thickness, channel current and channel conductance. First step is to calculate the saturation current, channel conductance, transconductance, and characteristic switching time. Finally, these results will be verified by computer calculations and should agree with experimental data for a GaN MESFET.
Chapter 2 Theory on Gallium Nitride (GaN)

2.1 Crystal Structures

2.1.1 Wurtzite Structure Vs Zincblende Structure

Gallium nitride and its related compounds could crystallize both in the Zincblende structure as well as in the Wurtzite structure. However, the Zincblende and Wurtzite modifications of GaN, AIN and InN are related but show their significant differences which add an additional dimension to this field.

Crystallographically Zincblende structure and Wurtzite structure are very closely related in many terms. The bonding to the next neighbors is tetrahedral. The Bravais lattice of Wurtzite structure is hexagonal and the axis perpendicular to the hexagons which is usually labeled as c-axis. The structure along the c-axis can be thought as a sequence of the layer of atoms of the same element (e.g., all N or all Ga) built from regular hexagons. For the Zincblende lattice the stacking of the layers is:

\[ ...Ga_A Na_B N_B Ga_C N_C Ga_A Na_B N_B Ga_C N_C ... \]

But for the Wurtzite structure the changed stacking sequence is:

\[ ...Ga_A Na_B N_B Ga_A Na_B N_B Ga_A Na_B N_B ... \]

Figure 2.1 shows a clinographic projection of the Wurtzite structure, the most common crystal structure for GaN. The space group of Wurtzite structure is \( \text{C}_6 \text{v} \). Lattice constants a and b are equal (a=b) for the Wurtzite structure. There are Ga-atoms at (0, 0, 0) and at (2/3, 1/3, 1/2) and also there are N-atoms at (0, 0, u) and at (2/3, 1/3, ½+u). The value of ‘u’ is approximately 3/8. In fact for the value of u = 3/8, the nearest tetrahedral
are exactly the same for Wurtzite and Zincblende, while the positions differ for further neighbors. Table 2.1 shows the crystal lattice parameters for InN, AlN and GaN.

![Wurtzite structure](image)

**Figure 2.1: Wurtzite structure [10]**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>GaN</th>
<th>AlN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>3.111 Å</td>
<td>3.189 Å</td>
<td>3.544 Å</td>
</tr>
<tr>
<td>b</td>
<td>4.978 Å</td>
<td>5.185 Å</td>
<td>5.718 Å</td>
</tr>
<tr>
<td>u</td>
<td>0.382 Å</td>
<td>0.377 Å</td>
<td>0.379 Å</td>
</tr>
</tbody>
</table>

**Table 2.1: Lattice constants (a, b) & unit cell parameter (u) for GaN, AlN & InN [10]**

Figure 2.2 shows the Zincblende crystal structure of GaN. Few parameters for GaN

Zincblende structure are listed below

- Energy gap 3.2 eV
- An ideal angle: 109.47°
- Nearest neighbor: 19.5 nm
2.1.2 Polar Materials and Structures

An emerging class of materials is the (In, Al, Ga) N–based system for use in both optoelectronics and electronics. These materials are fundamentally different from conventional cubic semiconductors in that they exist normally in the Wurtzite phase and exhibit strong polarization in the <0001> direction (C-direction). Before studying HFET’s fabricated from these materials, it is necessary to first understand the effects that these polarization fields have on the electrical properties of the material [12].

Figure 2.3 (a) shows the ball and stick model of GaN in the basal plane and the associated polarization in the crystal. In the classical model, these polarizations charges exists on each unit cell. The sum of the internal polarization within the crystal is zero, as shown in Figure 2.3 (b), leaving ±Qπ charge at each end of the crystal forming a dipole. Since an unscreened dipole will result in a non-sustainable dipole moment, nature will always provide for a screening dipole by placing equal and opposite charges at or close to the charges of polarization dipole, as shown in Figure 2.3 (c).
Figure 2.3: (a) Stick ball representation of Wurtzite crystal structure. (b) Classical model polarization charge in a polar material such as GaN. (c) Crystal will draw in charge to screen the polarization dipole [12].

The spontaneous polarization charge density in GaN $n_\pi \sim 10^{13}$ cm$^{-2}$. This leads to an electric field $E_\pi$ which is given by:

$$E_\pi = \frac{Q_\pi}{\varepsilon} = \frac{n_\pi}{\varepsilon} \approx 1.6$ \text{MV/cm}$$

(2.1)

In a crystal of thickness $d = 1$ μm, the voltage across the material that results from this dipole charge is given by:

$$V_\pi = E_\pi \cdot d = 160 \text{ V}$$

(2.2)

Which is not sustainable, hence a screening dipole is essential. This raises the question of what is the nature of the charges that from the screening dipole. They could arise from counter ions from the atmosphere. This is probably the case for bulk polar
materials used in ceramic industry. However, this not probably the case for epitaxial GaN thin films, since these films can be created in an atmosphere free of counter ions, such as in an MBE reactor. This comes up with the question of whether screening of counter ions is possible without external counter ions. The following discussion addresses this issue.

Consider a lightly doped n-type GaN sample in the initial stages of growth, shown in Figure 2.3 (a). Due to lack of availability of GaN substrates, currently GaN is typically grown heteroepitaxially (on sapphire, Si or SiC substrates). The material at the substrate and thin film interface is highly defective and therefore capable of trapping mobile charges. The effect of the background n-type doping on the electric field profile within the material is assumed to be negligible when compared to the electric field generated by the polarization charges. The effects of surface states on the electrical properties of the material also ignored. Both of these effects will be considered later.

In the absence of surface states, as the material becomes thicker, the electric field in the material (given by the slope of the conduction and valence band) will remain constant until the valence band crosses the Fermi level as shown in Figure 2.3 (b). The thickness of the film $d_{cr}$ at which this occurs is given simply by

$$d_{cr} = \frac{E_g}{eE_r} = \frac{3.4 \text{ eV}}{1.6 \text{ MeV/cm}} \approx 215\text{Å}$$

(2.3)

where $E_g$= 3.4 eV is the Bandgap of GaN. Once $d > d_{cr}$, holes begin to accumulate at the surface (created by generating across the gap), leading to an equal electron concentration which drifts to the substrate-epi interface (the GaN N-face), creating a screening dipole. This is illustrated in Figure 2.3 (c). The magnitude of the screening charge $Q_{scr}$ increases continuously with epitaxial layer thickness. The evolution
of the screening charge with distance is obtained by recognizing that the maximum voltage across the structure is the bandgap of the material or

\[ \frac{1}{e} E_g = |\varepsilon| d = \left( \frac{Q_{\pi} - Q_{\text{scr}}}{\varepsilon} \right) d \]

(2.4)

\[ Q_{\text{scr}} = Q_{\pi} - \frac{eE_g}{\varepsilon d} \]

(2.5)

As \( d \to \infty \), \( Q_{\text{scr}} \to Q_{\pi} \), or in other words for very thick samples the polarization dipole is fully screened.

**Figure 2.4:** (a) Very thin GaN, for which surface states are not ionized. (b) Surface donors become ionized and polarization charge is screened [12].

If we now assume that there exists a surface donor state, a very similar situation develops, except that instead of holes providing the positive screening charge, ionized surface donors do. These states pin the Fermi level at the surface to create a built-in
voltage equal to the donor depth as illustrated in Figure 2.4. Figure 2.4 shows the schematic diagram of an n-type GaN sample along with charge profile and band diagram when the effects of surface states are taken into account.

As the epitaxial thickness increases, the donor level $E_{DD}$ approaches the Fermi level $E_F$ at the GaN surface and the screening charge $N_{DD}^+$ increases as given by the Fermi-Dirac occupancy probability

$$N_{DD}^+ = [1-f(E_{DD}(0))] N_{DD}$$

(2.6)

2.1.3 C-Plane Bulk GaN Substrates

Semiconductor epitaxy is best performed on native substrates in order to minimize interface effects and defect formation. Gallium nitride epitaxy on GaN substrates greatly improves a number of important device properties of subsequent GaN epitaxy when compared with heteroepitaxial GaN on SiC, sapphire, or silicon. The benefits in lattice constant mismatch, dislocation density and thermal conductivity can be seen in the Table 2.2 below [5].

<table>
<thead>
<tr>
<th></th>
<th>GaN on Bulk GaN</th>
<th>GaN on SiC</th>
<th>GaN on sapphire</th>
<th>GaN on Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice Constant Mismatch</td>
<td>0%</td>
<td>3.5% mismatch</td>
<td>14% mismatch</td>
<td>17% mismatch</td>
</tr>
<tr>
<td>Dislocation Density</td>
<td>$10^4 - 5 \times 10^6 / \text{cm}^2$</td>
<td>$1 \times 10^9 / \text{cm}^2$</td>
<td>$5 \times 10^9 / \text{cm}^2$</td>
<td>$1 \times 10^{11} / \text{cm}^2$</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>2.5 W/cm-K</td>
<td>1.3 W/cm-K</td>
<td>1.2 W/cm-K</td>
<td>1.0 W/cm-K</td>
</tr>
</tbody>
</table>
2.1.4 Growth of Wurtzite GaN onto Sappire

Figure 2.5 shows a schematic depiction of GaN, it clearly indicates the large lattice mismatch of GaN film onto a sapphire. Buffer layers are used to grow high quality GaN onto sapphire despite the large lattice mismatch and thermal mismatch.

![Schematic illustration of GaN growth onto sapphire surface](image)

Figure 2.5: Schematic illustration of GaN growth onto sapphire surface [6]

The band structure for GaN is shown in Figure 2.6 with few parameter that are chosen for $E_g, E_{M-L}, E_A, E_{SO}, E_{cr}$[6]. Where $E_g$ is Energy gaps, $E_{M-L}$ is Energy separation between M-L-valleys, $E_A$ is Energy separation between A-valley, $E_{SO}$ is Energy of spin-orbital, $E_{cr}$ is Energy of crystal-field.

![GaN Wurtzite Band Structure](image)

Figure 2.6: GaN Wurtzite Band Structure [6]
2.1.5 Band Structure of GaN Quantum Wells

The band diagram of GaN quantum well (QW) heterostructures is strongly affected by structural imperfections. Figure 2.7 contains results of positional dependence of the piezoelectric polarization, piezoelectric charge distribution and conduction band potential profile for several possible approximations.

![Band Structure of GaN Quantum Wells](image)

**Figure 2.7:** (a) Piezoelectric polarization, (b) Piezoelectric charge distribution and (c) Conduction band edge for the 2 nm GaN quantum well [7]

Where $L_1$ and $L_2$ are segregation lengths, $P_{\text{piezo}}$ is piezoelectric polarization in Figure 2.7
2.2 Electrical and Optical Properties of GaN

Recently, the activity in most of the electronic and optoelectronic applications shows group III-nitride semiconductor materials have led to an exponential increase. From the decades of study only GaN has changed from a research curiosity to a commercially important semiconductor material. This change is brought due to rapid progression over fabrication of viable devices and improvements in epitaxial growth of GaN. Gallium Nitride is an excellent material for high power and high speed due to its robust and versatile properties. On a monthly basis interest towards GaN has exploded in the past few years. GaN chips will be used more for applications that needed power management because Si has already reached its practical limits in power management chips.

The bandgap for GaN ranges from 3.4 eV to 6.2 eV by Ga and N ratio in the material. The GaN is being studied widely for applications in high frequency, high temperature and high power electronic devices [8]. The comparison of few electrical properties of GaN with other materials are listed below in Table 2.3. Table 2.4 shows few electrical parameter for GaN that are used in this project.
Table 2.3: Comparing electrical properties of GaN with other materials [8]

<table>
<thead>
<tr>
<th>Material</th>
<th>Bandgap (eV)</th>
<th>Electron Mobility (cm²/Vs)</th>
<th>Hole Mobility (cm²/Vs)</th>
<th>Critical Field $E_C$ (V/cm)</th>
<th>Thermal Conductivity $\sigma_T$ (W/m*K)</th>
<th>Coefficient of Thermal Expansion (ppm/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>InSb</td>
<td>0.17, D</td>
<td>77,000</td>
<td>850</td>
<td>1,000</td>
<td>18</td>
<td>5.37</td>
</tr>
<tr>
<td>InAs</td>
<td>0.354, D</td>
<td>44,000</td>
<td>500</td>
<td>40,000</td>
<td>27</td>
<td>4.52</td>
</tr>
<tr>
<td>GaSb</td>
<td>0.726, D</td>
<td>3,000</td>
<td>1,000</td>
<td>50,000</td>
<td>32</td>
<td>7.75</td>
</tr>
<tr>
<td>InP</td>
<td>1.344, D</td>
<td>5,400</td>
<td>200</td>
<td>500,000</td>
<td>68</td>
<td>4.6</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.424, D</td>
<td>8500</td>
<td>400</td>
<td>400,000</td>
<td>55</td>
<td>5.73</td>
</tr>
<tr>
<td>GaN</td>
<td>3.44, D</td>
<td>900</td>
<td>10</td>
<td>3,000,000</td>
<td>110 (200 Film)</td>
<td>5.4-7.2</td>
</tr>
<tr>
<td>Ge</td>
<td>0.661, I</td>
<td>3,900</td>
<td>1,900</td>
<td>100,000</td>
<td>58</td>
<td>5.9</td>
</tr>
<tr>
<td>Si</td>
<td>1.12, I</td>
<td>1,400</td>
<td>450</td>
<td>300,000</td>
<td>130</td>
<td>2.6</td>
</tr>
<tr>
<td>GaP</td>
<td>2.26, I</td>
<td>250</td>
<td>150</td>
<td>1,000,000</td>
<td>110</td>
<td>4.65</td>
</tr>
<tr>
<td>SiC (3C, b)</td>
<td>2.36, I</td>
<td>300-900</td>
<td>10-30</td>
<td>1,300,000</td>
<td>700</td>
<td>2.77</td>
</tr>
<tr>
<td>SiC (6H, a)</td>
<td>2.86, I</td>
<td>330-400</td>
<td>75</td>
<td>2,400,000</td>
<td>700</td>
<td>5.12</td>
</tr>
<tr>
<td>SiC (4H, a)</td>
<td>3.25, I</td>
<td>700</td>
<td></td>
<td>3,180,000</td>
<td>700</td>
<td>5.12</td>
</tr>
<tr>
<td>C (diamond)</td>
<td>5.46-5.6, I</td>
<td>2,200</td>
<td>1,800</td>
<td>6,000,000</td>
<td>1,300</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Table 2.4: Electrical parameters for GaN [8]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap</td>
<td>3.44 eV</td>
</tr>
<tr>
<td>Lattice constant</td>
<td>3.189 Å (a), 5.185 Å (c)</td>
</tr>
<tr>
<td>Breakdown field</td>
<td>$3.3 \times 10^6$ V/cm</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>9.5 (static), 5.35 (high freq.)</td>
</tr>
<tr>
<td>Optical phonon energy</td>
<td>91.8 meV</td>
</tr>
<tr>
<td>Ionization energy</td>
<td>Si (12 meV), Mg (210 meV)</td>
</tr>
<tr>
<td>Mobility (cm²V⁻¹S⁻¹)</td>
<td>$\mu_n$ =1000, $\mu_h$$\leq$200</td>
</tr>
</tbody>
</table>
Owing to intense activity in light emitters and detectors, much of the effort devoted to GaN has been directed toward determining its optical properties. Band-to-band luminescence is observed at room temperature in high-quality GaN layer. It is well-known that the so-called yellow luminescence is observed at room temperature in high-quality GaN layers. It is well-known that the so-called yellow luminescence centered around 560 nm has been observed in the undoped and Si-doped GaN layers grown by MOCVD and MBE.

Ogino and Aoki proposed that the yellow emission is due to a transition from a shallow donor to a deep acceptor level at \( E \approx E_v + 0.2\text{eV} \) from optically detected magnetic resonance experiments. Neugebauer and Van de Walle pointed out the deep acceptor level introduced by the Ga vacancy or related complexes is responsible for yellow luminescence using state-of-the-art first-principles calculations. The current uncertainty about the nature of the defect responsible for the yellow luminescence impedes efforts to control and improve the materials quality. The effects of the defects on GaN MESFETs are not well understood [9].
Figure 2.8: PL spectrum at 300K for an undoped Gallium Nitride layer grown on sapphire by MOCVD [10].

Figure 2.8 shows the photoluminescence (PL) spectrum at 300 K for the undoped GaN layer excited with the 325 nm line of a He-Cd laser. As shown in Figure 2.8, the PL spectrum at 300 K showed near-band emission at 362 nm with a full-width at half maximum of 48.5 meV and deep-level emission (yellow luminescence) centered at 532 nm. This deep-level emission has been associated with the Ga vacancy.

Figure 2.9 shows the near-band emission of the PL measurement at 4.2 K. The A- and B- exciton lines were clearly observed at 3.488 and 3.495 eV. A weak peak was observed at 3.488 and 3.495 eV. A weak peak was also observed at 3.503 eV, which is attributed to the first excited state of A-exciton. In addition to these free exciton lines, weak peaks corresponding to the recombination of acceptor-bound excitons (ABE) were observed at 3.466 and 3.471 eV. A weak shoulder corresponding to the recombination of donor-bound exciton, so-called I$_2$, was also observed at around 3.48 eV.
Carrier mobility is dependent on the temperature, electric field, doping concentration and material quality of a semiconductor. Nakamura and colleagues reported Hall mobility as high as 900 and 3000 cm²/Vs at 300 and 70 K, respectively. The mobility depends on the thickness of the GaN nucleation layer [10]. It is difficult to study the electrical properties of the undoped GaN layer because the undoped GaN shows high resistivity caused by the native defects such as nitrogen vacancies. However, such native defects in the undoped GaN layer play an important role in the GaN MESFET characteristics.
The dependence of the Hall mobility of the Si-doped n-GaN layer on temperature is shown in Figure 2.10. The Hall mobility first increased by $T^{1.5}$ and then decreased by $T^{1.5}$ with increasing temperature. The main scattering mechanisms that contribute to the Hall mobility appear to be ionized impurity scattering below 130 K and acoustic phonon scattering above 130 K. The Hall mobilities of the n-GaN layer were 585 cm$^2$/Vs with an electron carrier concentration of $1.1 \times 10^{17}$ cm$^{-3}$ at 300 K and 1217 cm$^2$/Vs with electron carrier concentration of $5.4 \times 10^{16}$ cm$^{-3}$.

Figure 2.10: Dependence of Hall mobility on temperature for a Si-doped n-GaN layer sapphire grown by MOCVD [10]
2.2.1 Excitation Energy Vs Temperature

For GaN Wurtzite structure the practical analysis of excitation energy vs. temperature with temperature dependence below 295K is given by:

\[ E_g(T) - E_g(0) = -5.08 \times 10^{-4} \frac{T^2}{(996 - T)}, \; (T \text{ in K}). \]

\[ E_g(300K) = 3.44 \text{ eV} \]

Where \( E_g \) is excitation energy gap. Figure 2.11 shows the graphical analysis of excitation energy under different temperatures below 300K.

![Graphical representation of excitation energy vs. temperature](image)

**Figure 2.11: Excitation energy vs. temperature [10]**

2.2.2 Bandgap Energy Vs Temperature

Using various techniques GaN samples were grown on different substrates. Below Figure 2.12 shows the graphical representation of bandgap vs. temperature for experimental data taken from four different samples [11].

20
2.2.3 *Intrinsic Carrier Concentration Vs Temperature*

The following Figure 2.13 shows the experimental analysis for both Wurtzite and Zincblende structures of GaN [11].

![Intrinsic carrier concentration vs. temperature for GaN, Wurtzite & Zinc Blende](image)

**Figure 2.13:** Intrinsic carrier concentration vs. temperature for GaN, Wurtzite & Zinc Blende [11].
2.2.4 Thermal and Mechanical Properties of GaN

The group III-nitride materials are ideal for high temperature devices due to their large energy bandgap, high peak electron velocity, high breakdown voltage and high electron sheet density in channels when used in a heterostructure. Utilizing group III-nitride materials, metal-semiconductor field effect transistors (MESFET’s), metal-insulator field effect transistors (MISFET’s), junction field effect transistors (JFET’s) and heterojunction field effect transistors (HFET’s) have been fabricated, recent reports on GaN based FET’s are concentrated on AlGaN/GaN HFET’s/HEMT’s and have demonstrated outstanding DC and RF characteristics as summarized in Table 2.5 below.

Table 2.5: Group III-nitride FET performances [12]

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum drain current density</td>
<td>1.43 A/mm</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>340 V between gate and drain</td>
</tr>
<tr>
<td>$f_T/f_{max}$</td>
<td>67/140GHz (0.15 µm gate)</td>
</tr>
<tr>
<td>Output power density</td>
<td>3.3 W/mm (18 GHz, 23% PAE, 2.4 dB gain)</td>
</tr>
<tr>
<td>Output power</td>
<td>3.2 W(4 GHz, 30% PAE, 2 mm gate)</td>
</tr>
</tbody>
</table>

2.2.5 Thermal Considerations

In general, an increase in operating temperature of an FET degrades the transconductance and maximum drain-source current (I) because both the low electric-field mobility and high electric-field electron velocity decrease with temperature. The mobility degradation results in an increase in the sheet resistivity and parasitic resistance.
The temperature increase also activates deep levels and forms an electrical leakage paths. The maximum operating temperature of a device is related to its semiconductor material properties and also to the fabrication technology. Even with degraded performance, working GaN based FETs have been demonstrated at temperatures up to 500°C.

The effects of temperature are important not only for high temperature operation but also for high power operation where self-heating becomes severe. A temperature increase due to the self-heating of an operating device is inversely proportional to the thermal conductivity (K). Utilizing SiC substrates in place of sapphire substrates for group III-nitride FET layers is important to minimize the self-heating effect of power devices. The other possible approach to overcoming the self-heating effect is to flip-chip group III-nitride FET’s to a highly thermally conductive substrate such as diamond or AIN. Some useful parameters of GaN are shown in below Table 2.6.

<table>
<thead>
<tr>
<th>Table 2.6: Thermal Properties of GaN [12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal conductivity</td>
</tr>
<tr>
<td>Thermal expansion</td>
</tr>
<tr>
<td>Elastic constants (GPa)</td>
</tr>
<tr>
<td>Piezoelectric constants</td>
</tr>
<tr>
<td>Hardness</td>
</tr>
</tbody>
</table>
2.2.6 Mechanical Properties

Cubic polytypes of GaN is grown on silicon by molecular beam epitaxy. The mechanical properties of the epitaxial layers were investigated by nanoindentation. The knowledge and control of mechanical properties and residual stress are essential for (MEMS and NEMS) micro and nano electromechanical systems. MEMS and NEMS cover a wide application range with varying designs from cantilevers/bridge up to membranes. The mechanical properties of Cubic GaN grown by plasma assisted molecular beam epitaxial growth on Si substrates as well as on SiC grown on Ge modified Si and Si.

Table 2.7: Mechanical Properties of GaN [12]

<table>
<thead>
<tr>
<th>Elastic Constants (GPa)</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{11}$</td>
<td>410.5±10</td>
</tr>
<tr>
<td>$C_{12}$</td>
<td>148.5±10</td>
</tr>
<tr>
<td>$C_{13}$</td>
<td>98.9±3.5</td>
</tr>
<tr>
<td>$C_{33}$</td>
<td>388.5±10</td>
</tr>
<tr>
<td>$C_{44}$</td>
<td>124.6±4.5</td>
</tr>
</tbody>
</table>
Chapter 3 MESFET

3.1 Metal-Semiconductor Field Effect Transistor

The MESFET was proposed and first demonstrated by Mead in 1966. The MESFET has three metal-semiconductor contacts: one Schottky barrier for the gate electrode and two ohmic contacts for the source and drain electrodes. MESFET is quite similar to a metal oxide semiconductor field effect transistor (MOSFET). The main difference is that in a MESFET, the MOS gate is replaced by a metal semiconductor (Schottky) junction [13].

A self-aligned GaN MESFET structure is shown in Figure 3.1 below. The heavily doped source and drain junctions are formed in an n-type epitaxial layer on semi-insulating GaN, which provides a low parasitic capacitance. The n-type region has a thickness (A) typically less than 200nm.

![Figure 3.1: Semi-insulating GaN](image)

The common source and drain contact materials used are AuGe alloys. Popular Schottky gate metals include Al, Pt, and W. The source and drain junctions are formed by
ion implantation after annealing. Since the source and drain implantation and implant annealing must be performed after gate formation, refractory metals that can withstand the annealing temperatures are preferred in a self-aligned MESFET.

Currently, MESFETs are fabricated on compound semiconductors, predominantly GaN. To form a better-quality MOS gate, a MESFET is an option that does not have a good dielectric.

A MESFET consists of a conducting channel between source and drain regions. The Schottky metal gate controls the carrier flow from source to drain. The channel control is obtained by altering the depletion layer width beneath the metal contact, and this modulates the thickness of the channel—and thereby the current.

The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to in the MOSFET because it permits the majority of carriers with less of a scattering effect. Since the carriers located in the inversion layer of a MOSFET have a wave function that extends into the oxide, their mobility—also referred to as “surface mobility”—is less than half of the mobility of bulk material. As the depletion region of a MESFET separates the carriers from the surface, their mobility is close to that of bulk material. The higher mobility leads to a higher current, transconductance, and transit frequency of the device. The two important advantages of a MESFET over a MOSFET are that (i) a MOSFET needs a substrate base, but a MESFET does not require it; and (ii) MOSFET performance depends on gate integrity, but MESFET does not.

The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky
This turn-on voltage is typically 0.7 V for GaAs Schottky diodes. It is better to select a high Schottky barrier height to prevent the low turn-on voltage. The threshold voltage therefore must be lower than this turn-on voltage. As a result, it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFETs [14].

Metal-semiconductor contacts are building blocks for MESFET and MODFET devices. Employing a Schottky barrier as the gate electrode and two ohmic contacts as the source and drain electrodes forms a MESFET. This three-terminal device is important for high-frequency applications, especially for monolithic microwave integrated circuits (MMIC). Most MESFETs are made with n-type III-V compound semiconductors because of their high electron mobilities and high average drift velocities.

The MODFET is a device with enhanced high-frequency performance. This device structure is similar to that of a MESFET except there is a heterojunction under the gate. A two-dimensional electron gas, i.e., a conductive channel, is formed at the heterojunction interface, and electrons with high mobility and high average drift velocity can be transported from the source through the channel to the drain.

3.1.1 MESFET Types

There are two main types of MESFETs: enhancement MESFETs and depletion MESFETs.

1. Depletion-mode MESFET: A MESFET is a depletion-mode MESFET if the depletion region does not extend completely to the p-type substrate. A depletion-mode MESFET is turned “OFF” upon the application of a negative gate-to-source voltage, which increases the width of the depletion region. In turn, it “pinches off” the channel and is “ON” or conductive when gate-to-source voltage is not applied.
2. **Enhancement-mode MESFET**: A MESFET is an enhancement-mode MESFET if the depletion region is too wide to pinch off the channel without applied voltage. Hence, the enhancement-mode MESFET is normally “OFF.” If a positive voltage is applied between the gate and source, the depletion region shrinks, and the channel becomes conductive. However, applying a positive gate-to-source voltage puts the Schottky diode in forward bias where a large current can flow.

3.2 **Basic Structure**

The base material of the transistor is GaN substrate. The fabrication of GaN transistor is conducted in such a way that right above the GaN substrate there is buffer layer and nucleation layer which is epitaxially grown in order to isolate the defects of the substrate from the transistor. Figure 3.2 shows the Schematic and Cross section of GaN based MESFET with recessed gate [15].

![Figure 3.2: Schematic and Cross Section of GaN MESFET with recessed gate [15]](image-url)
The channel layer is a thin, lightly doped conducting layer of semiconducting material which is epitaxially grown over buffer layer. Since GaN has electron mobility which is 20 times greater than the hole mobility, the conducting channel is always a n-type conducting channel. Finally, a layer with highly doped ($n^+$) is grown on the surface to aid in the fabrication of low-resistance ohmic contacts to the transistor and further this layer will be etched away in the channel region.

Ion implantation might be used alternatively to create the n-channel and the highly doped ohmic contact regions directly in the semi-insulating substrate. The source and drain are two ohmic contacts that are fabricated on the highly doped layer to provide access to the external circuit. A Schottky contact is fabricated between the two ohmic contacts [16].

### 3.3 Basic Operation of MESFET

To understand the operation of a MESFET, we consider the section under the gate as shown in Figure 3.3. The source is grounded, and the gate and drain voltage are measured with respect to the source. Under normal operating conditions, the gate voltage is zero or reverse biased and the drain voltage is zero or forward biased; that is, $V_G \leq 0$ and $V_D \geq 0$. Since the channel is n-type material, the device is referred to as an n-channel MESFET. Most applications use the n-channel MESFET rather than the p-channel MESFET because of higher carrier mobility in n-channel devices.
Figure 3.3: Cross section of the gate region of a MESFET [16]

When no gate voltage is applied and $V_D$ is small, as shown in Figure 3.4 (a), a small drain current $I_D$ flows in the channel. The magnitude of the current is given by $V_D/R$, where $R$ is the channel resistance. Therefore, the current varies linearly with the drain voltage. Of course, for any given drain voltage, the voltage along the channel increases from zero at the source to $V_D$ at the drain.

Thus, the Schottky barrier becomes increasingly reverse biased as we proceed from the source to the drain. As $V_D$ is increased, $W$ increases, and the average cross-sectional area for current flow is reduced. The channel resistance $R$ also increases. As a result, the current increases at a slower rate.
Figure 3.4: Variation of the depletion-layer width and output characteristics of a MESFET under various biasing conditions. (a) $V_G = 0$ and a small $V_D$. (b) $V_G = 0$ and at pinch-off. (c) $V_G = 0$ at post pinch-off ($V_D > V_{Dsat}$). (d) $V_G = -1V$ and a small $V_D$ [16]

As the drain voltage is further increased, eventually the depletion region touches the semi insulating substrate, as shown in Figure 3.4 (b). This happens when $W = a$ at the drain. The corresponding value of the drain voltage is then obtained, called the \textit{saturation voltage} ($V_{Dsat}$). At this drain voltage, the source and the drain are \textit{pinched off} or completely separated by a reverse-biased depletion region. The location $P$ in Figure 3.4 (b) is called the pinch-off point. At this point, a large drain current called the \textit{saturation current} ($I_{Dsat}$) can flow across the depletion region. This is similar to the situation caused by injecting carriers into a reverse-biased depletion region such as the collector-base depletion region of a bipolar transistor [17].
Beyond the pinch-off point, as $V_D$ is increased further, the depletion region near the drain will expand and point $P$ will move toward the source, as indicated in Figure 3.4 (c). However, the voltage at point $P$ remains the same, $V_{Dsat}$. Thus, the number of electrons per unit time arriving from the source to point $P$ and hence the current flowing in the channel, remain the same because the potential drop in the channel from source to point $P$ does not change. Therefore, for drain voltages larger than $V_{Dsat}$, the current remains essentially at the value $I_{Dsat}$ and is independent of $V_D$.

When a gate voltage is applied to reverse bias the gate contact, the depletion-layer width $W$ increases. For a small $V_D$, the channel again acts as a resistor but its resistance is higher because the cross-sectional area available for current flow is decreased. As indicated in Figure 3.4 (d), the initial current is smaller for $V_G = -1$ V than for $V_G = 0$. When $V_D$ is increased to a critical value, the depletion region again touches the semi insulating substrate [18].

For an $n$-channel MESFET, the gate voltage is negative with respect to the source, so we use the absolute value of $V_G$. The application of a gate voltage $V_G$ reduces the drain voltage required for the onset of pinch-off by an amount equal to $V_G$. 
The operation of MESFET is easily understood by considering the I-V characteristics [19] of the device without the gate contact as shown in the Figure 3.3 below.

![Figure 3.3 I-V Characteristics for an ungated MESFET][20]

Figure 3.4 shows the Schematic of an Ungated MESFET. The Current will flow between the two contacts if small voltage is applied between source and drain. As the voltage is increased, the current also increases linearly. The equation for $I_D$ is given by

$$I_D = \frac{V_D}{R_D + R_S + R_{DS}}$$
where $R_{DS}$ is channel resistance, $R_S$ is source resistance and $R_D$ is drain resistance.

If the voltage is further increased, the applied electric field will be greater than the required electric field for saturation of electron velocity [20].
Chapter 4 GaN MESFET

4.1 Introduction to GaN MESFET

A simple theoretical consideration, experimental data [21–23], a two-dimensional computer analysis [24], and the most recent two-dimensional calculation [25] show that the standard Shockley theory of FETs [26–27] aligns with computer calculations [24–25] and experimental data [21, 28]. In this project it is assumed that the current saturation occurs when the average electric field under the gate reaches the sustaining field ($E_s$).

$$E_s = \frac{v_s}{\mu}$$ (4.1)

Figure 4.1: Saturation electron drift velocity versus domain sustain field

Where $v_s$ is the saturation electron drift velocity, and $\mu$ is the low-field mobility.

Figure 4.1 shows the graphical representation of saturation electron drift velocity versus domain sustain field. In fact, if the doping fluctuations are small and rather special boundary conditions are satisfied under the gate [29], the domain might form when the
electric field is larger than the electron peak velocity field $E_p$ rather than $E_S$ so that the hysteresis effects and negative differential resistance are due to the domain formation [21, 22]. This possibility is not considered in this simplified approach [25].

From the formal point of view, a condition similar to that in [30–32] where the MESFET saturation was at the peak velocity (avoiding domain and formation) was envisaged. But the physical interpretation and approximations used are different.

The transport properties of AlN, InN, and GaN have been studied using analytical calculations and Mante Carlo simulations. These properties depend on materials quality, and the values given in Table 4.1 represent theoretically predicted values. However, many of these parameters are still to be determined more accurately. Table 4.1 illustrates some important differences between GaN-based semiconductors and their conventional counterparts such as Ge, Si, III-V, or II-VI compounds. The first difference is crystal symmetry. GaN-based semiconductors more often have hexagonal (Wurtzite) crystal structure and grow along the hexagonal (polar axis). These have very pronounced piezoelectric and pyroelectric properties that play an important role in the physics of GaN-based devices.
Table 4.1: Parameters of GaN, AlN, and InN for Wurtzite crystal structure [21]

<table>
<thead>
<tr>
<th></th>
<th>Units</th>
<th>GaN</th>
<th>AlN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symmetry</td>
<td>-</td>
<td>Wurtzite/</td>
<td>Wurtzite</td>
<td>Wurtzite</td>
</tr>
<tr>
<td></td>
<td></td>
<td>zinc blende</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Density</td>
<td>g/cm</td>
<td>6.15</td>
<td>3.23</td>
<td>6.81</td>
</tr>
<tr>
<td>Static Dielectric Constant</td>
<td></td>
<td>8.9</td>
<td>8.5</td>
<td>15.3</td>
</tr>
<tr>
<td>High-Frequency Dielectric Constant</td>
<td></td>
<td>5.35</td>
<td>4.77</td>
<td>8.4</td>
</tr>
<tr>
<td>Energy Gap (Γ Valley)</td>
<td>eV</td>
<td>3.39</td>
<td>6.2</td>
<td>1.89</td>
</tr>
<tr>
<td>Effective Mass (Γ Valley)</td>
<td>m_e</td>
<td>0.20</td>
<td>0.48</td>
<td>0.11</td>
</tr>
<tr>
<td>Polar Optical Phonon Energy</td>
<td>meV</td>
<td>91.2</td>
<td>99.2</td>
<td>89.0</td>
</tr>
<tr>
<td>Lattice Constant, a (c)</td>
<td>Å</td>
<td>3.189 (5.185)</td>
<td>3.11 (4.98)</td>
<td>3.54 (5.70)</td>
</tr>
<tr>
<td>Electron mobility</td>
<td>cm²/Vs</td>
<td>1000</td>
<td>135</td>
<td>3200</td>
</tr>
<tr>
<td>Hole mobility</td>
<td>cm²/Vs</td>
<td>30</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>Saturation velocity</td>
<td>cm/s</td>
<td>2.5 x 10⁷</td>
<td>1.4 x 10⁷</td>
<td>2.5 x 10⁷</td>
</tr>
<tr>
<td>Peak velocity</td>
<td>cm/s</td>
<td>3.1 x 10⁶</td>
<td>1.7 x 10⁶</td>
<td>4.3 x 10⁶</td>
</tr>
<tr>
<td>Peak velocity field</td>
<td>kV/cm</td>
<td>150</td>
<td>450</td>
<td>67</td>
</tr>
<tr>
<td>Breakdown field</td>
<td>V/cm</td>
<td>&gt;5 x 10⁶</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Light hole mass</td>
<td>m_e</td>
<td>0.259</td>
<td>0.471</td>
<td></td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>W/cm-K</td>
<td>1.5</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Melting Temperature</td>
<td>ºC</td>
<td>2530</td>
<td>3000</td>
<td>1100</td>
</tr>
</tbody>
</table>

4.2 Saturation Current, Small-Signal Parameters, Switching Time, and Power-Delay Product

The elemental section of a junction field-effect transistor before the onset of saturation is shown in the figure below.
The elemental section of the channel employed in the derivation of the current-voltage characteristics of junction field-effect transistors [27]

The voltage drop across the elemental section of the channel is given by

\[ dV = I_D dR = \frac{I_D dy}{q \mu \bar{n} N_D Z [d - 2W(y)]} \]

(4.7)

where, \( R = \) channel resistance,

\( N_D = \) donor concentration in the active channel,

\( L = \) channel length,

\( Z = \) channel width,

\( d = \) active channel thickness,

\( w = \) width of the depletion region,

\( I_D = \) drain current,
\(q = \text{charge of electron, and}\)

\(\mu_n = \text{mobility of electron.}\)

The resistance of the channel is given by

\[
R = \frac{L}{q\mu_n N_D Z [d - 2W]} \tag{4.8}
\]

The depletion region width at distance \(y\) from the source is given by

\[
W(y) = \sqrt{\frac{2\varepsilon\varepsilon_0 [V(y) + V_{Bl} - V_G]}{q N_D}} \tag{4.9}
\]

The fundamental equation of field-effect transistors is given by

\[
I_{ch} = g_0 \left\{ V_i - \frac{2}{3} \left[ \frac{\left( V_i + V_{Bl} - V_G \right)^3}{V_{po}^2} - \frac{\left( V_{Bl} - V_G \right)^3}{V_{po}^2} \right] \right\} \tag{4.10}
\]

where, \(I_{ch} = \text{channel current (see Figure 4.3)},\)

\(V_i = \text{voltage drop across the gate region},\)

\(V_{Bl} = \text{built-in voltage between the channel and substrate},\)

\(V_G = \text{gate voltage},\)

\(g_0 = \text{channel conductance},\)

\(V_{po} = \text{the pinchoff voltage},\)
$g_0$ is the channel conductance given by,

$$g_0 = \frac{q\mu N_D W A}{W_G} \quad (4.11)$$

and $V_{p0}$ is the pinchoff voltage given by,

$$V_{p0} = \frac{q N_D A^2}{2\epsilon_0 \epsilon} \quad (4.12)$$

where, $q$ = electronic charge,

$N_D$ = doping density,

$\epsilon_0 \epsilon$ = permittivity,

$A$ = active channel thickness,

$W$ = gate width, and

$W_G$ = gate length.

---

Figure 4.3: MESFET geometry [27]
Equation (4.5) is valid when

\[ V_i < V_s = E_s W_G \]  

(4.13)

for typical MESFET parameters \( W_G \sim 1 \mu m \)

\[ V_s << V_{Bi} - V_G \]  

(4.14)

and the channel current is almost linear up to the saturation point

\[ I_{ch} = g_0 \left[ 1 - \frac{A_0}{A} \right] V_i = g_d V_i \]  

(4.15)

here

\[ A_0 = \left[ \frac{2 \epsilon_0 \epsilon (V_{Bi} - V_G) V_p}{q N_D} \right]^{1/2} \]  

(4.16)

which is further simplified into the following equation by substituting values for \( V_{po} \).

\[ A_0 = A \left[ \frac{V_{Bi} - V_G}{V_{po}} \right]^{1/2} \]  

(4.17)

and

\[ g_d = g_0 \left[ 1 - \frac{A_0}{A} \right] \]  

(4.18)

where \( g_d \) is the drain conductance. The saturation current \( I_{sat} \) is given by

\[ I_{sat} = g_d V_s \]  

(4.19)

In order to check equations (4.13) and (4.14), the dependencies of \( g_d \) and \( I_{sat} \) on the active channel thickness \( A \) in the frame of the two-dimensional model developed in [25] are calculated. The results of a two-dimensional computer analysis and experimental data [21, 28] are then compared. This comparison shows good agreement.
The transconductance in the saturation region is equal to

\[ g_m \approx \frac{\partial I_{ch}}{\partial V_G} = g_0 \left( \frac{(V_i + V_{Bi} - V_G)^2}{V_{po}^2} - \frac{(V_{Bi} - V_G)^2}{V_{po}^2} \right)^{1/2} \]  

(4.20)

Or, taking equation (4) into account

\[ g_m \approx g_0 \frac{V_s}{2 \left[ V_{po} (V_{Bi} - V_G) \right]^{1/2}} \left[ \frac{\epsilon_0 \epsilon q N_D}{V_{po}^2} \right]^{1/2} \cdot V_s \cdot W \]  

(4.21)

(This is completely different from the Shockley theory according to which the transconductance in the saturation region exactly equals the drain conductance in the linear region given by equation \[4.13\]). Equation \[4.16\] also agrees well with experimental data \[21\] and with computer calculations performed in the frame of the two-dimensional model developed in \[25\].

A smaller value of \( g_m \) measure in \[18\] might be due to the series gate-to-source resistance \( R_s \) and source contact resistance \( R_{sc} \) because the observed value \( g_m(\text{obs}) \) of the transconductance is given by \[27\].

\[ g_m(\text{obs}) = \frac{g_m}{1 + (R_s + R_{sc})g_m} \]  

(4.22)

The drain-to-gate and gate-to-source capacitances \( C_{dg} \) and \( C_{gs} \) (the simplified equivalent circuit of a GaN MEESFET is shown in Figure 4.4) are given by,
Figure 4.4: Simple equivalent circuit of a GaN MESFET [27]

\[
C_{dg} = \frac{2\sqrt{2} WW_G (e_0 e q N_D)^{3/2}}{3 A V_i^2} \left[ \frac{3}{2} V_i (V_i + V_{Bi-V_G})^{1/2} - (V_i + V_{Bi-V_G})^{3/2} \right] \quad (4.23)
\]

\[
C_{gs} = \frac{2\sqrt{2} WW_G (e_0 e q N_D)^{1/2}}{3 A V_i^2} \left[ (V_i + V_{Bi-V_G})^{3/2} - (V_{Bi-V_G})^{3/2} - \frac{3}{2} (V_{Bi-V_G})^{1/2} \right] \quad (4.24)
\]

The cutoff frequency [33] in terms of conductance and capacitance has been calculated and given below:

\[
f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs}} \quad (4.25)
\]
For the case when \( V_i \ll V_{Bi} - V_G \) the value of \( f_T \) becomes,

\[
f_T \approx \frac{1}{\pi} \frac{v_s}{W_G}
\]

so that \( f_T \sim 25.5 \text{ GHz} \) for a 1-\( \mu \text{m} \) gate device. It agrees well with estimates given in [23], where another formula derived in [32] was used:

\[
f_T \approx \frac{1}{2\pi} \frac{b_p}{W_G}
\]

where \( v_p \) is a peak electron velocity. It is also in accord with the computer calculations [25]. These expressions can be simplified further. The switching time characteristic of a GaN MESFET can be expressed by [34, 25]:

\[
\tau = \frac{QV_s}{I_{sat}}
\]

By substituting the values for \( Q, I_{sat} \), and \( V_s \) the value of switching time (\( \tau \)) becomes

\[
\tau \approx \frac{W_G A_0}{v_s (A - A_0)}
\]

For typical parameters of GaN MESFET \( A_0 \) is about 0.1 \( \mu \text{m} \). That sets an ultimate limit for a characteristic switching time in picosecond range.

The power required by a MESFET at the saturation point is given by

\[
P = qN_D v_s W (A - A_0) E_s, W_G = \frac{qN_D W W_G^2 A_0 E_s}{\tau}
\]
The power-delay product is equal to

\[ P_t \approx qN_D W W_G^2 A_0 E_s = W W_G^2 E_s \sqrt{2\varepsilon_0 \varepsilon q N_D (V_{Bi} - V_G)} \]  

(4.31)

This expression has a simple physical meaning. This is an amount of work to be done in order to move the total charge in the depletion layer \( q N_D W W_G^2 A_0 \) in the electric field \( E_s \) at the distance \( W_G \). There is great potential of GaN MESFET for high-speed low-power integrated circuits [36, 37]. A GaN MESFET can yield a power-delay product in a femtojoule range in good agreement with experimental data [35].
Chapter 5 Results and Discussion

The analytical model of a GaN-based MESFET device has been developed, and the simulated result using the MATLAB tool has been presented here to study the channel current, channel conductance and gate capacitance in order to determine the device performance by optimizing, the device structure, doping concentration, and other intrinsic and extrinsic parameters.

Figure 5.1: Channel current versus active channel thickness

Figure 5.1 shows the plot of channel current ($I_{ch}$) versus device thickness ($A$) for different gate voltages ($V_G$) of -24V, -12V, and 0V with drain voltage ($V_D$) of 0.151V,
channel doping concentration ($N_D$) of $1 \times 10^{17}$ cm$^{-3}$; channel length ($W_g$) of 1.0 $\mu$m; channel width ($W$) of 500 $\mu$m and substrate concentration ($N_a$) of $1 \times 10^{15}$ cm$^{-3}$.

The channel current linearly increases with an increase of channel active thickness from 0.7 $\mu$m to 0.9 $\mu$m, which reflects the pinch-off voltage ($V_{po}$) reasonably agreed with the channel current. This plot is an important foundation to design the high power GaN MESFET device. The gate voltage of $V_G = 0$V shows the large current, which confirms the device working as normally-on mode. The linear variation of the active layer thickness with channel current exhibits device performance for high power-aided efficiency (PAE) where the channel current can be controlled by changing the active channel thickness and channel doping concentration. Figure 5.1 has been plotted using equation (4.10).

![Channel saturation current vs. gate voltage](image)

**Figure 5.2: Channel current versus gate voltage**

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Figure 5.2 demonstrates the transfer characteristics in linear region and the plot shows the channel current versus gate voltage ($V_G$) for different drain voltage ($V_D$) of 0.151V, 1.151V and 2.151V, channel doping concentration ($N_D$) of 1x10$^{17}$cm$^{-3}$; channel length ($W_G$) of 1.0 µm, channel width ($W$) of 500 µm and substrate concentration ($N_A$) of 1x10$^{15}$cm$^{-3}$. The channel current ($I_{ch}$) linearly increases with an increase of gate voltage ($V_G$). The device shows the property of the depletion-mode (normally-ON) MESFET, and threshold voltage was found to be -27V, which agrees well with the channel active thickness and material properties. This plot has been generated by using the equation (4.10) with respect to gate voltage ($V_G$).

![Channel Conductance Vs. Active Channel Thickness](image)

**Figure 5.3: Channel conductance versus active channel thickness**

Figure 5.3 presents a plot of channel conductance ($g_0$) versus active channel thickness ($A$) for different gate voltages ($V_G$) of -24V, -12V, and 0V with constant drain
voltage ($V_i$) of 0.151V, channel doping concentration ($N_D$) of $1 \times 10^{17}$ cm$^{-3}$, channel length ($W_G$) of 1.0 $\mu$m, channel width ($W$) of 500 $\mu$m and substrate concentration ($N_A$) of $1 \times 10^{15}$ cm$^{-3}$. The channel conductance shows a linear variation with the active channel thickness from 0.7 $\mu$m to 0.9 $\mu$m. The channel conductance variation is an important parameter for (PAE) and high-frequency performance. The device cut-off frequency and device (PAE) depends on the channel conductance, which is controlled by active channel thickness. This plot has been generated by using the equation (4.18).

Figure 5.4: Drain-to-gate capacitance versus drain-to-source voltage

The Figure 5.4 presents a plot of drain-gate capacitance ($C_{dg}$) versus drain-source voltage ($V_i$) for different gate voltages ($V_G$) of 0, -3, -6V with channel doping concentration ($N_D$) of $1 \times 10^{17}$ cm$^{-3}$, channel length ($W_G$) of 1.0 $\mu$m, channel width ($W$) of
500 μm and substrate concentration (N_A) of 1x10^{15} \text{cm}^{-3}. The drain-to-gate capacitance (C_{dg}) exponentially decreases with the increase of drain-to-source voltage (V_i) and finally saturates at higher drain-to-source voltage (V_i). The value of drain-to-gate capacitance (C_{dg}) exponentially decreases with drain-to-source voltage (V_i) due to high reverse voltage at the drain-end. This plot has been generated by using the equation (4.23).

**Figure 5.5: Gate-to-source capacitance versus gate-source voltage**

The Figure 5.5 exhibits a plot of gate-to-source capacitance (C_{gs}) versus gate-to-source voltage (V_G) for different drain-source voltage (V_i) of 10, 20, 30V with constant channel doping concentration (N_D) of 1x10^{17} \text{cm}^{-3}, channel length (W_G) of 1.0 μm, channel width (W) of 500 μm and substrate concentration (N_A) of 1x10^{15} \text{cm}^{-3}. The gate-to-source capacitance (C_{gs}) exponentially increases with increase of gate voltage(V_G). The plot shows that the increase of gate voltage (V_G) is responsible for the increase of
gate-to-source capacitance ($C_{gs}$) rather than the influence of drain-to-source voltage ($V_{ds}$).
The larger gate-to-source capacitance ($C_{gs}$) value is obtained for drain-to-source voltage ($V_i$) of 10V compared drain-to-source voltage ($V_i$) of 30V. This plot has been generated by using the equation (4.24).

The gate capacitance due to the effect of gate-to-source capacitance ($C_{gs}$) and drain-to-gate capacitance ($C_{dg}$) shows a valuable intrinsic parameter to estimate the switching time and cut-off frequency for determination of device performance. Further scope of this research works can be extended to analyze for high power RF device performance using the channel conductance.
Chapter 6 Conclusion

In this graduate project, the detailed study on GaN shows how it has taken over the superiority in high operating temperature, high speed switching, power handling and high exceptional carrier mobility compared with other semiconductors. The research on GaN electrical and optical properties demonstrates the importance of GaN in electronic and optoelectronic devices. The simulation results of channel current vs. active channel thickness, channel conductance vs. active channel thickness, channel current vs. gate voltage, drain-to-gate capacitance vs. drain-to-source voltage, and gate-to-source capacitance vs. gate-source voltage are presented in graphs.

The channel current, and channel conductance versus active channel thickness, channel current versus gate-source voltage and gate capacitance (gate-source capacitance and gate-drain capacitance) have been studied to evaluate the GaN device performance for high power RF device application. The analytical results obtained here agree well with the results of computer calculations and experimental data. The frequency performance of GaN MESFET device has been outlined by the study of the gate capacitance.

The power-aided efficiency ($P_{AE}$) can be enhanced by the study of the active channel thickness effect on both the channel current and channel conductance. The simplicity of the proposed model makes it very suitable for the analysis and computer-aided design of microwave FET amplifiers and high-speed integrated circuits. In order to perform the detailed study of frequency response of the device, the scope of the research can be extended to develop the analytical model to evaluate the transconductance.
References


[18] Retrieved March 24, 2014, from
http://www.iue.tuwien.ac.at/phd/ayalew/node106.html


http://www.iue.tuwien.ac.at/phd/ayalew/node107.html


APPENDIX A

A  Active channel thickness

$C_{dg}$  Drain-to-gate capacitance

$C_{gs}$  Gate-to-source capacitance

$C_s$  Fringe capacitance

$d_d$  Depletion layer width

$D_n$  Diffusion constant

E  Electric field

$E_b$  Breakdown electric field

$E_m$  Maximum domain field

$E_p$  Electron peak velocity field

$E_s$  Domain sustain field

$E_v$  Electric field of the field electron drift velocity saturation

$\varepsilon_0\varepsilon$  Permittivity

$f_T$  Cutoff frequency

$g_d$  Channel conductance

$g_m$  Transconductance

$g_m(\text{obs})$  Observed value of the transconductance
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ch}$</td>
<td>Channel current</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current</td>
</tr>
<tr>
<td>$I_{sat}$</td>
<td>Saturation current</td>
</tr>
<tr>
<td>$I_{sub}$</td>
<td>Substrate current</td>
</tr>
<tr>
<td>$L_d$</td>
<td>Debye length</td>
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<tr>
<td>$\mu$</td>
<td>Low-field mobility</td>
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<tr>
<td>$N_D$</td>
<td>Doping density</td>
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<tr>
<td>P</td>
<td>Power</td>
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<tr>
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<td>Total positive charge under the gate</td>
</tr>
<tr>
<td>$Q_s$</td>
<td>Stray charge</td>
</tr>
<tr>
<td>q</td>
<td>Electronic charge</td>
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<tr>
<td>$R_D$</td>
<td>Drain-to-source section resistance</td>
</tr>
<tr>
<td>$R_{dc}$</td>
<td>Drain contact resistance</td>
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<tr>
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<td>Gate-to-source section resistance</td>
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<td>Source contact resistance</td>
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<td>$R_{sub}$</td>
<td>Substrate resistance</td>
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<td>Switching time</td>
</tr>
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<td>Dielectric relaxation time</td>
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<tr>
<td>Symbol</td>
<td>Description</td>
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<td>-------------</td>
</tr>
<tr>
<td>$\tau_T$</td>
<td>Energy relaxation time</td>
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<tr>
<td>$V_{Bi}$</td>
<td>Built in voltage</td>
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<tr>
<td>$V_C$</td>
<td>Voltage drop across source-gate and gate-drain sections</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Drain voltage</td>
</tr>
<tr>
<td>$V_{dom}$</td>
<td>Domain voltage</td>
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<tr>
<td>$V_G$</td>
<td>Gate voltage</td>
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<tr>
<td>$V_l$</td>
<td>Voltage drop across the gate</td>
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<tr>
<td>$V_{po}$</td>
<td>Pinch-off voltage</td>
</tr>
<tr>
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<td>Electron saturation drift velocity</td>
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<td>Gate width</td>
</tr>
<tr>
<td>$W_G$</td>
<td>Gate length</td>
</tr>
<tr>
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<td>Gallium Nitride</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
</tbody>
</table>
APPENDIX B

Matlab code for channel current ($I_{ch}$) and channel conductance ($g_o$)

```matlab
clc; %clear the command window

clear all; %clears all function variables, workspaces, etc

close all; %close all open files

q = 1.6e-19; % charge of an electron

epsilon = 8.9*8.8542e-14; % EPS=Eo*Es

Nd = 1.0e+17; % donor concentration

Na = 1.0e+15; % acceptor concentration

ni =1.0e-9; % intrinsic concentration

u=1000; % mobility of an electron

w=500e-4; % Gate width

wg=1*(10^-4); % Gate length

A=[0.7*(10^-4) 0.8*(10^-4) 0.9*(10^-4)]; % Device thickness

Vi=0.151; % Voltage drop across the gate, here Vi is Vds

Vbi= (0.0259) * (log((Na*Nd)/(ni*ni))); % Built-in Voltage

Vs= 0.8*(10^7); % Velocity

Vg=[-24 -12 0]; % Gate Voltage
```
\[ k = 0.942 \times \left( w \times w_g \times (\varepsilon \times q \times N_d)^{0.5} / (V_i^2) \right) \] % Cdg, Cgs common

\[ E_s = V_i / w_g; \]

\[ \text{for } i = 1:3 \quad \% \text{looping the values for } V_g \]

\[ \text{for } m = 1:3 \]

\[ j(i) = V_i + V_{bi} - V_g(m); \]

\[ V_{p0} = ((q \times N_d \times A(i) \times A(i)) / (2 \times \varepsilon)) \]

\[ g_0 = (q \times u \times N_d \times w \times A(i)) / w_g; \]

\[ \text{nume}(m) = \left( 2 \times ((V_i + V_{bi} - V_g(m))^{1.5}) - (V_{bi} - V_g(m))^{1.5}) \right); \]

\[ \text{denom} = (3 \times (V_{p0}^{1.5})) \]

\[ I(i,m) = g_0 \times (V_i - (\text{nume}(m) / \text{denom})); \]

\[ A_0(i) = A(i) \times ((V_{bi} - V_g(m)) / V_{p0})^{0.5}; \]

\[ g_d(i) = g_0 \times (1 - (A_0(i) / A(i))); \]

\[ T(i) = (w_g / V_s) \times (A_0(i) / (A(i) - A_0(i))); \]

\[ C_{dg}(i) = k \times (1.5 \times V_i \times (j(i)^{0.5}) - (j(i)^{1.5}) + (V_{bi} - V_g(m))^{1.5}); \]

\[ C_{gs}(i) = k \times ((j(i)^{1.5}) - (V_{bi} - V_g(m))^{1.5} - (1.5 \times (V_{bi} - V_g(m))^{0.5}) \times V_i); \]

\[ \text{end} \]

\[ \text{end} \]
figure(1);

plot(A, I);

xlabel('Active Channel Thickness(A) in um'); ylabel('Channel Current(Ich) in mA');
title('Channel Current Vs. Active Channel Thickness');

hleg1 = legend('Vg=-24v', 'Vg=-12v', 'Vg=0v');

figure(2);

plot(Vg, I);

xlabel('Gate Voltage in V'); ylabel('Channel Current in a/cm');
title('Channel saturation current Vs. gate voltage');

hleg1 = legend('Vi=0.151v', 'Vi=2.151v', 'Vi=3.151v');

figure(3);

plot(A, gd);

xlabel('Active Channel Thickness(A) in um'); ylabel('Channel Conductance(gd) in mho');
title('Channel Conductance Vs. Active Channel Thickness');
Matlab code for plots drain-gate capacitance ($C_{dg}$) and gate-to-source capacitance ($C_{gs}$)

cle; %clear the command window

clear all; %clears all function variables, workspaces, etc

close all; %close all open files

q = 1.6e-19; % charge of an electron

epsilon = 8.9*8.8542e-14; % EPS=Eo*Es

Nd = 1.0e+17; % donor concentration

Na = 1.0e+15; % acceptor concentration

ni = 1.0e-9; % intrinsic concentration

u = 1000; % mobility of an electron

w = 500e-4; % Gate width

wg = 1*(10^-4); % Gate length

A = [0.9*(10^-4)]; % Device thickness

Vi = 0:1:20 % Gate Voltage

Vg = [0 -3 -6];

V2i = [10 20 30];

V2bi = 3;

V2g = [0 -1 -2 -3 -4 -5 -6 -7]

Vbi = (0.0259) * (log((Na*Nd)/(ni*ni))); % Built-in Voltage

for i = 1:21 % looping the values for Vg

    for m = 1:3

        j(i) = Vi(i) + Vbi - Vg(m);

    end

end
\[ k = 0.942 \times ((w \times w_g \times (\varepsilon \times q \times N_d)^{0.5})/(V_{i(i)} \times V_{i(i)})) \]

\[ V_{p0} = ((q \times N_d \times A \times A)/(2 \times \varepsilon)) \]

\[ C_{dg}(i,m) = -(k/A) \times (-1.5 \times V_{i(i)} \times (j(i)^{0.5})+(j(i)^{1.5})-(V_{bi} - V_{g(m)})^{1.5}) \]

\[ V_{p0} = (((q \times N_d \times A \times A)/(2 \times \varepsilon)) \]

\[ C_{gs}(i,m) = (k(m)/A) \times (j2(i)^{1.5})-(V_{bi} - V_{gs}(i))^{1.5}-(1.5 \times (V_{bi} - V_{gs}(i))^{0.5}) \times V_{2i(m)} \]

\[ \text{end} \]

\[ \text{end} \]

\[ \text{for } i = 1:8 \]

\[ \text{for } m = 1:3 \]

\[ j2(i) = V_{2i(m)} + V_{2bi} - V_{2g}(i); \]

\[ k(m) = 0.942 \times ((w \times w_g \times (\varepsilon \times q \times N_d)^{0.5})/(V_{2i(m)} \times V_{2i(m)})); \]

\[ V_{p0} = ((q \times N_d \times A \times A)/(2 \times \varepsilon)) \]

\[ C_{gs}(i,m) = (k(m)/A) \times (j2(i)^{1.5})-(V_{bi} - V_{2g}(i))^{1.5}-(1.5 \times (V_{bi} - V_{2g}(i))^{0.5}) \times V_{2i(m)} \]

\[ \text{end} \]

\[ \text{end} \]

\[ \text{figure(1);} \]

\[ \text{plot(Vi,Cdg);} \]

\[ \text{xlabel(} \text{'Drain-to-Source Voltage (Vi)' }; \text{ylabel(} \text{'Drain-to-Gate capacitances (Cdg) in pF'}); \]

\[ \text{title(} \text{'Drain-to-Gate capacitances Vs. Drain-to-Source Voltage'}); \]

\[ \text{hleg1 = legend(} \text{'Vg=0v','Vg=-3v','Vg=-6v'}); \]

\[ \text{figure(2);} \]

\[ \text{plot(V2g,Cgs);} \]

\[ \text{xlabel(} \text{'Gate-to-Source Voltage (Vg)' }; \text{ylabel(} \text{'Gate-to-Source capacitance (Cgs) in pF'}); \]

\[ \text{title(} \text{'Gate-to-Source capacitance Vs. Gate-to-Source Voltage'}); \]

\[ \text{hleg2 = legend(} \text{'Vi=10v','Vi=20v','Vi=30v'}); \]