

CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

SIMULATION

OF TEMPERATURE EFFECTS ON GaN MESFET

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By

Feng Liang

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The graduate project of Feng Liang is approved:

Prof. Benjamin F Mallard

Date

Dr. Ichiro Hashimoto

Date

Dr. Somnath Chattopadhyay, Chair

Date

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Table of Contents

Signature Page	ii
Acknowledgement	iii
List of Tables	vi
List of Figures	vii
Abstract	ix
Chapter 1: Introduction	1
1.1 The application of GaN and SiC MESFET devices	1
1.2 GaN and SiC power diodes	2
1.3 GaN and SiC optoelectronic devices	3
Chapter 2: Material Properties of GaN	6
2.1 Basic properties of GaN	6
2.2 Crystal structure	7
2.3 Defects of GaN materials	8
Chapter 3: Ion Implantation of GaN	11
3.1 Doping impurities of ion implantation	11
3.2 Defects and damage induced in the process of ion implantation	14
3.3 Problems demanding prompt solution	16
Chapter 4: Schottky Diode Physics	18
4.1 Structure and operation principle	18
4.2 Schottky barrier lowering	21
4.3 Current of Schottky diode	22
Chapter 5: MESFET Device Physics	24
5.1 Introduction	24
5.2 Charge control	26
5.3 Current-voltage characteristics	28
Chapter 6: Results of Calculation and Simulation	33

6.1 Physical model	33
6.2 Temperature-dependent physical parameters	35
6.3 Doping concentration of ion implantation	37
6.4 Results of simulation	38
Chapter 7: Conclusions	42
References	43
Appendix A: Code of Drain Current-Drain Voltage Characteristic Simulation	53
Appendix B: Code of Current-Temperature Characteristic Simulation	61
Appendix C: Code of Intrinsic Carrier Concentration-Temperature Characteristic Simulation	65
Appendix D: Code of Saturation Electron Drift Velocity-Temperature Characteristic Simulation	66

List of Tables

Table 2.1 comparison between GaN & other common semiconductor materials at the temperature of 300K	6
Table 3.1 properties of main doping impurities implanted into GaN	11
Table 3.2 donor energy of ionization for GaN of wurtzite structure	11
Table 3.3 GaN acceptors energies of ionization (meV) of wurtzite & zincblende	13
Table 6.1 nomenclature	33

List of Figures

Figure 2.1 the correlation between $1/\sqrt{2}$ of lattice constant a_{ZB} for zincblende or lattice constant a for wurtzite and band gap energy for InN, AlN, GaN and related alloys	7
Figure 2.2 Structures of atoms of ZB (a), WZ (b) and RS (rocksalt) (c)	8
Figure 2.3 the determined formation energy of the whole group of native point defects in GaN versus all charges in Fermi level	9
Figure 2.4 the related levels of transition for native point defects	10
Figure 3.1 shallow impurities formation energies of GaN	12
Figure 3.2 the vacancy profiles induced by 100keV ^{197}Au , 300keV ^{197}Au and 40keV ^{12}C ion implantation into GaN	14
Figure 3.3 profile of damage and defects in GaN induced by ion implantation of 300keV Au with $3.1 \times 10^{12}/\text{cm}^2 \cdot \text{s}$ beam flux (a) and $4.4 \times 10^{12}/\text{cm}^2 \cdot \text{s}$ beam flux (b) at LN2 and RT respectively	16
Figure 4.1 M/S diagram of energy band	18
Figure 4.2 the structure of M/S junction	18
Figure 4.3 M/S diagram of energy band before (a) and after (b) contacting	19
Figure 4.4 M/S junction diagram of energy band under the condition of thermal equilibrium	20
Figure 4.5 M/S diagram of energy band under the condition of forward (a) and reverse (b) bias	21
Figure 4.6 Schottky barrier and barrier lowering in a Schottky diode based on n -type silicon with $N_d=10^{19}\text{cm}^{-3}$ and $\phi_B=0.8\text{V}$	22
Figure 5.1 the cross-section and top view of a MESFET with channel length of $0.1\mu\text{m}$	24
Figure 5.2 tunnel density of carriers	25
Figure 5.3 structure and band diagram with applied gate bias of a MESFET	26

Figure 5.4 change of drain current and channel layer thickness of a MESFET with increasing gate bias and fixed drain-source bias	27
Figure 5.5 change of drain current and channel layer thickness of a MESFET with increasing drain-source bias and fixed gate bias	28
Figure 5.6 the structure and gate diagram of energy band in a MESFET device of GaN	29
Figure 5.7 channel layer thickness in a MESFET under different source-drain potential	30
Figure 5.8 the schematic and channel diagram of energy band in a MESFET before depletion	31
Figure 5.9 current-voltage relation of a MESFET of n-type	32
Figure 6.1 structure and related parameters of a MESFET device	33
Figure 6.2 cross-sections of a non-self aligned (a) and a self-align (b) MESFET	34
Figure 6.3 drain current-drain voltage characteristic	38
Figure 6.4 current-temperature characteristic	39
Figure 6.5 intrinsic carrier concentration-temperature characteristic	40
Figure 6.6 saturation electron drift velocity-temperature characteristic	41

ABSTRACT
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Since several years ago, semiconductor materials the band gap of which is wide, including Gallium Nitride (GaN) & Silicon Carbide (SiC), have been very promising in the applications of fabricating devices of high power, high temperature and microwave frequency as the characteristics of high breakdown voltages & low thermal generation rates. However, the performance of devices made from these materials is strongly influenced by the ambient temperature. In order to analyze the temperature effects, an analytical physical model is adopted in this paper to determine the temperature-dependent characteristics, including current-voltage characteristic, current-temperature characteristic and saturation electron drift velocity-temperature characteristic, which are also simulated through MATLAB software. Based on these characteristics, the device performance can be anticipated and device structure can be optimized.

Index terms: GaN, MESFET, temperature effects, physical model.

Chapter 1 Introduction

1.1 The application of GaN and SiC MESFET devices

Because the breakdown voltages is high and thermal rates of generation is low, some materials band gap of which is large, including Silicon Carbide (SiC) & Gallium Nitride (GaN), have been highly attractive for the related semiconductor industries in recent couple of years [1]. Based on these characteristics which are desirable for fabricating electronic devices, there is great potential for the application that the temperature and power needs to be high and microwave frequency needs to be reached [2].

For example, compared with ever-used materials, such as Gallium Arsenide (GaAs) & Silicon (Si), which can only be in dependable operation during a temperature range up to 150°C [3, 4] and 300°C [5, 6] respectively, GaN and SiC can be in coherent operation during the range of high temperature [7].

Moreover, the extensive applications in high speed integrated circuits (ICs) and microwave analog circuits are highly promising to be realized by utilizing GaN based MESFET [8-11].

Meanwhile, the utilizations of wireless base stations, which belong to the wave band of low microwave frequency, are extremely expected by applying GaN MESFET devices [2, 12-16].

In the application of military, advanced multi-functional radio frequency (RF) systems (AMRFS) are possible to be manufactured by using GaN with low life cycle cost, which will turn out to be a completely new system [17].

Based on the temperature dependent characteristics and high temperature performance of GaN and SiC devices, temperature sensors could be created by using both the materials. For example, a temperature sensor consisting of SiC FETs devices was fabricated by Jeffrey B. Casady *et al.* and could be used to indicate the temperature ranging from 25°C to 500°C [18]. A theoretical study was conducted by Sutanu Dutta to design a temperature sensor by adopting SiC MESFET [19].

According to the simulations of Monte Carlo, a saturation electron velocity of 1.3×10^7 cm/s and a maximum electron velocity of 3×10^7 cm/s are expected [20], which leads to the operation of high-frequency realized for SiC devices [21]. Compared with 4H-SiC, 6H-SiC has been approved to be the most significant in power FETs technology of high dependability among the SiC poly types because of the higher conduction band offset with SiO₂ [22].

Meanwhile, in the field of high-power radar applications, including the monitoring and control of air traffic, there is an increasingly high demand of high-power transistors instead of tubes of electrons as they are lower-cost, more dependable and faster for installation [23]. Because of the characteristics that power density and high working voltage is high, SiC MESFETs (silicon carbide metal semiconductor field effect transistors) have been approved for being such a type of transistor which meets all these needs. For example, 120W and 80W output level are demonstrated in operation of pulse and continuous wave respectively based on monolithic MESFET

devices of SiC [24]. In recent years, a maximum 60W output level is achieved in devices of production-level. The dependability of SiC MESFET devices has been confirmed to be beyond the requirements of microwave power amplifiers in the application of both military and commerce [25].

1.2 GaN and SiC power diodes

Since the availability of high breakdown voltage, quick switching speed and low onset resistance, SiC has been paid great attention in fabricating power devices. As an IV-IV group compound material of semiconductor, SiC demonstrates many excellent electrical characteristics, including dielectric breakdown voltage which is 10-time larger than silicon's [26]. Meanwhile, equipments fabricated by SiC is valid to operate in high temperature, which could be higher than 300°C, because silicon carbide's band gap is large, which is 3-time larger than silicon's.

In 1993, diode with barrier of Schottky of a 1kV breakdown voltage was fabricated based on 6H-SiC [27]. In 1995, 4H-SiC was approved to be a more excellent material used to fabricate devices of high power [28]. Since 2001, Schottky barrier diodes based on SiC have been manufactured commercially. Among the highly-required electrical characteristics of Schottky barrier diodes, the most excellent one is the fast speed of reverse recovery, which is ten times faster than the one of fast recovery diodes based on silicon. This property lowers losses of switching and increases power supply efficiency.

Because of breakdown voltage which is very high, quick speed of switching and excellent thermal characteristics [29-32], a new type of Schottky diodes based on GaN has been very promising in some applications, including power rectifier. However, the main difficulty is to design and manufacture the diode with low cut-in voltage but still maintaining high breakdown fields and low reverse leaking current. In order to achieve this, some innovative methods and technologies have developed very fast, including recess technology of Schottky junction [30, 33] and cap layers based on SiCN [34], which are adopted to reduce the onset voltage of diodes. Meanwhile, the reverse leaking current is lowered through the method of terminating Schottky junction [35, 36] and matching metals of low and high Schottky barrier [31]. Moreover, a CMOS-compatible and Au-free diode based on GaN has been achieved on a silicon wafer of 8 inches, which acquires a reverse leaking current not exceeding 1 μ A/mm at the reverse voltage of 600V. Compared with the traditional Schottky diodes fabricated on the same silicon planar, this value is several magnitude orders less. Also, through the recess technology at the anode, the onset voltage of diode is not greater than 0.5V [37].

Compared with SiC-based technology of high power electronics (HPEs), which is more developed, it is still more promising to fabricate related devices by adopting GaN since its faster electron mobility and stronger critical field [38]. In the year of 2010, the theoretically ultimate value of 4H-SiC was exceeded by Schottky diodes with high power based on GaN for the first time [39]. However, due to the challenge of film growth with low doping concentration of background, low density of damage

and defects and high quality crystals, it is difficult to obtain the result above repeatedly. With the diffusion priority of dopants to the dislocations, the breakdown field and local strain field are lowered. Meanwhile, the local electrical field is increased. Furthermore, energy gap states, as the traps of majority carriers, are induced by dislocations. In the reversely biased condition, it is easier for these traps to be ionized, which actually lowers the critical field.

To solve this problem, the factor that actually lowers the breakdown voltage needs to be determined initially. Randy P. Tompkins *et al.* conducted an experiment to investigate it. Diodes were fabricated on wafers which were of growth through the method of MOCVD. The dislocation densities of substrates are between $10^3/\text{cm}^2$ to $10^9/\text{cm}^2$. However, the breakdown voltages of these diodes were not found to be extremely different [38]. Compared with the theoretical values and those obtained from the substrates grown through the method of hydride vapor phase epitaxy (HVPE), these breakdown voltages were comparatively low [40]. Based on the research, impurities of carbon, which were deep acceptors [41], were the main reason that breakdown voltage was reduced in the films grown through the method of MOCVD [42]. Since GaCl is the source of gallium in the material grown by HVPE instead of $(\text{CH}_3)_3\text{Ga}$ in MOCVD method, the carbon concentration is lower in material of HVPE, which has been approved to be the key cause that the breakdown voltage of GaN substrates processed by HVPE is larger [38]. Therefore, through the growth method of HVPE, a vertical Schottky diode with the breakdown voltage close to 1000V and Figure of merits (FOM) around $250\text{MW}/\text{cm}^2$ could be easily fabricated on bulk GaN-based substrate grown by HVPE, getting the effect of substrate series resistance involved as well. Meanwhile, a lateral Schottky diode with the breakdown voltage greater than 700V and FOM greater than $100\text{MW}/\text{cm}^2$ could also be achieved [38].

1.3 GaN and SiC optoelectronic devices

Over the past 15 years, due to the low-cost and feasibility in fabricating wafers of large diameters which is up to 12 inches currently, it has been paid great attention for silicon to be used for epitaxial layer growing substrate of III-V semiconductor materials, including InP and GaAs [43]. However, there is still a bottleneck of fabrication since the fast degradation caused by the dislocations with a high mobility of these semiconductor materials, even through a great effort has been made. Comparatively, it has been approved that devices based on GaN can operate excellently without dislocation densities which could reach $10^{10}/\text{cm}^2$. Therefore, it has become available to integrate devices based on silicon and GaN on a single chip simultaneously. Meanwhile, some related technology of optoelectronics has been very promising as well, including displays with full color, high resolution and small size.

In 1962, Bevacqua and Holonyak created a red-light-emitting diode (LED) fabricated by the alloy of gallium arsenide phosphide (GaAsP), which is the global first LED of visible lights based on p-n junction structure of semiconductor [44]. In 1968, Logan *et al.* introduced a green-light-emitting diode (green LED) through p-n

junction of nitrogen-doped GaP [45].

However, the method and technology to develop devices emitting blue light, the energy and wavelength of which are the largest and the shortest respectively among the spectrum of visible lights, had not come out.

During the period between late 1960s and 1970s, there were some materials which were likely to be used to fabricate blue-light-emitting diode (blue LED), including zinc selenide (ZnSe) with 2.7 eV energy gap, silicon carbide (6H-SiC) with 3.0 eV energy gap and gallium nitride (GaN) with 3.4 eV energy gap [46]. At that time, SiC was the only semiconductor with wide-bandgap which might be applied to fabricate p-n junctions and it was ever adopted to create blue LEDs. However, it is invalid in the manufacture of efficient LEDs because it is not a direct-transition semiconductor.

In recent years, great attention has been paid to the optoelectronic devices fabricated by using GaN with the spectrum ranging from the whole visible lights extending to the ultra-violet (UV) rays. For example, a diode made by GaN and emitting blue, green and white light was achieved [46]. Meanwhile, the laser diode (LD) of violet/blue with high-performance is produced. These achievements make it possible to use semiconductors to create the three primary light colors. Along with red LEDs of high-brightness, there are many applications for blue LEDs and green LEDs, such as displays of entirely solid-state and full-color, signage, traffic lights and use of specialized lighting. Moreover, compared with traditional fluorescent light, white LEDs, which consist of blue/ultraviolet LEDs based on nitride, are much more efficient. Related applications include computer, cell phone and TV displays and use of general lighting, such as factories, homes and offices. In agriculture, blue LEDs are used as lighting sources. In systems of optical disc, violet LEDs based on nitride are applied for data reading/writing. More importantly, in extreme environments, these devices are still valid, saving a great amount of energy and offering a method not to use risky materials. As a result, the application of such devices will contribute a lot to prevent global warming [46].

Since the early 1990s, devices based on GaN have been increasingly attractive due to the development of the method of 3-step nucleation conducted by Akasaki *et al.* [47], making GaN growth with density of damage and defects under 10^{10}cm^{-2} available at the first time. Therefore, optoelectronic devices, such as emitting laser modules at the wavelength of 420 nm, have developed very fast based on the layer induced with high quality [48]. However, due to the density of threshold current, which was around $10\text{KA}/\text{cm}^{-2}$ [49], the device life time was not long enough. Thus, lasers which are applicable in commercial use can not be manufactured [50]. As the development of method and technology for reducing the density of damage and defects, including later epitaxial overgrowth (LEO/ELOG) [51, 52], lower density of damage and defects, which is less than 10^7cm^{-2} , have been achieved. Therefore, material of higher quality is available and laser modules of a life time beyond 10000 h and a maximum output power 100mW [53, 54].

Meanwhile, imaging of ultraviolet has been highly attractive recently in the utilizations of scientific and astronomy instrument, which induces a great demand of radiation detectors. Due to the large contrast between visible lights and ultraviolet,

high sensitivity, insignificant defects and damage induced in operation of extreme environments and dark current of quite low values, AlGaN alloys have been paid more attention as the most promising materials to fabricate photodetectors [55-57]. Through the method of changing the concentration of Al in a Schottky diodes based on Al/GaN/Ni, the photoresponse is confirmed to cover the whole spectrum range of ultraviolet between the wavelength of 200 and 360nm [58].

Another application of optoelectronic devices based on GaN is intersubband (ISB) devices. InN, AlN and GaN, which are semiconductors made by nitride of III-group, have been highly attractive recently for fabricating ISB devices used to operate in the spectrum range of near-infrared and especially in the wave band of 1.3-1.55 μ m wavelength, which is applied for the telecommunication of fiber optics [59]. There are two reasons that these semiconductor materials are very suitable for the application of ISB devices. One is that during a wide range of spectrum, these materials are transparent, for example, GaN is transparent between the wavelengths of 360nm to 13 μ m; the other is that the hetero-structures of them offer a extremely large offset of conduction band, for example, such an offset of conduction band of AlN/GaN is 1.75eV [60]. Compared with other semiconductor materials, the conduction band offset of which is large as well, such as AlSb/InAs, the energy level of remote valleys is quite high for GaN which is greater than 2eV above the Γ point [61], making it is promising for ISB devices of light-emitting to operate at the wavelengths of near-infrared.

Chapter 2 Material Properties of GaN

2.1 Basic properties of GaN

Table 2.1 shows the comparison between GaN and other common semiconductor materials at the temperature of 300K [62].

Table 2.1 comparison between GaN and other common semiconductor materials at the temperature of 300K

Material	Band gap (eV)	Mobility of electrons (cm ² /Vs)	Mobility of holes (cm ² /Vs)	Critical field (V/cm)	Thermal conductivity (W/mK)	Thermal expansion coefficient (ppm/K)
GaSb	0.726, D	3,000	1,000	50,000	32	7.75
InAs	0.354, D	44,000	500	40,000	27	4.52
InSb	0.17, D	77,000	850	1,000	18	5.37
InP	1.344, D	5,400	200	500,000	68	4.6
GaAs	1.424, D	8,500	400	400,000	55	5.73
GaN	3.44, D	900	10	3,000,000	110	5.4-7.2
Ge	0.661, I	3,900	1,900	100,000	58	5.9
Si	1.12, I	1,400	450	300,000	130	2.6
GaP	2.26, I	250	150	1,000,000	110	4.65
3C-SiC	2.36, I	300-900	10-30	1,300,000	700	2.77
6H-SiC	2.86, I	330-400	75	2,400,000	700	5.12
4H-SiC	3.25, I	700		3,180,000	700	5.12
C	5.46-5.6, I	2,200	1,800	6,000,000	1,300	0.8

Remark: D stands for direct band gap, I stands for indirect band gap, the parameters of carbon are valid for the diamond structure.

From the Table above, it can be noticed that compared with Si, the critical field of both SiC and GaN are higher, which is the characteristic that induces the availability for devices based on SiC and GaN to work at lower leaking current and higher bias voltage. Meanwhile, the electron mobility of SiC is higher than Si but lower than GaN, which implies that GaN is more promising to be the most excellent material in the application of ultimately high frequency including radio frequency since faster saturation velocity and mobility of electron are the key factors of higher frequency adoption. Furthermore, due to the higher thermal conductivity, which indicates higher efficiency of heat conduction, SiC is more potential to operate at higher power density in contrast with Si and GaN. As high power is a mainly desirable merit of devices, SiC is more excellent in the application of high power devices based on its high critical field, wide band gap and high thermal conductivity. In contrast, heat management is a difficulty for GaN-based devices due to its comparatively low thermal conductivity.

When the doping concentration is $1 \times 10^{17} \text{ cm}^{-3}$, the GaN low-field electron mobility

is $100\text{cm}^2/\text{Vs}$ approximately, which is higher than any SiC material values [63]. The breakdown field of GaN film is confirmed to approach very high values (greater than 200V) [64]. According to the Baliga high-frequency Figure of merits (BHFFOM), GaN devices loss lower power than SiC devices when operated at both low-frequency and high-frequency [65]. Meanwhile, during microwave application, the hetero-structure field effect transistors (HFETs) of AlN/GaN could reach a maximum frequency of oscillation of 35 GHz, which is more desirable than the value of 6H-SiC MESFET [66].

Another characteristic of nitride semiconductor materials is extremely high phonon energy of longitudinal-optical (LO). Meanwhile, polarizations of spontaneousness and piezoelectricity form high internal fields, which is consistent in the wurtzite structure of them [59].

2.2 Crystal structure

Due to the direct and wide band gap, which overlaps the energy spectrum ranging from infrared rays to ultraviolet rays, the semiconductor materials of III-group nitride have been very attractive and promising to the application of high-power devices and light emitting devices of short-wavelength. Figure 2.1 demonstrates the correlation between $1/\sqrt{2}$ of lattice constant a_{ZB} for zincblende or lattice constant a for wurtzite and band gap energy of InN, AlN, GaN and related alloys [67].

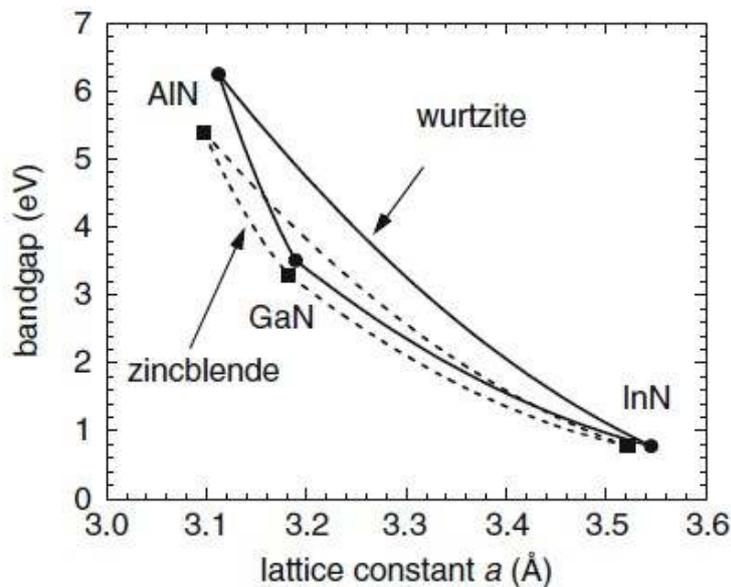


Figure 2.1 the correlation between $1/\sqrt{2}$ of lattice constant a_{ZB} for zincblende or lattice constant a for wurtzite and band gap energy for InN, AlN, GaN and related alloys

Normally, the crystal structure of GaN and other related semiconductor materials,

including AlN, InN and ZnO, is wurtzite (WZ) type of hexagon, which possesses similar tetrahedral atomic coordination of nearest-neighbor with the structure of cubic zincblende (ZB) type. The stacking sequence of WZ structure is AaBbAaBbAaBb...along the axis of [0001] and the stacking sequence of ZB structure is AaBbCcAaBbCc...along the axis of [111], where Aa, Bb, Cc represent the three types of cation and anion location in the lattice of triangle on the planes of (0001) and (111), which are demonstrated by Figure 2.2 [68].

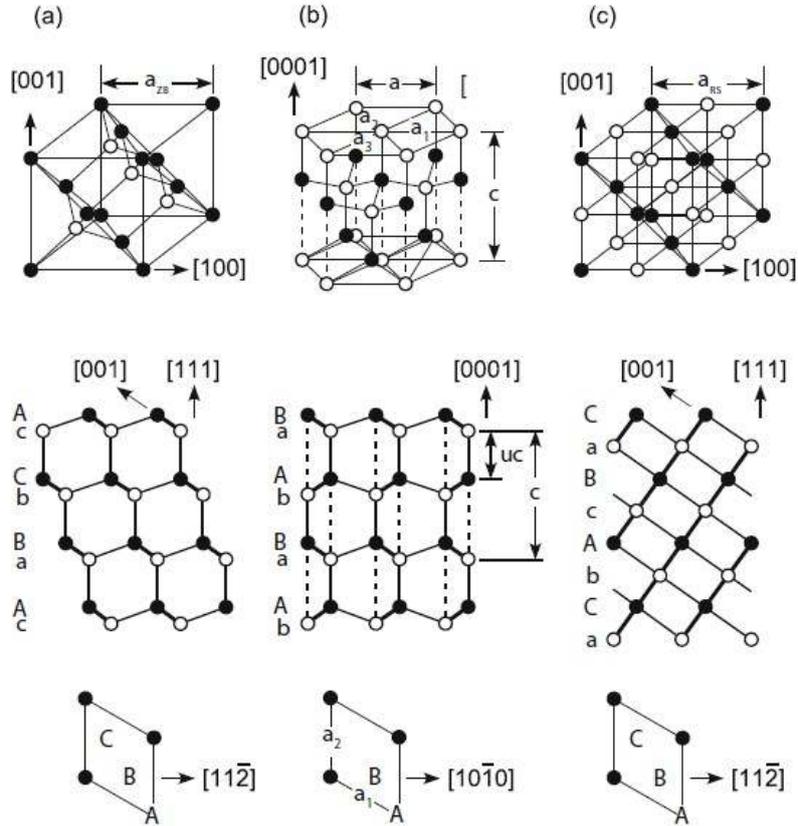


Figure 2.2 Structures of atoms for ZB (a), WZ (b) and RS (rocksalt) (c)

If stacking sequence is the only factor that differentiates structures types of WZ and ZB, the relation below,

$$c/a = \sqrt{8/3} = 1.633,$$

will exist between WZ structure lattice constants, a and c . Meanwhile, there is another equation, $u=3/8=0.375$, where u is the internal parameter and uc matches the bond length which is parallel to the axis of [0001].

2.3 Defects of GaN materials

Due to the mismatching and dislocation of stacking and lattice with substrates mainly, nitrides materials, including AlN, InN and GaN, demonstrate a large amount of defects and damages of structure and point, which significantly influence host materials on optical and electrical characteristics [69]. Moreover, device dependability

and performance based on related nitride materials can be extremely degraded by these damage and defects. Although the problem of dislocations of high density hasn't effect devices on obtaining desirable performance anymore, there is still another challenge to increase the emitter efficiency and operation lifetime of laser modules and promote the performance of electronic devices, which the existence of point defects, including unintentionally and intentionally-doped impurities, local isolated defects (antisites, interstitial and vacancies) and different isolated defect combinations.

As always being existent in semiconductor materials, native defects effectively influence the optical and electrical characteristics on host materials [69]. Normally, native defects are induced by impurities doping and act as the sources of compensation. Meanwhile, annealing and growth of nonstoichiometry can also induce native defects. In Figure 2.3, the determined formation energy of the whole group of native point defects in GaN versus all charges in Fermi level is shown while related levels of transition are shown in Figure 2.4 for native point defects [70]. In Figure 2.3, the slopes of different lines stand for corresponding defect charges and the valence band top is reflected by the zero position of Fermi level, only showing the segment which offers the lowest overall energy for every state of charge. Meanwhile, it is assumed that the condition of Ga-rich is present. In Figure 2.4, the defect energy levels are represented by slope differences which are able to be experimentally tested.

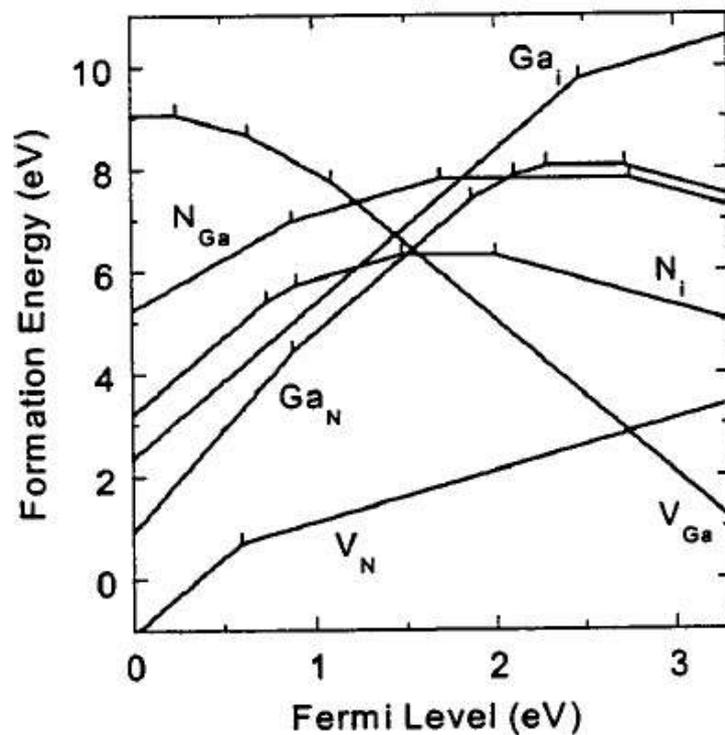


Figure 2.3 the determined formation energy of the whole group of native point defects in GaN versus all charges in Fermi level

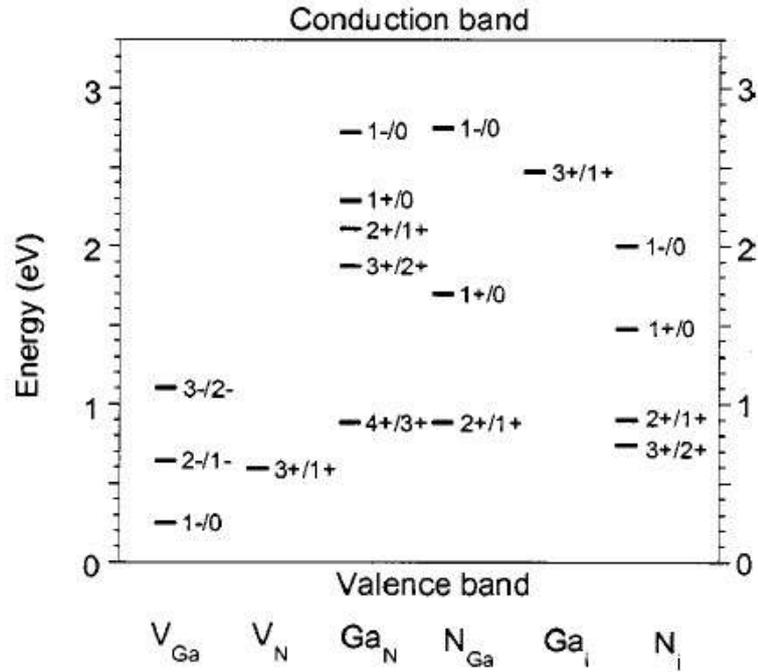


Figure 2.4 related levels of transition for native point defects

From Figure 2.3, it can be noticed that high energy of formation exists in antisite and interstitial defects, which means normally they can not be formed in GaN during the process of growth. Meanwhile, it can be aware that high density of defects with high energy of formation may be induced through the process of ion implantation and electron irradiation [69].

Chapter 3 Ion Implantation of GaN

Since more than thirty years ago, the method of ion implantation has been an extremely attractive and effective way in many applications, including ion cutting, electrical isolation, dry etching, doping of selective area, etc., of GaN-based devices fabrication [71].

3.1 Doping impurities of ion implantation

Normally, the shallow donors of GaN include Ge, Si and C occupying the site of Ga and Se, S and O occupying the site of N while the shallow acceptors of GaN include Ca, Mg, Zn, Cd and Be occupying the site of Ga and Ge, Si and C occupying the site of N. The properties of main doping impurities implanted into GaN are shown in Table 3.1 [71]. Through the method of effective mass, formation energy, which indicates the defect that is more likely to form, and energy level, which can be used to determine ionization energy more accurately, can be obtained.

Table 3.1 properties of main doping impurities implanted into GaN

	Max available doping concentration (cm ⁻³)	Coefficient of diffusion (cm ² /s)	Ionization energy (meV)
Donors			
Si	5×10 ²⁰	<2×10 ⁻¹³ (1500°C)	28
S	5×10 ¹⁸	<2×10 ⁻¹³ (1400°C)	48
Se	2×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	-
Te	1×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	50
O	3×10 ¹⁸	<2×10 ⁻¹³ (1200°C)	30
Acceptors			
Mg	~5×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	170
Ca	~5×10 ¹⁸	<2×10 ⁻¹³ (1450°C)	165
Be	<5×10 ¹⁷	Defect-assisted	-
C	n-type	<2×10 ⁻¹³ (1400°C)	-

a. Shallow donors

Based on the approximation method of effective mass, energy levels are determined for the substitution shallow donors of GaN and related ionization energies of donors are obtained for GaN of wurtzite structure, which are demonstrated by Table 3.2 [72].

Table 3.2 ionization energies for GaN of wurtzite structure (donors)

Ga site (meV)			N site (meV)		
C	Si	Ge	O	S	Se
34.0	30.8	31.1	32.4	29.5	29.5

According to the calculation of first principles, among the substitution impurities in GaN of wurtzite structure, including Ge, Si, C, it has been noted that the energy of

formation for the donors of Ge_{Ga} and Si_{Ga} is relatively low, which is 2.3eV and 0.9eV in Ca-rich situation respectively, and the donor of C_{Ga} is unlikely to form [73]. Through the estimation in different kinds of theoretical researches, the formation energy is approximately between 5.7eV and 6.5eV in Ga-rich situation and between 4.0eV and 4.7eV in N-rich situation for neutral C_{Ga} [73-75]. Meanwhile, low formation energy has been acquired for the donors of Si_{Ga} and O_{N} , which is lower than 2eV for both in Ga-rich situation [76, 77]. In Figure 3.1 [75, 78, 79], it can be found that the formation energy descends linearly for the shallow donors as Fermi level decreases. Therefore, it can be aware that the substitution shallow donors are much easier to establish among GaN of p-type and high-resistivity if the impurities are induced in the process of growth [69].

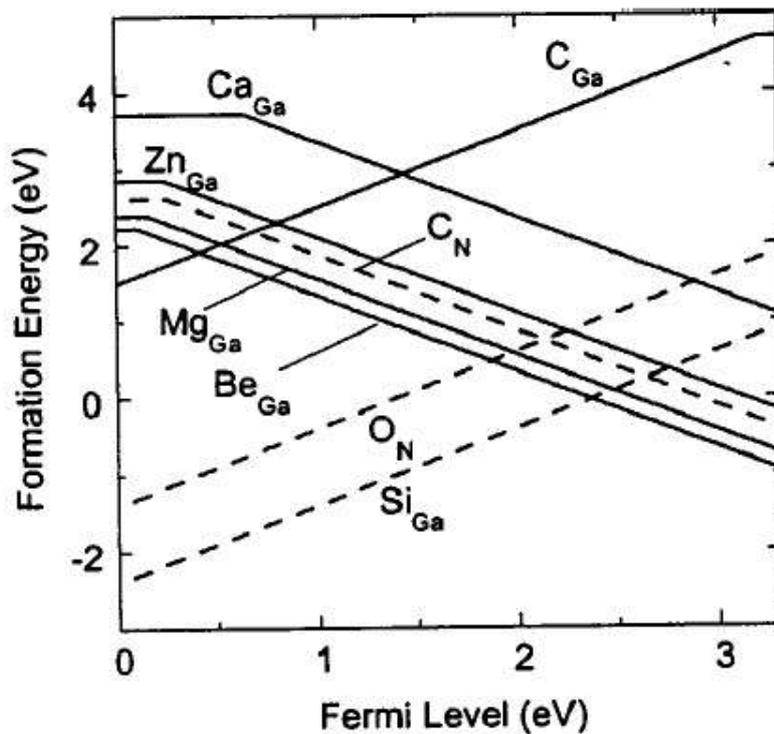


Figure 3.1 shallow impurities formation energies of GaN [75, 78, 79].

b. Substitution acceptors

Through the approximation method of effective mass, ionization energy has been determined for major substitution acceptors in CaN of wurtzite and zincblende structure, which is demonstrated by Table 3.3 [80, 81].

Table 3.3 GaN acceptors energies of ionization (meV) of wurtzite & zinblende

Acceptor	E_A (WZ)	E_A (WZ)	E_A (ZB)	E_A (ZB)
	[81]	[80]	[81]	[80]
Be_{Ga}	187	204	183	133
Mg_{Ga}	224	215	220	139
Ca_{Ga}	302	259	297	162
Zn_{Ga}	364	331	357	178
Cd_{Ga}	625		620	
C_{N}	152	230	143	147
Si_{N}	224	203	220	132
Ge_{N}	281		276	

According to Table 3.3, Be_{Ga} , Mg_{Ga} , C_{N} , Si_{N} are the most potential impurities for being shallow acceptors since the ionization energies of them are lower than other acceptor materials. Even more, the ionization energy of Be_{Ga} is considered as the lowest one in the potential acceptors by Pödör [82]. Through same method with the analysis of the negative charges between Ga atom and acceptor atoms, other acceptors which substitute Ga atom can be arranged as the sequence of decreasing ionization energy, which are Cd, Zn and Mg [82]. Based on the calculation of first principles and through the investigation of electronic and atomic structures of substitution acceptors in GaN, including C, Mg and Be, Park and Chadi argued that states of effective mass would be induced instead of AX states by the acceptors above [83]. In Figure 3.1, some determined formation energies of the previously-mentioned impurities can be found, among which Be_{Ga} and Mg_{Ga} possess the smallest ionization and formation energy. However, there is a challenge for adopting Be as the substitution acceptor impurity, which is that Be may become a donor in interstitial site due to its tiny atom size [78, 84-86]. Based on it, the most potential doping materials from group II are Be and Mg for GaN to form a *p*-type semiconductor while the doping materials from group IV, including Ge_{N} and Si_{N} , are difficult to be ionized in GaN under the condition of equilibrium due to their comparatively high formation energy [73, 78]. For C_{N} , it is not considered as an excellent acceptor even though it is possible to be easily ionized in Ga-rich case since the compensation of interstitial C could be present for C_{N} , which is desired to be an acceptor, under the condition of close Fermi level to conduction band [87]. However, Si_{N} and C_{N} could act as acceptors for *n*-type and intrinsic GaN in the process of growth since the acceptor formation energy of them decreases as the Fermi level increases, which is shown in Figure 3.1.

Moreover, acceptor dopants among I-group, including Li_{Ga} , Na_{Ga} and K_{Ga} , are not considered as potential *p*-type impurities for doping due to their comparatively high ionization and formation energy. Instead, Li and Na could be donors since their interstitials energies of formation are smaller under the condition of *p*-type GaN semiconductor [78].

3.2 Defects and damage induced in the process of ion implantation

In the process of ion implantation, defects and damage which are the principle factors that influence the effects of both optical and electrical doping are always induced, including lattice disorder. Meanwhile, the quality of dry-etching is affected as well by the defects and damage in layers of near-surface caused by ion implantation. Therefore, in order to promote the device quality, it is very significant to reduce the defects and damage produced in ion implantation.

3.2.1 Lattice disorder and atomic dislocation

Based on the research of solid-ion interactions [88], it has been approved that every ion with high enough energy to penetrate through the crystal of GaN induces the interstitials of Ga, N (G_{ai} , N_i) and sublattice vacancies of Ga, N (V_{Ga} , V_N) [89]. It is possible to form a space of disorder if the damage level reaches some limits [90-92].

Through the computer program of Monte Carlo simulation, TRIM code [93], atomic dislocations and ion ranges induced by ion implantation are determined. In Figure 3.2, the vacancy profiles induced by 100keV ^{197}Au , 300keV ^{197}Au and 40keV ^{12}C ion implantation into GaN are shown [71]. Based on Figure 3.2, it is aware that a profile distribution of atomic dislocation similar with Gaussian distribution is induced by ion implantation. Meanwhile, it is found that the number of atomic dislocation and layer thickness created by ion implantation are related to the energy and mass of ions.

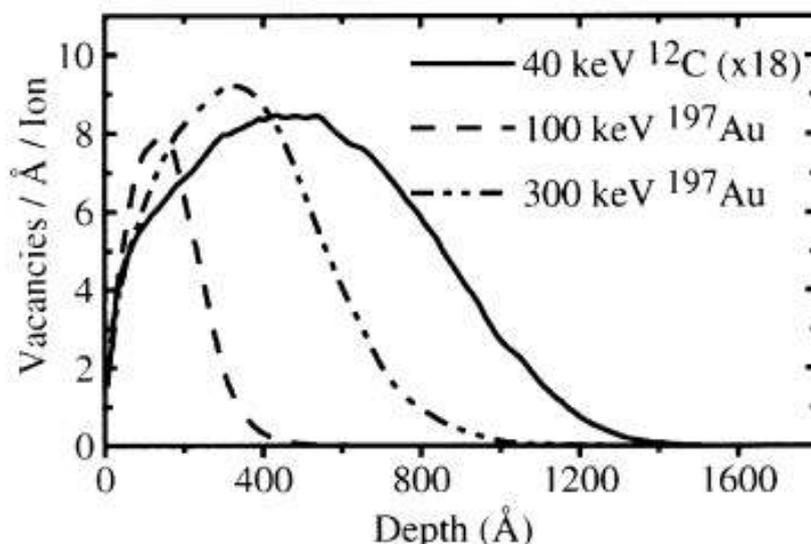


Figure 3.2 the vacancy profiles induced by 100keV ^{197}Au , 300keV ^{197}Au and 40keV ^{12}C ion implantation into GaN

3.2.2 Annealing of dynamics

Since the start research of accumulated defects under the condition of GaN, it has been considered that highly sufficient dynamic annealing is demonstrated in GaN in the process of ion implantation by Si with the ion energy of 90keV at the temperature of liquid nitrogen, which is also known as LN2 [94, 95]. This is based on the

phenomenon that the number of lattice disorder obtained in experiments is sufficiently less than the one determined through the method of ballistic analysis and calculation, including TRIM code, where the process of collision is involved while the annihilation and diffusion of damage and defects are neglected.

Firstly, as ion dose increases, undesired damage and defects are induced through GaN dynamic annealing to a certain extent. In Figure 3.3(a) and 3.3(b), it is shown that in GaN, the profiles of damage and defects accumulation with increasing ion dose, analyzed through RBS/C spectra, produced by ion implantation with Au of 300keV ion energy and $3.1 \times 10^{12}/\text{cm}^2 \cdot \text{s}$ beam flux at liquid nitrogen temperature (LN_2) and Au of 300keV ion energy and $4.4 \times 10^{12}/\text{cm}^2 \cdot \text{s}$ beam flux at room temperature (RT) respectively [71]. From these two Figures, large differences of damage and defects can be found as ion dose increases in implantation at LN_2 and RT. At LN_2 , most of the damage and defects accumulate at the surface of GaN for ion dose not beyond $2 \times 10^{14}/\text{cm}^2$. Meanwhile, the damage and defects in the bulk area of GaN, which is around 500Å away the surface, increase extremely fast between ion dose of $2 \times 10^{14}/\text{cm}^2$ and $3 \times 10^{14}/\text{cm}^2$. Even more, through the method of XTEM, it has been approved that amorphization is present when ion dose reaches a high level [96]. Compared with LN_2 , damage and defects in GaN increase at a slower speed in the bulk area as ion dose increases. In fact, damage and defects in bulk GaN reach a saturation level which is not beyond the level of random and amorphization is formed gradually from the surface of GaN.

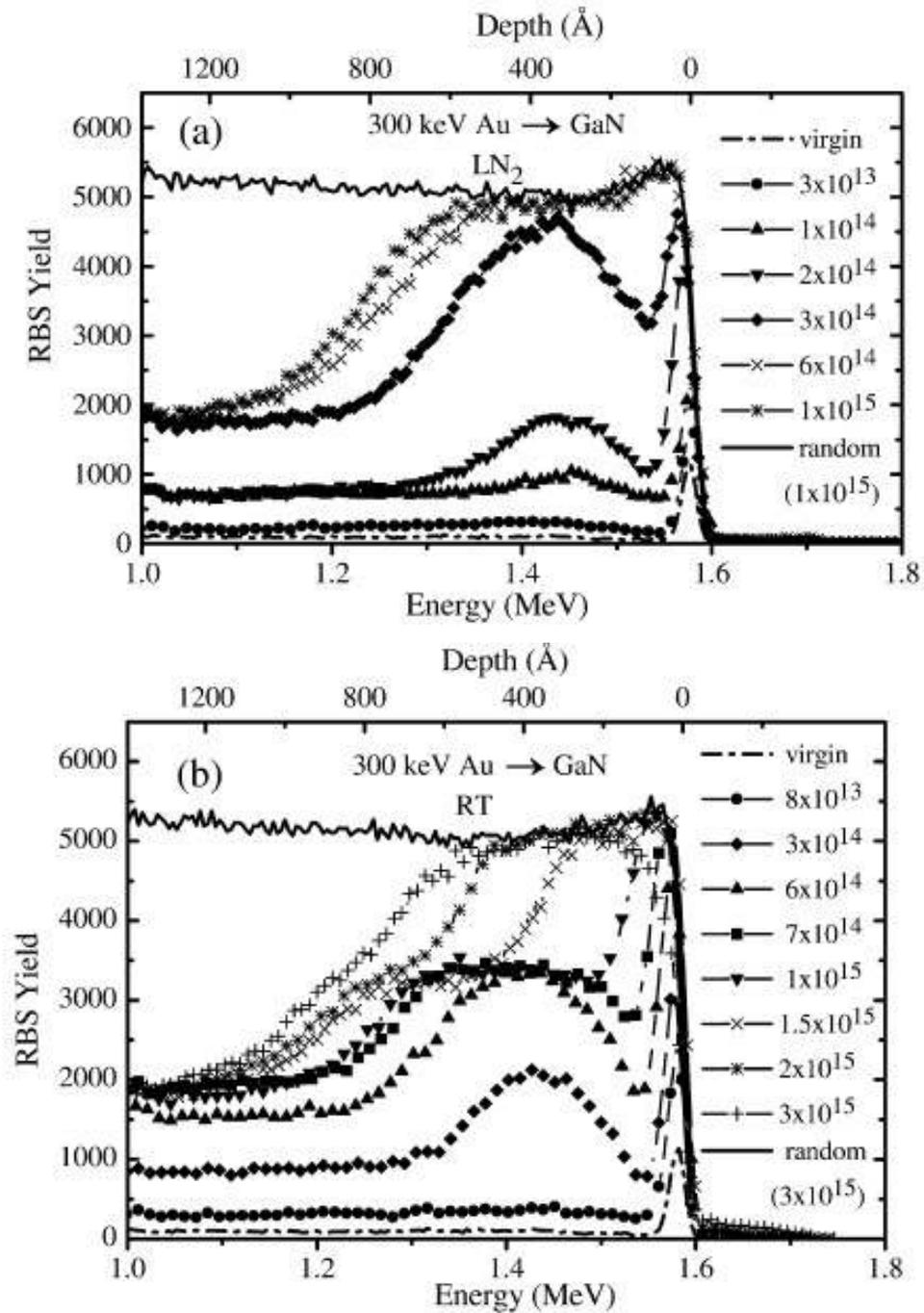


Figure 3.3 profile of damage and defects in GaN induced by ion implantation of 300keV Au with $3.1 \times 10^{12}/\text{cm}^2 \cdot \text{s}$ beam flux (a) and $4.4 \times 10^{12}/\text{cm}^2 \cdot \text{s}$ beam flux (b) at LN₂ and RT respectively. Ion dose is represented in unit of cm^{-2} .

3.3 Problems demanding prompt solution

In order to obtain a device fabricated by GaN with satisfactory performance, many problems related to disorder created through ion implantation need to be solved. Among these problems, lattice disorder induced in the process of implantation is the major one that influences ion implantation on the application of dry etching and

doping. Compared with GaAs and Si, only extremely high level of ion dose may produce amorphization in GaN bulk because of highly sufficient dynamic annealing present in GaN. Therefore, disorder induced through ion implantation is unlikely to form in GaN theoretically. However, a certain amount of defects and disorders are established in GaN through ion implantation based on defects and electrical/optical properties experimentally measured in GaN through the process of ion implantation [71]. Moreover, because of the presence of recombination centers formed by lattice disorder, even ion implantation with comparatively low level of ion dose may have effects on GaN. Therefore, annealing need to be used for recovering the damage and defects induced by ion bombardment after ion implantation even with a very level of ion dose.

However, it is a challenge to process annealing of defects and disorder induced by ion implantation in GaN. In order to entirely recover the defects created through ion implantation with quite low level of ion dose, which is between 10^{11}cm^{-2} and 10^{12}cm^{-2} for C with 150keV ion energy, 1100°C of temperature is still not high enough for annealing. Meanwhile, due to GaN decomposition and requirement of surface capping layer, it is complex to process annealing of higher temperatures.

In the applications of Ohmic contact and *p*-type doping, ion implantation of high level of ion dose is required while it is much harder to recover the defects induced by ion implantation. It is aware that extensive disorder and defects are created through ion implantation of high level of ion dose in the layer of implantation. Meanwhile, the recovery of extensive disorder and defects requires annealing at extremely high temperature, which is approximately two thirds of melting point. For GaN, the temperature is around 1650°C [71].

Chapter 4 Schottky Diode Physics

4.1 Structure and operation principle

The structure of Schottky diode is based on metal-semiconductor junction, which is significant in the applications of many related semiconductor devices. If M/S (metal/semiconductor) contact is formed, electrons in these two materials will migrate from one to another. However, the metal will obtain more electrons migrating from the semiconductor due to lower electron potential in the semiconductor, demonstrated by Figure 4.1 [97], which results a metal the charge of which is negative and a semiconductor the charge of which is positive under the condition of thermal equilibrium. Therefore, a bipolar layer similar with p-n junction is formed.

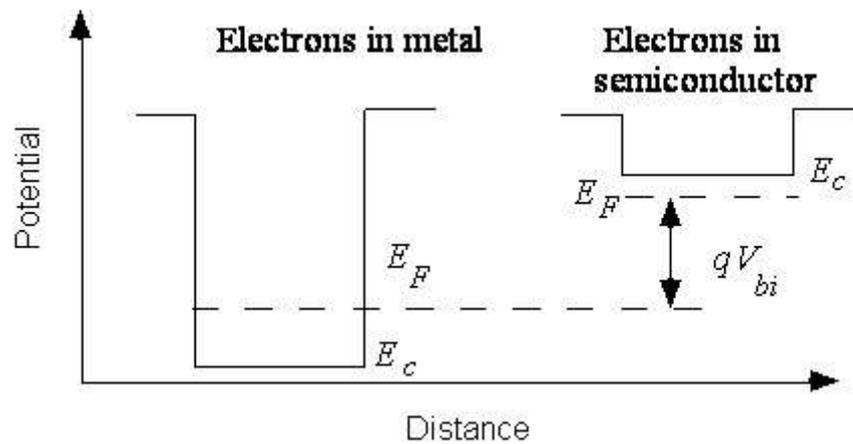


Figure 4.1 M/S diagram of energy band

4.1.1 Structure

Figure 4.2 demonstrates that structure of metal-semiconductor junction is mainly a M/S contact [97]. Meanwhile, an Ohmic contact is fabricated at the other end of the semiconductor.

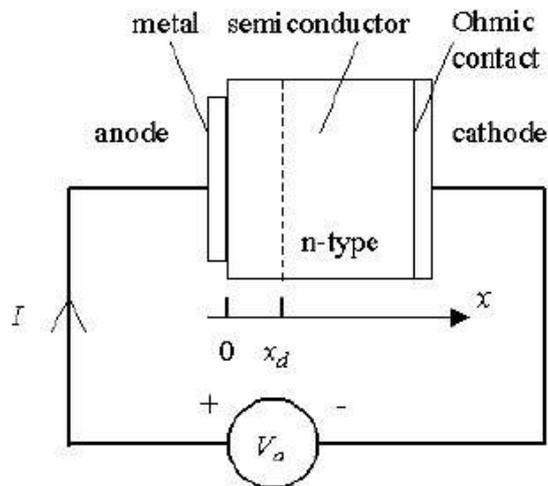


Figure 4.2 structure of metal-semiconductor junction

4.1.2 Energy diagram of flat band and built-in potential

Through energy diagram, the barrier between the semiconductor and the metal could be determined. The energy diagram is established by aligning the M/S diagrams of energy band based upon the same level of vacuum, which is indicated in Figure 4.3(a) [97]. Due to the contact between the metal and semiconductor, Fermi level can't change instantly, which obtains the energy diagram of flat band indicated by Figure 4.3(b) [97].

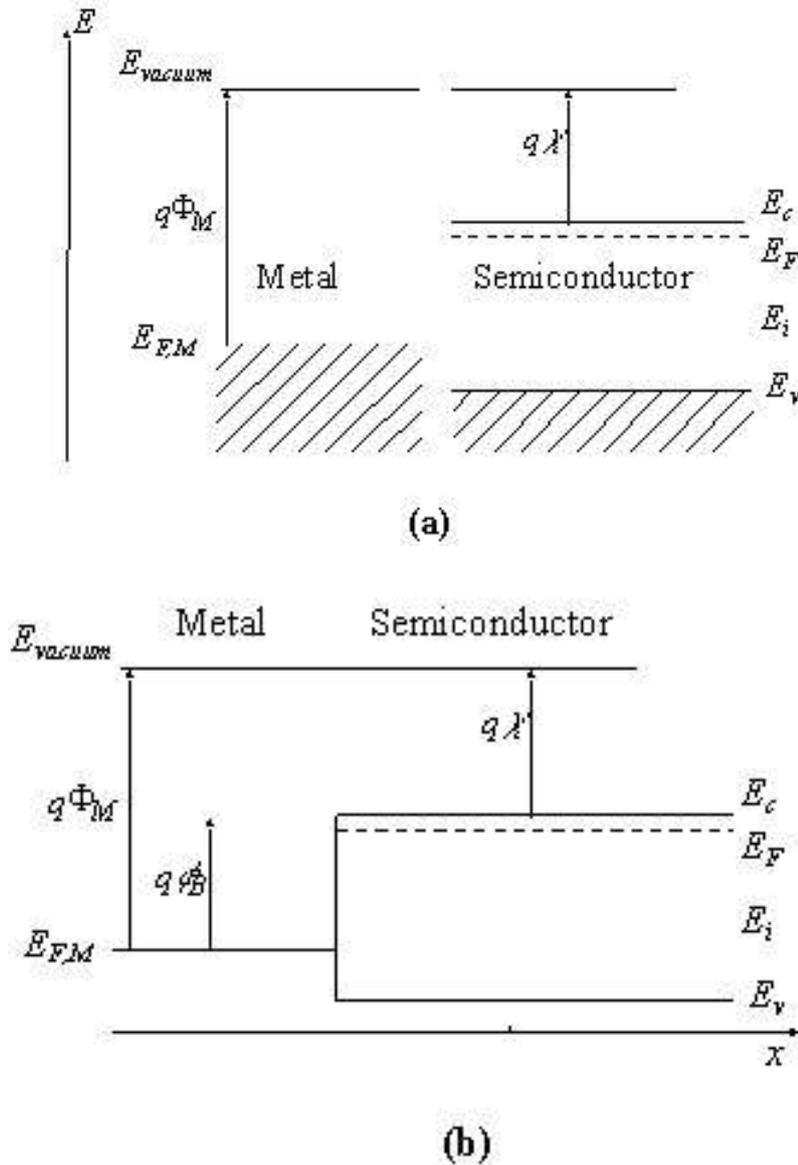


Figure 4.3 M/S diagram of energy band before (a) and after (b) contacting [97]

The barrier height, ϕ_B , can be determined through the following equations:

$$\phi_B = \Phi_M - \chi, \text{ valid for n-type semiconductors, and} \quad (4.1)$$

$$\phi_B = \frac{E_g}{q} + \chi - \Phi_M, \text{ valid for p-type semiconductors,} \quad (4.2)$$

The M/S difference of Fermi level is defined by built-in potential, ϕ_I , which can be determined through the following equations:

$$\phi_I = \Phi_M - \chi - \frac{E_C - E_{Fn}}{q}, \text{ valid for n-type semiconductors, and} \quad (4.3)$$

$$\phi_I = \chi + \frac{E_C - E_{Fp}}{q} - \Phi_M, \text{ valid for p-type semiconductors.} \quad (4.4)$$

4.1.3 Thermal equilibrium

Because of the M/S difference of Fermi level, which is demonstrated by Figure 4.3(b), the energy diagram of flat band is not under the condition of thermal equilibrium. When an electron migrates in the direction of S→M, a charge which is positive is created through the donor atom which is ionized. Therefore, a negative field is induced, which creates electron transport in the direction of M→S, and the energy band of the semiconductor is lowered. Then, electrons keep migrating in the direction of S→M unless equilibrium is established between the electron transport in the direction of S→M and in the direction of M→S. The flat Fermi level through the M/S junction indicates the equilibrium is established, which is demonstrated by Figure 4.4 [97].

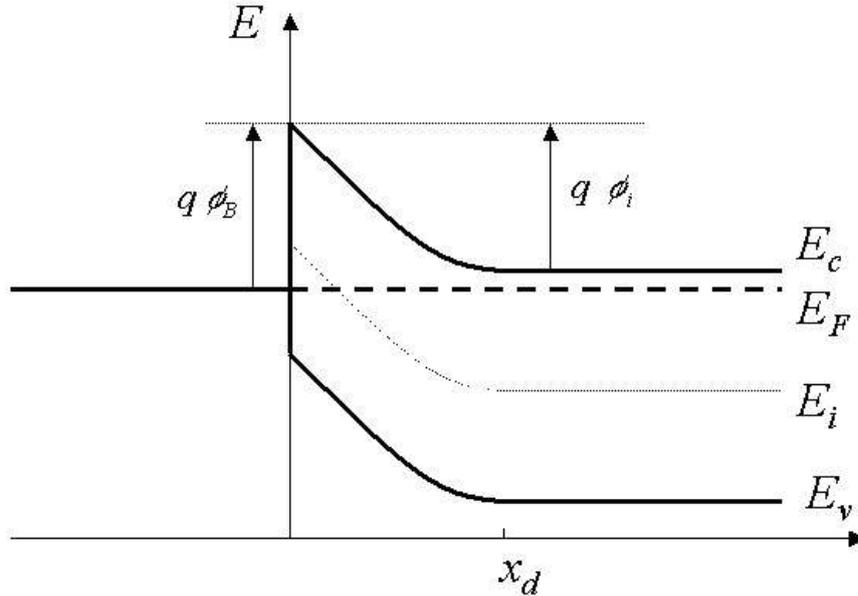


Figure 4.4 M/S junction diagram of energy band under the condition of thermal equilibrium

4.1.4 Forward and reverse bias

With an applied positive bias, the Fermi level of M is lower than the one of S, which lowers the potential drop across the semiconductor. Therefore, the thermal equilibrium doesn't exist any more and diffusion electrons towards the metal are more than drifting electrons towards the semiconductor. Then, a positive current is formed when the voltage is applied to be at least equal to the built-in potential, which is

demonstrated by Figure 4.5(a) [97].

With an applied negative bias, the Fermi level of M is high compared to the one of S, which increases potential drop across S. Due to the constant barrier that prevents electrons migrating to the metal, the electron transport is controlled by the barrier regardless of bias, demonstrated by Figure 4.5(b) [97].

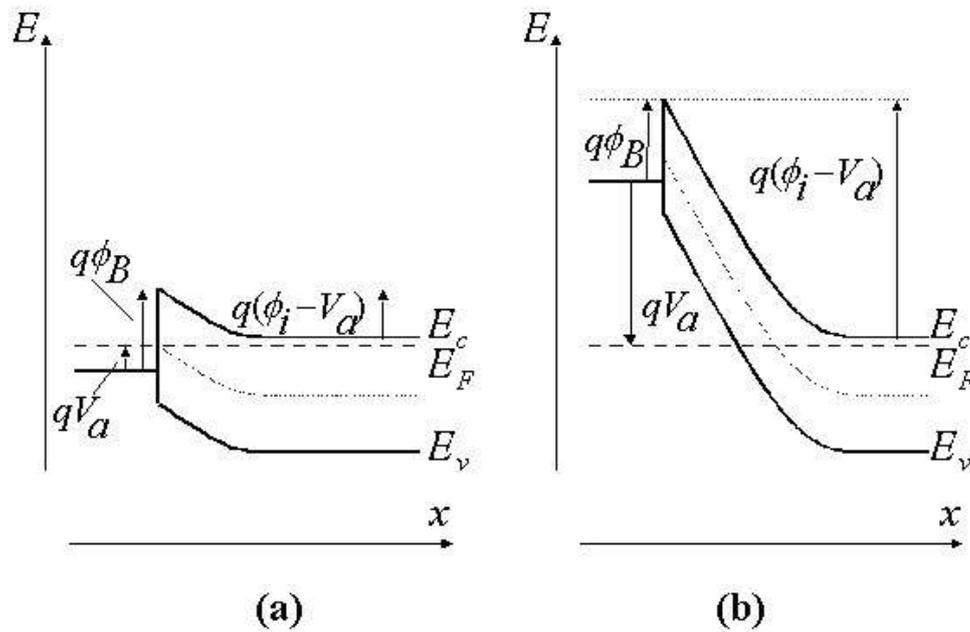


Figure 4.5 M/S diagram of energy band under the condition of forward (a) and reverse (b) bias

4.2 Schottky barrier lowering

When carriers accumulate at the interface of metal-semiconductor, image charges are created at the metal side of an M/S contact, which lowers the effective height of barrier. Compared with the original one, its lowering is quite small. However, the barrier lowering is significant because it is influenced by the applied bias and produces effects of applied bias on reverse bias current. Meanwhile, it is aware that through the measurement of capacitance-voltage, the Schottky barrier lowering can't be found since it only exists while carriers accumulate at the interface of metal-semiconductor [98].

In Figure 4.6, the Schottky barrier and barrier lowering are demonstrated based on n -type silicon Schottky barrier diode [98].

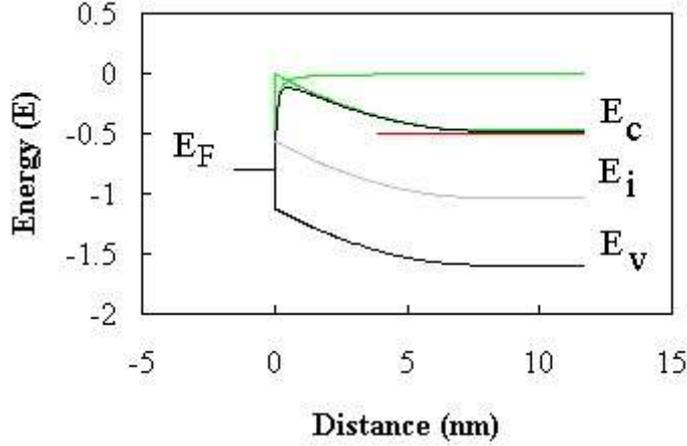


Figure 4.6 the Schottky barrier and barrier lowering in a Schottky diode based on n -type silicon with $N_d=10^{19}\text{cm}^{-3}$ and $\phi_B=0.8\text{V}$

4.3 Current of Schottky diode

The S-diode current is primarily produced by majority carriers through three completely different mechanisms, which are diffusion, thermionic emission and quantum-mechanical tunneling.

4.3.1 Diffusion

With the approximation of large width of depletion layer (compared with the length of diffusion), the density of diffusion current is determined through following equation:

$$J_n = \frac{q^2 D_n N_C}{V_t} \sqrt{\frac{2q(\phi_i - V_a)N_d}{\epsilon_s}} \exp\left(-\frac{\phi_B}{V_t}\right) \left[\exp\left(\frac{V_a}{V_t}\right) - 1 \right]. \quad (4.5)$$

4.3.2 Thermionic emission

Based on the assumption that electrons with energy higher than the barrier height will migrate over the barrier, the thermionic emission current density can be determined through the following equation:

$$J_n = A^* T^2 \exp\left(-\frac{\phi_B}{V_t}\right) \left[\exp\left(\frac{V_a}{V_t}\right) - 1 \right], \quad (4.6)$$

where $A^* = \frac{4\pi q m^* k^2}{h^3}$ is the Richardson constant.

4.3.3 Quantum-mechanical tunneling

The quantum-mechanical tunneling current density can be determined through the following equation:

$$J_n = q v_R n \Theta, \quad (4.7)$$

where $v_R = \sqrt{\frac{kT}{2\pi m}}$ is the Richardson velocity, n is the concentration of available electrons and $\Theta = \exp\left(-\frac{4}{3} \frac{\sqrt{2qm^*}}{\hbar} \frac{\phi_B^{3/2}}{E}\right)$ is the tunneling probability where $E = \phi_B / L$ is the electrical field.

Chapter 5 MESFET Device Physics

5.1 Introduction

MESFET is a kind of device among which current is formed through major carriers. The cross-section and top view of a MESFET with channel length of $0.1\mu\text{m}$ are demonstrated in Figure 5.1 [99].

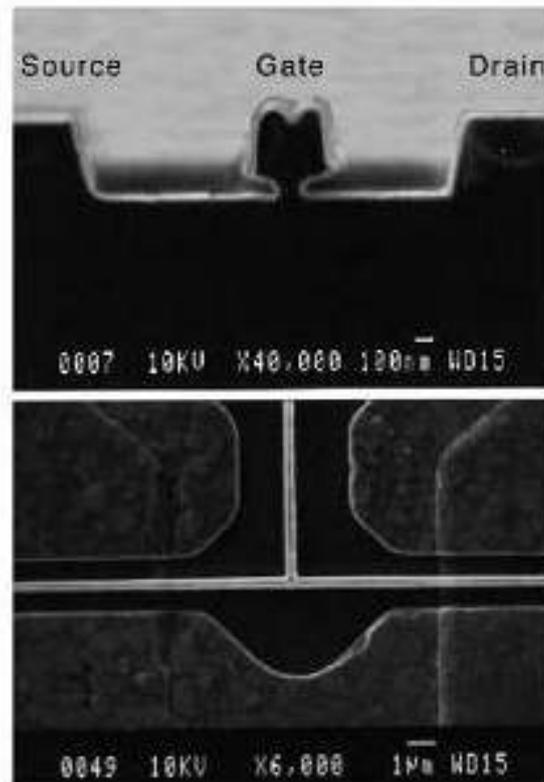


Figure 5.1 cross-section & top view of a MESFET with channel length of $0.1\mu\text{m}$

In MESFET, an active layer behaves as a tunnel where electrons (n -type MESFET) or holes (p -type MESFET) migrate from s -terminal to the d -terminal, where Ohmic contacts are used. Through the gate potential, the channel current is dominated, which leads to the charge density control of the tunnel, which is demonstrated in Figure 5.2 [90].

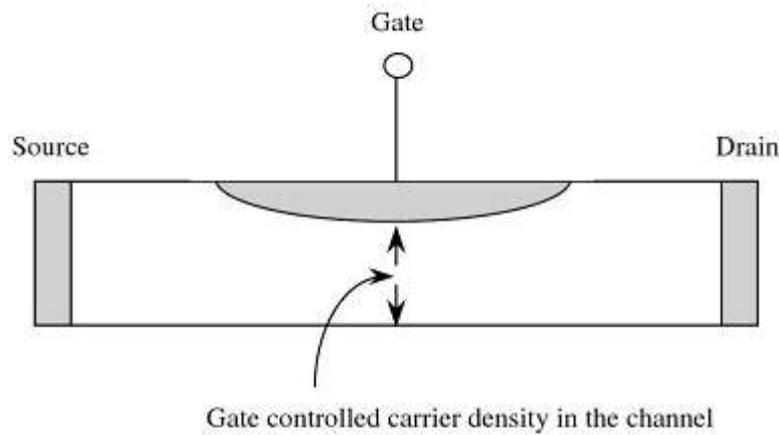


Figure 5.2 tunnel density of carriers

It has been aware that it is extremely significant for gate isolation from the channel to prevent current leaking to the gate. According to the different methods of processing the gate isolation, FET devices are divided into different types. With gate isolation induced by an oxide layer, metal-oxide-semiconductor FETs (MOSFETs) are fabricated, which is the fundamental of silicon-based devices. With gate isolation produced, MESFETs are fabricated. In Schottky barrier, the flowing current is tiny under applied gate potentials, which realizes the gate isolation. With gate isolation created by a reversely-biased p-n junction, junction-FETs (JFETs) are fabricated. With gate isolation realized by semiconductor with large band gap, which is different from the substrate material, hetero-junction FETs (HFETs) and modulation doped FETs (MODFETs) are fabricated.

Compared with the MOSFET, the carrier mobility flowing through the channel is higher. This is because in a MOSFET, the electrons or holes flowing in the inversion layer possess a wave function, extending into the layer of oxide. Therefore, the mobility of carriers in MOSFET is considered as the surface mobility which is lower than half of the bulk material mobility. In MESFET, due to the depletion region induced by the Schottky barrier which prevents the contact of the electrons or holes with the surface, the carrier mobility almost reaches the bulk material mobility. Because of the higher mobility, MESFET devices demonstrate a performance of larger current, higher transit frequency and transconductance.

However, the gate structure of Schottky barrier in a MESFET creates a limit value for the forward-biased gate voltage. Therefore, threshold voltage of a MESFET can't exceed it, resulting in a difficulty in fabricating a circuit consisting of many MESFET of enhancement type. Owing to the property of high frequency of transit, the disadvantage of threshold control caused by Schottky barrier can be neglected to a large extent. The reason is that depletion-mode MESFET devices are usually applied to microwave circuits and amplifiers based on the high transit frequency of MESFET devices. Meanwhile, the circuits consisting of depletion-mode devices need much less transistors than the circuits consisting of enhancement-mode devices. Therefore, the problem of threshold control can be easily solved.

5.2 Charge control

A typical MESFET device is fabricated on a substrate with low level of conductivity, which is demonstrated by Figure 5.3(a) [99]. The gate is formed through an S-barrier while the drain and source are both contacts of Ohmic. When there is no potential applied to the gate, partial depletion is present in the channel, which is demonstrated by Figure 5.3(b) [99]. Depletion area width will be changed with an applied negative gate bias through which the gate metal-semiconductor junction is reversely-biased for an n -type MESFET. Therefore, the conductivity of the device can be modulated through the gate. Full depletion of the channel is demonstrated by Figure 5.3(c) [99].

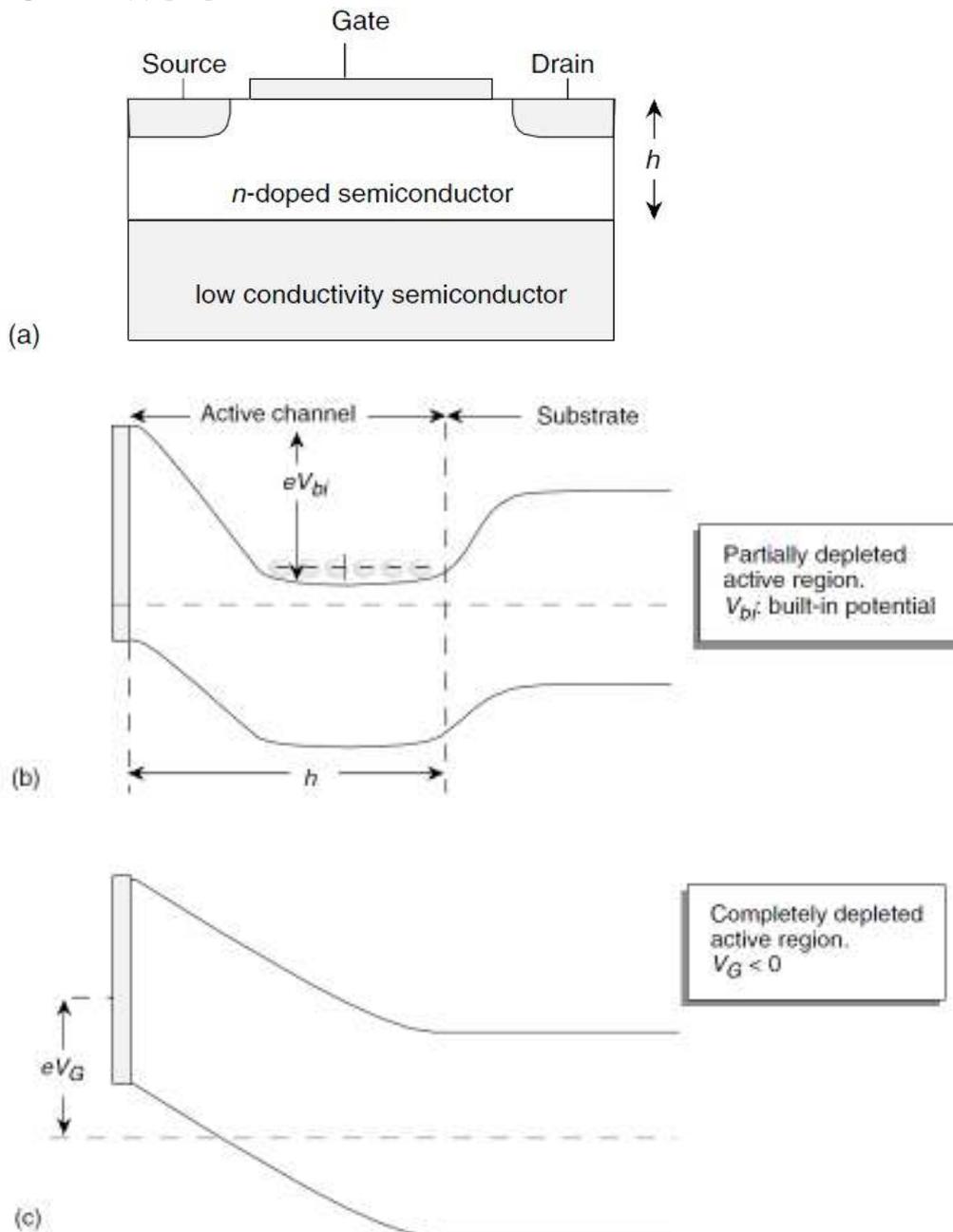


Figure 5.3 structure and band diagram with applied gate bias of a MESFET

A depletion-mode MESFET, which possesses a conducting channel when gate potential is zero, is demonstrated by Figure 5.4 [99]. Through Figure 5.4(a), a bias is applied between s-terminal and d-terminal while gate potential is zero. With the gate bias increases, the Schottky barrier is reversely-biased and depletion area width is larger. Therefore, the current flowing through active channel is smaller, which is demonstrated by Figure 5.4(b), and will be finally “pinched off” with the continuing increase of the gate bias, which is demonstrated by Figure 5.4(c).

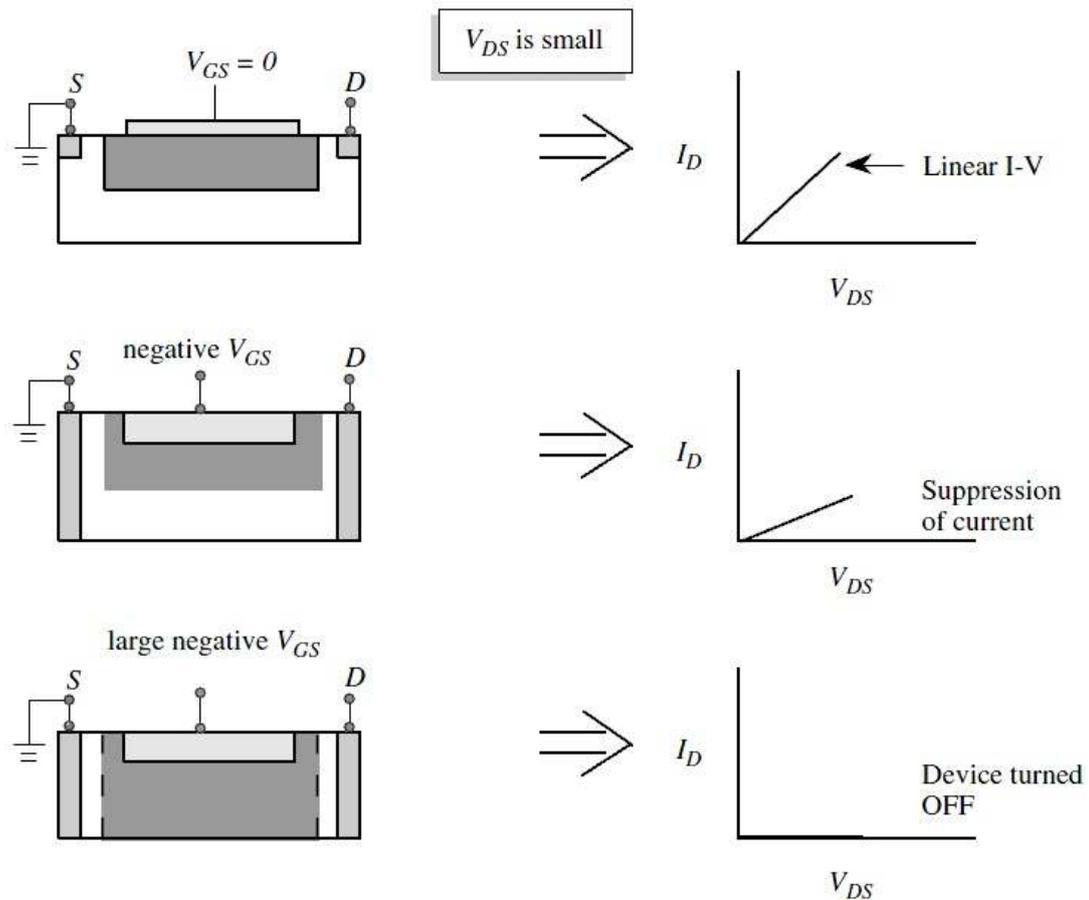


Figure 5.4 change of drain current & channel layer thickness of a MESFET with increasing gate bias and fixed drain-source bias

When a constant and unchanged gate potential is applied, drain side of the Schottky barrier in a MESFET will be more reversely-biased than the source side since the drain potential is larger. Therefore, width of depletion area will be larger at the drain side and finally the channel where the current flows is pinched off at d-terminal. Under the condition, current in the active channel will not increase even though the drain bias increases, which is known as the saturation current. This process is illustrated below [99].

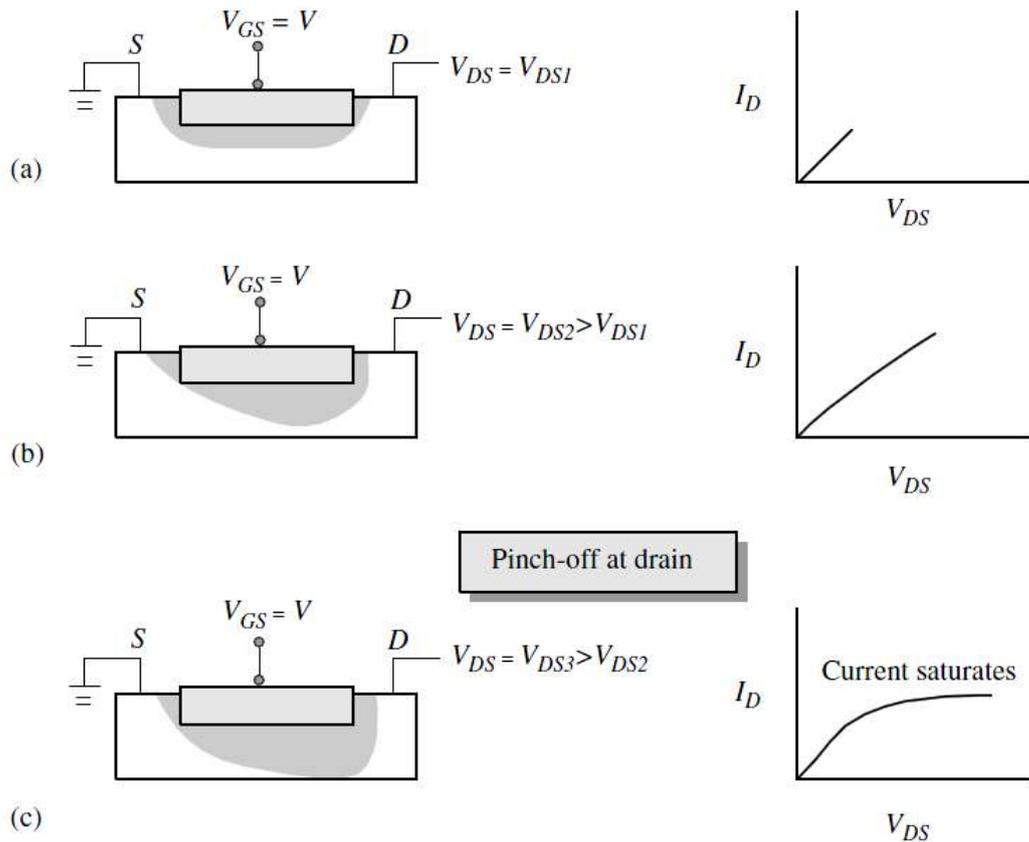


Figure 5.5 change of drain current & channel layer thickness of a MESFET with increasing drain-source bias and fixed gate bias

5.3 Current-voltage characteristics

The structure and diagram of gate band energy in a MESFET device by GaN is shown in Figure 5.6 [99] while the cross-section and width of the depletion area in a MESFET is demonstrated by Figure 5.7 [99]. When the gate potential is zero, the depletion area is uniform demonstrated by Figure 5.7(a). When gate potential is negative, width of depletion area will increase, and finally pinch off the entire active channel. Therefore, along with the gate bias increases more negatively, the effective carriers decrease until the active layer is completely pinched off.

When a constant and unchanged gate potential is applied, width of depletion area will increase at d-terminal along with increasing drain bias demonstrated by Figure 5.7(b) [99]. Finally, active channel will be pinched off from the drain end as the bias at the drain point is higher than the bias at any other points. After this, the current flowing through the channel will keep constant even through the bias at the drain end continues to increase. The voltage of drain-terminal at which active channel is pinched off and current flowing through the channel reaches saturation is defined as the saturation voltage and the current at this time is defined as the saturation current.

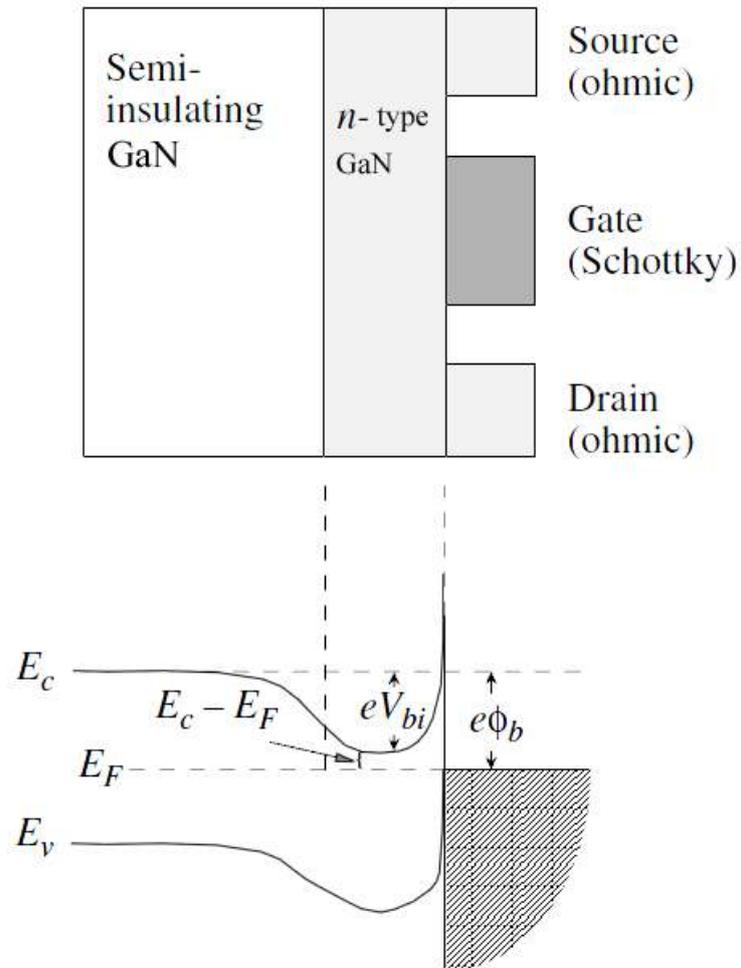


Figure 5.6 the structure and gate diagram of energy band in a MESFET device by GaN

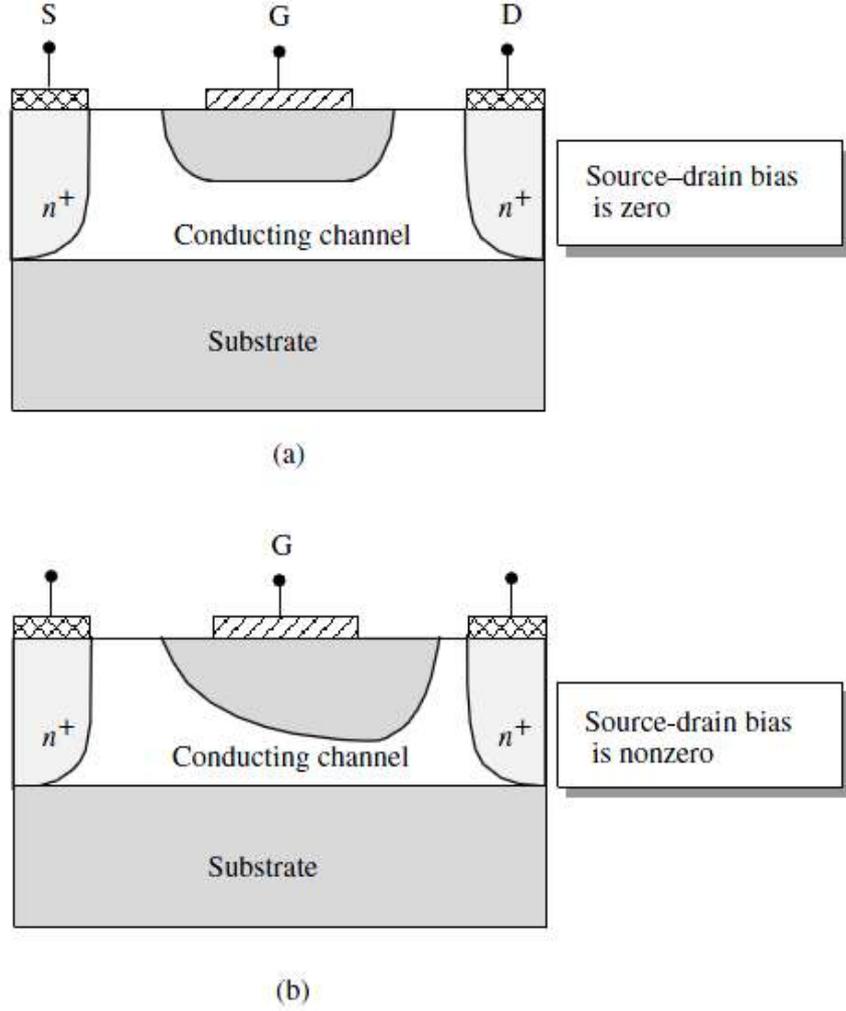


Figure 5.7 channel layer thickness in a MESFET under different source-drain potential

Current of drain is determined by:

$$I_D = Z[h - W(x)]eN_d\mu_n \frac{dV}{dx}, \quad (5.1)$$

where $W(x)$ is depletion area width and h is channel layer thickness, which are shown in Figure 5.8 [99]. The width of the depletion area is determined by:

$$W(x) = \left[\frac{2\varepsilon[V(x) + V_{bi} - V_{GS}]}{eN_d} \right]^{1/2}, \quad (5.2)$$

where V_{GS} is the gate-source bias, V_{bi} is the built-in potential and $V(x)$ is the channel potential.

Since I_D is a constant through the entire channel, I_D can be determined by substituting $W(x)$ into the first equation and integrating:

$$I_D \int_0^L dx = e\mu_n N_d Z \int_0^{V_{DS}} \left[h - \left\{ \frac{2\varepsilon[V(x) + V_{bi} - V_{GS}]}{eN_d} \right\}^{1/2} \right] dV. \quad (5.3)$$

Therefore, I_D is given by the following equation:

$$I_D = \frac{e\mu_n N_d Z h}{L} \left\{ V_{DS} - \frac{2 \left[(V_{DS} + V_{bi} - V_{GS})^{3/2} - (V_{bi} - V_{GS})^{3/2} \right]}{3(eN_d h^2 / 2\epsilon)^{1/2}} \right\}. \quad (5.4)$$

g_0 is defined as the channel conductance before the channel is pinched off, which is given by:

$$g_0 = \frac{e\mu_n N_d Z h}{L}. \quad (5.5)$$

Pinched-off voltage is given by:

$$V_p = \frac{eN_d h^2}{2\epsilon}. \quad (5.6)$$

Therefore, the drain current can be written as:

$$I_D = \frac{e\mu_n N_d Z h}{L} \left\{ V_{DS} - \frac{2 \left[(V_{DS} + V_{bi} - V_{GS})^{3/2} - (V_{bi} - V_{GS})^{3/2} \right]}{3V_p^{1/2}} \right\}. \quad (5.7)$$

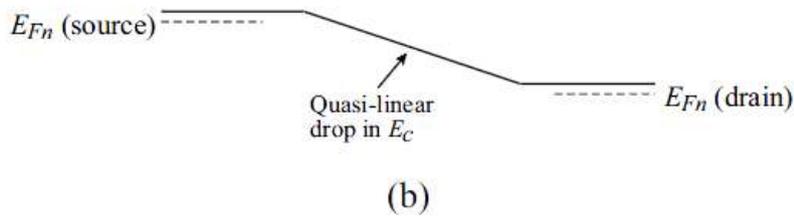
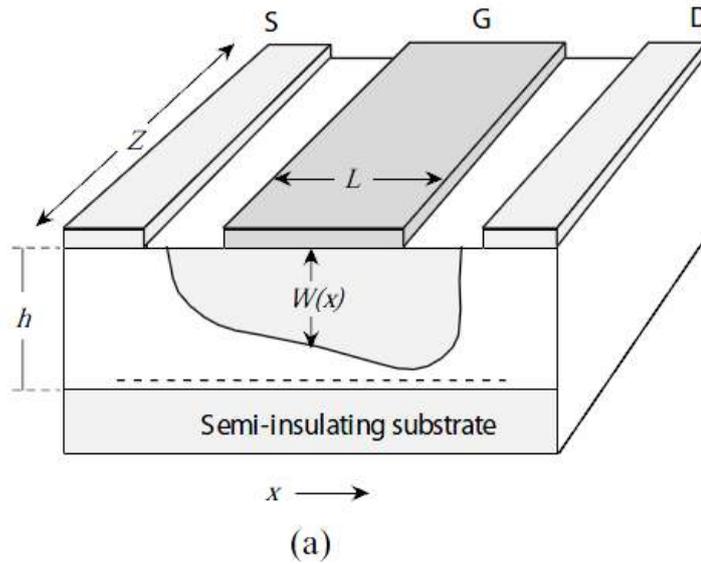


Figure 5.8 the schematic and band diagram along the channel in a MESFET before depletion

The saturation drain-source voltage is given by:

$$V_{DS(sat)} = V_p - V_{bi} + V_{GS}, \quad (5.8)$$

and the saturation current can be written as:

$$I_{D(sat)} = g_0 \left[\frac{V_P}{3} - V_{bi} + V_{GS} + \frac{2(V_{bi} - V_{GS})^{3/2}}{3V_P^{1/2}} \right]. \quad (5.9)$$

The transconductance g_m , which describes the gate control on the drain current, is described by:

$$g_m = \frac{dI_D}{dV_{GS}} \Big|_{V_{DS}=\text{constant}} = g_0 \frac{(V_{DS} + V_{bi} - V_{GS})^{1/2} - (V_{bi} - V_{GS})^{1/2}}{V_P^{1/2}}. \quad (5.10)$$

Through the equations above, it can be aware that materials with shorter active channel length and higher carrier mobility will increase the transconductance of MESFET devices, which means more effective gate control on the channel as well as the device property of higher gain and high frequency.

If the source-drain voltage is much smaller than the difference between the built-in potential and gate voltage, which means $V_{DS} \ll V_{bi} - V_{GS}$, the drain current can be simplified by Taylor series and turns out to be:

$$I_D = g_0 \left[1 - \left(\frac{V_{bi} - V_{GS}}{V_P} \right)^{1/2} \right] V_{DS}. \quad (5.11)$$

In this region, which is considered as linear region, the device is ohmic, demonstrated by Figure 5.9 [99], and transconductance is described as:

$$g_m = \frac{g_0 V_{DS}}{2V_P^{1/2} (V_{bi} - V_{GS})^{1/2}}. \quad (5.12)$$

In the saturation, the transconductance is given by:

$$g_{m(sat)} = g_0 \left[1 - \left(\frac{V_{bi} - V_{GS}}{V_P} \right)^{1/2} \right]. \quad (5.13)$$

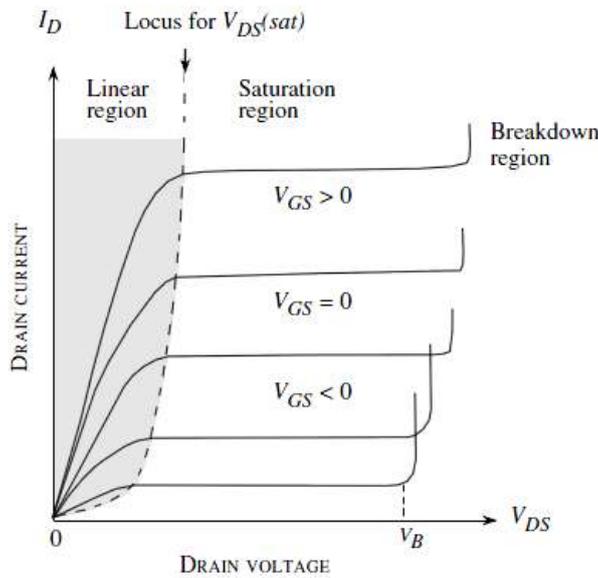


Figure 5.9 I-V characteristics of an n -type MESFET

Chapter 6 Results of Calculation and Simulation

6.1 Physical model

In Figure 6.1 [100, 101], the structure and related parameters of a MESFET device is shown while the nomenclature is defined through the following table.

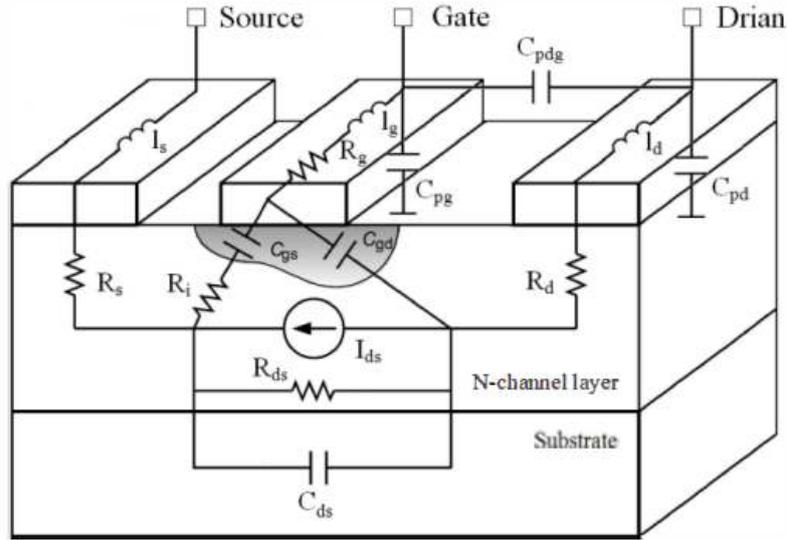


Figure 6.1 the structure & related parameters in a MESFET device

Table 6.1 nomenclature

Q	Unit electron charge
ϵ_S	Absolute dielectric constant of GaN
v_{sat}	Saturation electron drift velocity
μ_n	Electron drift mobility of low field
N_D	Doping concentration
L_g	Gate length
Z_g	Gate width
W	Channel layer thickness
V_{bi}	Schottky barrier built-in potential
V_{p0}	Pinch-off voltage

The cross-sections of a non-self aligned and a self-align MESFET are illustrated in Figure 6.2 [102]. In area I, the drift mobility in the low field is a constant, μ_n , based on the approximation of gradual channel. In area II and III, the electron drift velocity is saturated, which is denoted by v_{sat} [103]. For clarity, uniform doping, N , is assumed in this chapter.

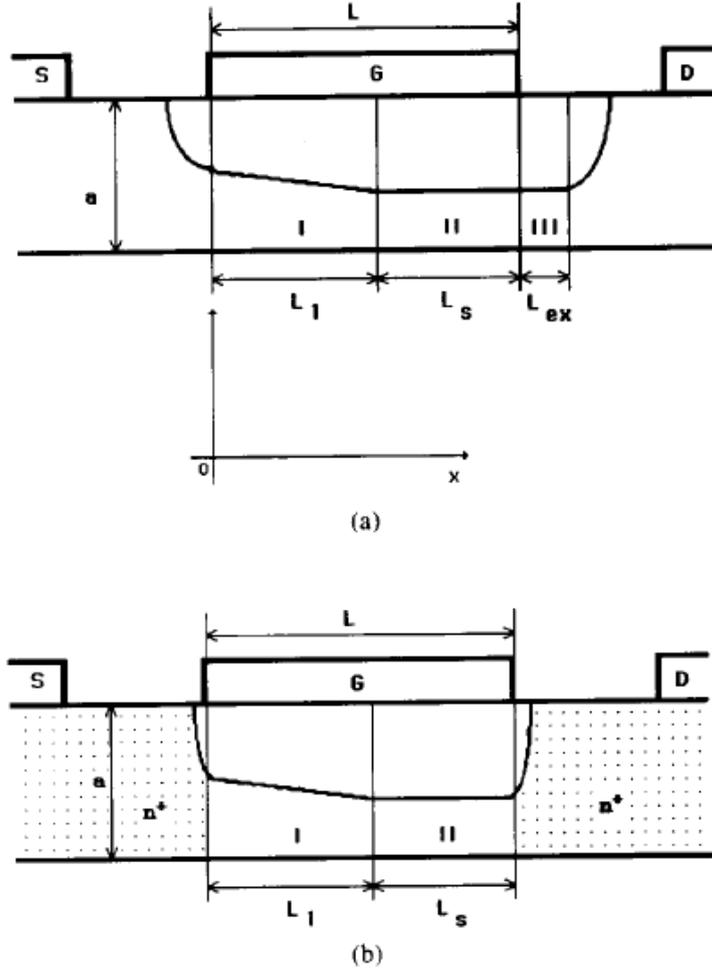


Figure 6.2 cross-sections of a non-self aligned (a) and a self-align (b) MESFET

According to the physical model studied by H. Statz *et al.* (Raytheon model) [104], the drain current is described through the following equation:

$$I_{ds}(V_{ds}, V_{gs}) = I_p(V_{gs}) f_{CLM}(V_{ds}, V_{gs}) P(\alpha, V_{ds}). \quad (6.1)$$

In the above equation, I_p describes the current by electrons with saturation drift velocity and can be obtained by [105]:

$$I_p(V_{gs}) = g_0 V_{p0} \xi \left(1 - \sqrt{\frac{s^4 - s^2 - \xi}{s^2 - (1 + \xi)}} \right), \quad (6.2)$$

where g_0 is conductance of the channel and determined through:

$$g_0 = \frac{q\mu_n N_D Z_g w}{L_g}; \quad (6.3)$$

V_{p0} is the pinch-off voltage and described as:

$$V_{p0} = \frac{qN_D w^2}{2\epsilon_s}; \quad (6.4)$$

$$s = \frac{V_{bi} - V_{gs}}{V_{p0}}; \quad (6.5)$$

ξ is the index of saturation [106] and given by:

$$\xi = \frac{E_s L_g}{V_{p0}}, \quad (6.6)$$

where E_s is the electric field when electron drift velocity is saturated and given by:

$$E_s = \frac{v_{sat}}{\mu_n}. \quad (6.7)$$

f_{CLM} is the factor of channel length modulation and given by [102]:

$$f_{CLM}(V_{ds}, V_{gs}) = \frac{V_{p0} + 3E_s L_g}{V_{p0} + 3E_s(L_g - L_s)}, \quad (6.8)$$

where L_s is the length of saturation area (shown in Figure 6.2) and given by [103]:

$$L_s(V_{ds}, V_{gs}) = 0, \text{ for } 0 < V_{ds} < V_p(V_{gs}); \quad (6.9)$$

$$L_s(V_{ds}, V_{gs}) = \frac{2w}{\pi} \sinh^{-1} \left(\frac{\pi K_d}{2wE_s} [V_{ds} - V_p(V_{gs})] \right), \text{ for } V_{ds} \geq V_p(V_{gs}), \quad (6.10)$$

where V_p is the gate voltage over the non-saturation area and given by:

$$V_p(V_{gs}) = V_{p0} \frac{\xi(1-s)}{\xi+1-s}, \quad (6.11)$$

K_d is the parameter of domain, which is approximate to 1 in the case of this chapter.

The parameter $P(\alpha, V_{ds})$ is given by [104]:

$$P(\alpha, V_{ds}) = 1 - \left(1 - \alpha \frac{V_{ds}}{3} \right)^3, \text{ for } 0 < V_{ds} < \frac{3}{\alpha}; \quad (6.12)$$

$$P(\alpha, V_{ds}) = 1, \text{ for } V_{ds} \geq \frac{3}{\alpha}, \quad (6.13)$$

where α is the curve parameter of non-saturation current and given by [102]:

$$\alpha = \frac{V_{p0} + 3E_s \left(L_g - \frac{2w}{\pi} \sinh^{-1} \left(-\frac{\pi K_d}{2wE_s} \right) \right)}{E_s L_g \left(1 - \sqrt{\frac{E_s L_g}{V_{p0} + E_s L_g}} \right) (V_{p0} + 3E_s L_g)}. \quad (6.14)$$

6.2 Temperature-dependent physical parameters

6.2.1 Schottky barrier built-in potential

The built-in potential of Schottky barrier can be determined by [107-109]:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) - \frac{E_C - E_F}{q}, \quad (6.15)$$

where n_i is the intrinsic carrier concentration of GaN and assumed linearly dependent on the temperature and given by:

$$n_i = 1.9 \times 10^{-10} \frac{T}{300}, \quad (6.16)$$

where 1.9×10^{-10} is the intrinsic carrier concentration (cm^{-3}) of GaN at room temperature (300K);

$E_C - E_F/q$ is described as:

$$\frac{E_C - E_F}{q} = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right), \quad (6.17)$$

where N_C is the conduction band effective density states of GaN and described as:

$$N_C = 2.3 \times 10^{18} \left(\frac{T}{300}\right)^{3/2}, \quad (6.18)$$

where 2.3×10^{18} is the conduction band effective density states (cm^{-3}) of GaN at room temperature.

6.2.2 Dielectric constant

The dielectric constant of GaN is dependent on the temperature and can be described as [110]:

$$\varepsilon_s = \varepsilon_{s0} [1 + \sigma_s (T - 300)], \quad (6.19)$$

where $\varepsilon_{s0} = 9\varepsilon_0$ is the absolute dielectric constant of GaN ($T=300\text{K}$) and $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm² is vacuum absolute dielectric constant; $\sigma_s = 10^{-4}$ K⁻¹ is an empirical constant related to the dielectric constant.

6.2.3 Electron drift mobility of low field

The electron drift mobility of low field in GaN is dependent of the temperature and can be described as [111]:

$$\mu_n = \mu_{n0} \left(\frac{T}{300}\right)^{-1.7}, \quad (6.20)$$

where $\mu_{n0} = 1300$ cm²/V·s is the electron drift mobility of low field in GaN at room temperature.

6.2.4 Saturation electron drift velocity

The saturation electron drift velocity in GaN is dependent of the temperature and can be described as [112]:

$$v_{sat} = v_{sat0} - \sigma_v T, \quad (6.21)$$

where $v_{sat0} = 2.87 \times 10^7$ cm/s is the saturation electron drift velocity in GaN at room

temperature and $\sigma_s=9800$ cm/ K·s is an empirical constant related to saturation electron drift velocity.

In order to calculate v_{sat0} under different drain source voltages, the following equations are used [113]:

$$E = \frac{qN_D}{\epsilon_s} \sqrt{\frac{2\epsilon_s}{qN_D} (V_{bi} + V_{DS} - V_{GS})}, \quad (6.22)$$

where E is gate electric field and,

$$v_{sat0} = \mu_n E. \quad (6.23)$$

6.3 Doping concentration of ion implantation

In this paper, Si is adopted to dope into GaN as the donor impurity through the method of ion implantation with an ion dose of $5 \times 10^{12} \text{cm}^{-2}$, ion energy of 100keV and a protective cap layer of 300Å width. In order to recover the defects induced in the process of ion implantation, annealing is processed at the temperature of 1800°C for one hour after ion implantation.

The impurities are considered to follow a symmetric Gaussian distribution, which is described by [114]:

$$N(x,t) = \frac{Q}{\sqrt{2\pi\sqrt{\Delta R_p^2 + 2Dt}}} \exp\left[-\left(\frac{x - R_p + t_{cap}}{\sqrt{2}\sqrt{\Delta R_p^2 + 2Dt}}\right)^2\right], \quad (6.24)$$

where N is the concentration of impurities, x is depth under the surface of ion implantation, t is the annealing time, Q is the ion dose, ΔR_p and R_p are the straggling and range parameters of ion implantation respectively, D is the diffusion coefficient of Si in GaN, and t_{cap} is the width of cap layer.

Through the software of SRIM, the values of ΔR_p and R_p can be calculated, which are 278Å and 750Å.

The coefficient of diffusion is obtained by:

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right), \quad (6.25)$$

where $D_0=6.5 \times 10^{-11} \text{cm}^2/\text{s}$, $E_a=0.89\text{eV}$ [115] are the prefactor of coefficient of diffusion and activation energy of Si in GaN respectively, and T is the annealing temperature.

In this paper, the impurity concentration of 400Å under the ion implantation surface ($x=400\text{Å}$) is considered as the concentration value of uniform doping, N_D , which is calculated to be $3.47 \times 10^{16} \text{cm}^{-3}$. Meanwhile, the specification of the GaN MESFET device is 1μm gate length, 1000μm gate width and 0.1μm channel layer thickness.

6.4 Results and discussion

MATLAB is used to simulate the temperature-dependent drain current-drain voltage characteristic, current-temperature characteristic, intrinsic carrier concentration-temperature characteristic and saturation electron drift velocity-temperature characteristic, which are presented in the following figures (6.3, 6.4, 6.5 & 6.6).

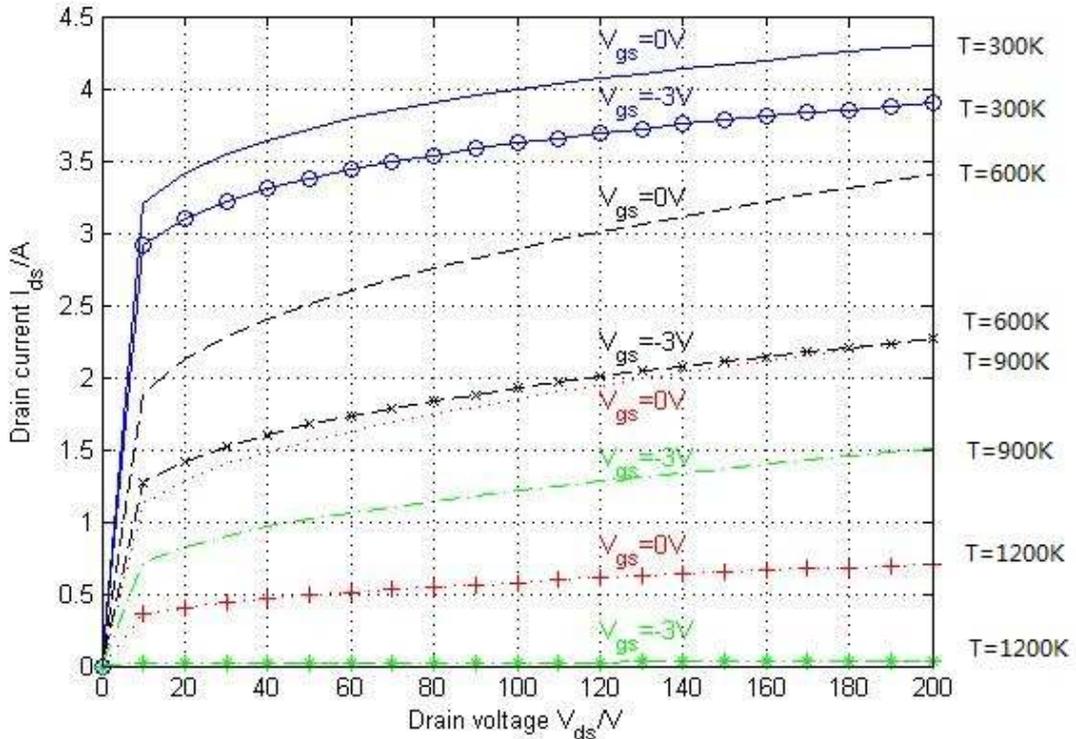


Figure 6.3 drain current-drain voltage characteristic
 $N_D=3.47 \times 10^{17} \text{cm}^{-3}$, $N_A=1 \times 10^{15} \text{cm}^{-3}$, $Z_g=1000 \mu\text{m}$, $L_g=1 \mu\text{m}$, $w=0.1 \mu\text{m}$

The Figure 6.3 shows a plot of temperature influence (300-1200K) on drain current (I_{ds}) versus drain voltage V_{ds} for gate-source voltage (V_{gs}) of 0V and -3V with active channel doping $N_D=3.47 \times 10^{17} \text{cm}^{-3}$, substrate concentration $N_A=1 \times 10^{15} \text{cm}^{-3}$, device width $Z_g=1000 \mu\text{m}$, channel length $L_g=1 \mu\text{m}$, and active channel depth $w=0.1 \mu\text{m}$. The I - V characteristic shows clearly the properties of linear region in the drain-source voltage (V_{ds}) range of 0-10V for $V_{gs}=0V$ and -3V and the linear property of channel current exhibits no variation during the transition from low temperature to high temperature. The saturation region of channel current shows a clear indication of good device with a reasonable pinch-off voltage, which agrees well with active channel thickness. The applied gate voltage, $V_{gs}=0V$ and -3V, shows the device working in the depletion mode and the channel current shows a symmetrical nature for all temperatures. The maximum channel current is obtained at 300K, whereas the minimum channel current is obtained at 1200K without any change in the shape of

channel current nature. The plot in Figure 6.3 was drawn by using the Equation (6.1).

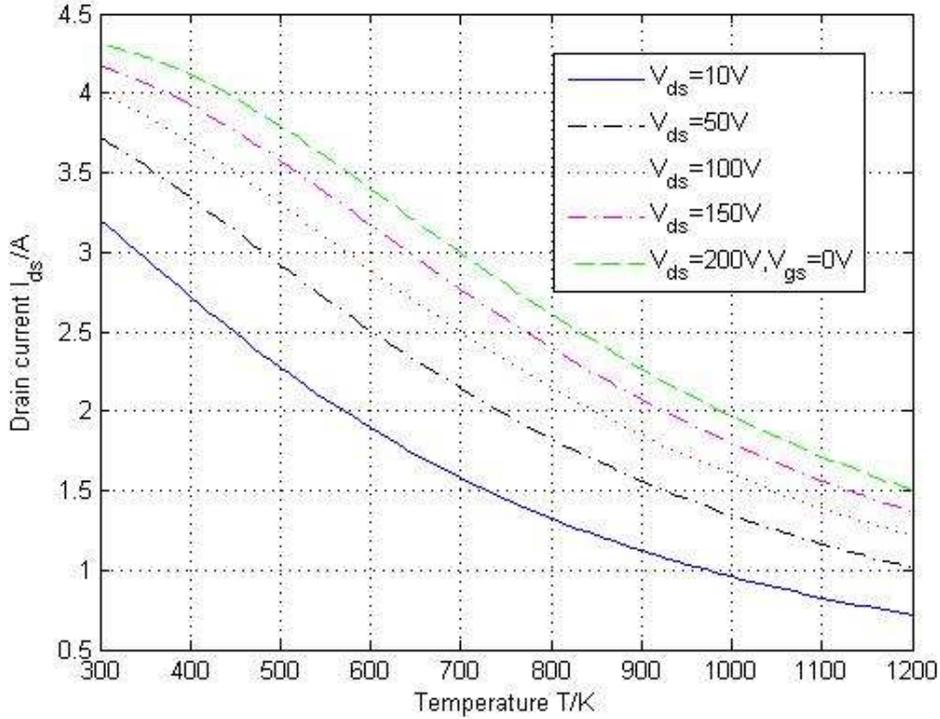


Figure 6.4 current-temperature characteristic
 $N_D=3.47 \times 10^{17} \text{cm}^{-3}$, $N_A=1 \times 10^{15} \text{cm}^{-3}$, $Z_g=1000 \mu\text{m}$, $L_g=1 \mu\text{m}$, $w=0.1 \mu\text{m}$

The Figure 6.4 presents a plot of drain current versus temperatures for different drain-source voltage for $V_{ds}=10\text{V}$, 50V , 100V , 150V and 200V for gate-source voltage $V_{gs}=0\text{V}$ with active channel doping $N_D = 3.47 \times 10^{17} \text{cm}^{-3}$, substrate concentration $N_A=1 \times 10^{15} \text{cm}^{-3}$, device width $Z_g=1000 \mu\text{m}$, channel length $L_g=1 \mu\text{m}$, and active channel depth $w=0.1 \mu\text{m}$. The channel current is decreasing with increasing of temperature from 300K to 1200K and shows consistency with I-V characteristics in Figure 6.3. At high drain-source voltage $V_{ds}=200\text{V}$, the nature of channel current is not the same as $V_{ds}=10\text{V}$ due to the linear and saturation regimes affected by the drain-source voltage. The Figure 6.4 was drawn by using the Equation (6.1).

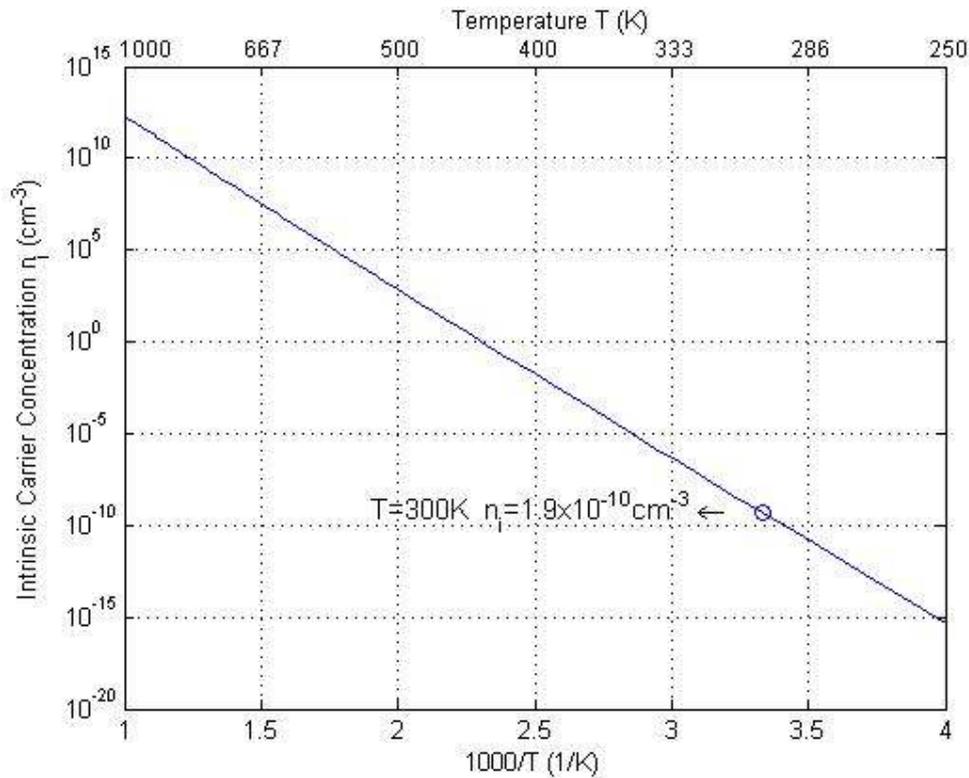


Figure 6.5 intrinsic carrier concentration-temperature characteristic

The Figure 6.5 displays a plot of intrinsic carrier concentration versus temperature considering effective mass and the effect of band gap energy with temperature variation. The intrinsic carrier concentration, n_i , changes from the value of $1 \times 10^{12} \text{cm}^{-3}$ to $1.9 \times 10^{-10} \text{cm}^{-3}$ for the temperature variable from 1000K to 300K. The value of intrinsic concentration of GaN is identical with silicon carbide due to wide band gap properties. The intrinsic carrier concentration is extremely low for GaN and SiC, therefore the built-in voltage is high compared to Si and GaAs. This property will provide the SiC/GaN devices with low reverse recovery time for high power semiconductor devices. The graph in Figure 6.5 was generated by using Equation (6.16).

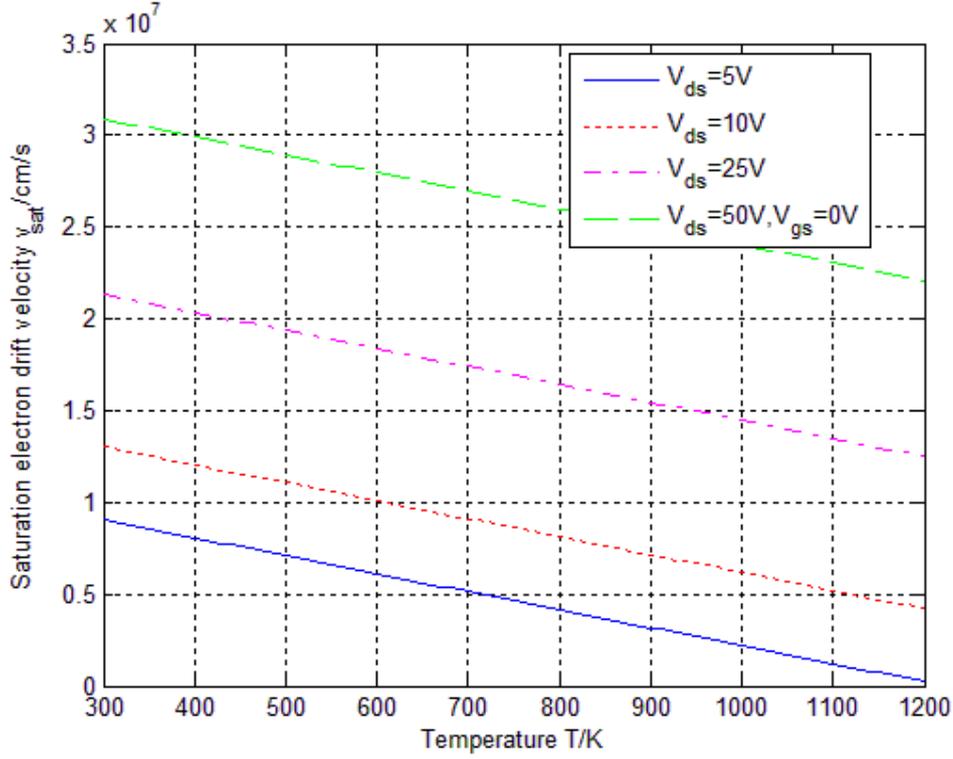


Figure 6.6 saturation electron drift velocity-temperature characteristic
 $N_D=3.47 \times 10^{17} \text{ cm}^{-3}$, $N_A=1 \times 10^{15} \text{ cm}^{-3}$, $Z_g=1000 \mu\text{m}$, $L_g=1 \mu\text{m}$, $w=0.1 \mu\text{m}$

The Figure 6.6 exhibits a plot of saturation electron drift velocity versus temperature for different drain-source voltages, $V_{ds}=5V$, $10V$, $25V$ and $50V$, with gate-source voltage $V_{gs}=0V$, active channel doping $N_D=3.47 \times 10^{17} \text{ cm}^{-3}$, substrate concentration $N_A=1 \times 10^{15} \text{ cm}^{-3}$, device width $Z_g=1000 \mu\text{m}$, channel length $L_g=1 \mu\text{m}$, and active channel depth $w=0.1 \mu\text{m}$. The saturation drift velocity for $V_{ds}=50V$ is linearly decreasing from the value of $3.1 \times 10^7 \text{ cm/s}$ to $2.25 \times 10^7 \text{ cm/s}$ for the temperature variation from $300K$ to $1200K$, whereas the saturation drift velocity for $V_{ds}=10V$ also linearly decreases from $0.85 \times 10^7 \text{ cm/s}$ to $0.1 \times 10^7 \text{ cm/s}$. The large saturation drift velocity obtained at $V_{ds}=50V$ is observed due to the high electric field in the drain region. This plot in Figure 6.6 was generated by using the Equation (6.21).

Chapter 7 Conclusions

To study the effects of temperature on MESFET devices by GaN, analytical modeling based on physical parameters with numerical calculations has been conducted along with simulation through MATLAB software.

Through the current-voltage characteristic and current-temperature characteristic developed in this paper, it can be aware that the drain current of a GaN-based MESFET device increases fast in the linear area and still increases at a slow rate until a very large drain voltage is applied in the saturation area with a wide range of drain voltage. This reflects the potential of GaN-based MESFET devices on the application of high power devices.

Meanwhile, through the temperature-dependent characteristics, the device performance can be anticipated, which helps optimize the parameters and structure of the device.

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Appendix A

Code of Drain Current-Drain Voltage Characteristic Simulation

```
T=300;
q=1.6*10^(-19);           % charge of the electron
ep_s0=9*8.85*10^(-14);    % absolute dielectric constant of GaN at room
                           % temperature (T=300K)
sig_s=1*10^(-4);         % empirical constant of temperature dependence of
                           % dielectric constant
v_sat0=2.87*10^(7);       % saturation electron drift velocity at room temperature
                           % (T=300K)
sig_v=9800;              % empirical constant of temperature dependence of
                           % saturation electron drift velocity
u_n=1300;                % electron low field mobility at room temperature
                           % (T=300K)

L_g=1.0*10^(-4);         % gate length
Z_g=1000*10^(-4);       % gate width
w=0.1*10^(-4);          % channel layer thickness under the gate
Q=5*10^(12);            % ion (Si) implantation dose
R_p=750*10^(-8);        % implant range parameter
deltaR_p=278*10^(-8);   % straggle parameter
t_cap=300*10^(-8);      % cap layer thickness
t=3600;                 % annealing time
T_a=2073;               % annealing temperature (1800 degree Celsius)
V_t=0.026*(T/300);      % thermal voltage
V_ta=0.026*(T_a/300);   % thermal voltage at annealing temperature
D_0=6.5*10^(-11);       % prefactor of diffusion coefficient of Si in GaN
E_a=0.89;               % activation energy of Si
D=D_0*exp(-E_a/V_ta);   % diffusion coefficient of Si
x=0.04*10^(-4);         % implantation depth
N_D=Q/(2*pi*(deltaR_p^2+2*D*t)^(1/2)*exp(-(x-R_p+t_cap)/(2*(deltaR_p^2+
2*D*t)^(1/2)))^(2));    % doping concentration of implanting Si into GaN at x
N_c=2.3*10^(18)*(T/300)^(3/2); % effective conduction band density of states
n_i=1.9*10^(-10)*(T/300); % intrinsic carrier concentration
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D); % built-in voltage of Schottky
                                   % barrier
V_gs=0;                 % gate-source voltage
ep_s=ep_s0*(1+sig_s*(T-300)); % dielectric constant
V_p0=q*N_D*w^2/(2*ep_s); % pinch-off voltage
v_sat=v_sat0-sig_v*T;   % saturation electron drift velocity
u_n0=u_n*(T/300)^(-1.7); % electron low field mobility
g_0=q*N_D*u_n0*w*Z_g/L_g; % conductance of the metallurgical channel
E_s=v_sat/u_n0;
```

```

xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s.*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g)));
V_p=V_p0*xi*(1-s)/(xi+1-s);           % voltage drop across non-saturated region
                                       under the gate
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2)));
V_ds=0:10:200;                       % drain voltage
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p)); % saturation
                                                         region's length
end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s)); %Channel length
                                                modulation factor

P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^(3);
else
    P(k)=1;
end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds);
grid on;
xlabel('Drain voltage V_d_s/V');
ylabel('Drain current I_d_s/A');
hold on;
T=600;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);
n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;

```

```

alp=(V_p0+3*E_s.*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^(3);
else
    P(k)=1;
end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds,'k--');
T=900;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);
n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s.*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
end
end

```

```

end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^3;
    else
    P(k)=1;
    end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds,'r');
T=1200;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);
n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g)));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
    else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
    end
end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^3;
    else
    P(k)=1;
    end
end
I_ds=I_p*f_CLM.*P;

```

```

plot(V_ds,I_ds,'g-.');
T=300;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);
n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
V_gs=-3;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s*(L_g-2*w/pi*asinh(pi/(2*w)/
(1-(E_s/(V_p0+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
V_ds=0:10:200;
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
    else
        L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
    end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^(3);
    else
        P(k)=1;
    end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds,'-o');
grid on;
xlabel('Drain voltage V_d_s/V');
ylabel('Drain current I_d_s/A');
hold on;
T=600;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);

```

```

n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g)));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^(3);
else
    P(k)=1;
end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds,'k--o');
T=900;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);
n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;

```

```

alp=(V_p0+3*E_s.*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1-alp*V_ds(k)/3)^(3);
else
    P(k)=1;
end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds,'r:o');
T=1200;
V_t=0.026*(T/300);
N_c=2.3*10^(18)*(T/300)^(3/2);
n_i=1.9*10^(-10)*(T/300);
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D);
ep_s=ep_s0*(1+sig_s*(T-300));
V_p0=q*N_D*w^(2)/(2*ep_s);
v_sat=v_sat0-sig_v*T;
u_n0=u_n*(T/300)^(-1.7);
g_0=q*N_D*u_n0*w*Z_g/L_g;
E_s=v_sat/u_n0;
xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s.*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g));
V_p=V_p0*xi*(1-s)/(xi+1-s);
I_p=g_0*V_p0*xi*(1-((s^(4)-s^(2)-xi)/(s^(2)-(1+xi)))^(1/2));
L_s=1:length(V_ds);
for k=1:length
    L_s(k)=0;
else
    L_s(k)=2*w/pi*asinh(pi/(2*w*E_s)*(V_ds(k)-V_p));
end

```

```

end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s*(L_g-L_s));
P=1:length(V_ds);
for k=1:length
    P(k)=1-(1- $\alpha$ p*V_ds(k)/3)^3;
else
    P(k)=1;
end
end
I_ds=I_p*f_CLM.*P;
plot(V_ds,I_ds,'g-o');
END

```

Appendix B

Code of Current-Temperature Characteristic Simulation

```
T=230:10:1200;
q=1.6*10(-19); % charge of the electron
ep_s0=9*8.85*10(-14); % absolute dielectric constant of GaN at room
temperature (T=300K)
sig_s=1*10(-4); % empirical constant of temperature dependence of
dielectric constant
v_sat0=2.87*10(7); % saturation electron drift velocity at room temperature
(T=300K)
sig_v=9800; % empirical constant of temperature dependence of
saturation electron drift velocity
u_n=1300; % electron low field mobility at room temperature
(T=300K)
L_g=1.0*10(-4); % gate length
Z_g=1000*10(-4); % gate width
w=0.1*10(-4); % channel layer thickness under the gate
Q=5*10(12); % ion (Si) implantation dose
R_p=750*10(-8); % implant range parameter
deltaR_p=278*10(-8); % straggle parameter
t_cap=300*10(-8); % cap layer thickness
t=3600; % annealing time
T_a=2073; % annealing temperature (1800 degree Celsius)
V_t=0.026*(T/300); % thermal voltage
V_ta=0.026*(T_a/300); % thermal voltage at annealing temperature
D_0=6.5*10(-11); % prefactor of diffusion coefficient of Si in GaN
E_a=0.89; % activation energy of Si
D=D_0*exp(-E_a/V_ta); % diffusion coefficient of Si
x=0.04*10(-4); % implantation depth
N_D=Q/(2*pi*(deltaR_p(2)+2*D*t))(1/2)*exp(-(x-R_p+t_cap)/(2*(deltaR_p(2)+
2*D*t))(1/2)); % doping concentration of implanting Si into GaN at x
N_c=2.3*10(18)*(T/300)(3/2); % effective conduction band density of states
n_i=1.9*10(-10)*(T/300); % intrinsic carrier concentration
V_bi=V_t*log(N_D/n_i)-V_t*log(N_c/N_D); % built-in voltage of Schottky
barrier
V_gs=0; % gate-source voltage
ep_s=ep_s0*(1+sig_s*(T-300)); % dielectric constant
V_p0=q*N_D*w(2)/(2*ep_s); % pinch-off voltage
v_sat=v_sat0-sig_v*T; % saturation electron drift velocity
u_n0=u_n*(T/300)(-1.7); % electron low field mobility
g_0=q*N_D*u_n0*w*Z_g/L_g; % conductance of the metallurgical channel
E_s=v_sat/u_n0;
```

```

xi=E_s*L_g/V_p0;
s=(V_bi-V_gs)/V_p0;
alp=(V_p0+3*E_s.*(L_g-2*w/pi*asinh(pi./(2*w)/
(1-(E_s/(V_p+E_s*L_g)).^(1/2)).*(V_p0+3*E_s*L_g)));
V_p=V_p0.*xi.*(1-s)/(xi+1-s);      % voltage drop across non-saturated region
                                   under the gate
I_p=g_0.*V_p0.*xi.*(1-((s.^4)-s.^2)-xi)/(s.^2)-(1+xi))).^(1/2));
V_ds=10;                            % drain voltage
L_s=1:length(T);
for k=1:length(T)
    if V_ds>=0 && V_ds<V_p(k)
        L_s(k)=0;
    else
        L_s(k)=2*w/pi*asinh(pi/(2*w*E_s(k))*(V_ds-V_p(k))); % saturation
                                                                region's length
    end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s.*(L_g-L_s)); % channel length
                                                    modulation factor
P=1:length(T);
for k=1:length(T)
    if V_ds>=0 && V_ds<3/alp(k)
        P(k)=1-(1-alp(k)*V_ds/3)^(3);
    else
        P(k)=1;
    end
end
I_ds=I_p.*f_CLM.*P;
plot(T,I_ds);
grid on;
xlabel('Temperature T/K');
ylabel('Drain current I_d_s/A');
hold on;
V_ds=50;
for k=1:length(T)
    if V_ds>=0 && V_ds<V_p(k)
        L_s(k)=0;
    else
        L_s(k)=2*w/pi*asinh(pi/(2*w*E_s(k))*(V_ds-V_p(k)));
    end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s.*(L_g-L_s));
P=1:length(T);
for k=1:length(T)

```

```

    if V_ds>=0 && V_ds<3/alp(k)
        P(k)=1-(1-alp(k)*V_ds/3)^(3);
    else
        P(k)=1;
    end
end
I_ds=I_p.*f_CLM.*P;
plot(T,I_ds,'k--');
V_ds=100;
for k=1:length(T)
    if V_ds>=0 && V_ds<V_p(k)
        L_s(k)=0;
    else
        L_s(k)=2*w/pi*asinh(pi/(2*w*E_s(k))*(V_ds-V_p(k)));
    end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s.*(L_g-L_s));
P=1:length(T);
for k=1:length(T)
    if V_ds>=0 && V_ds<3/alp(k)
        P(k)=1-(1-alp(k)*V_ds/3)^(3);
    else
        P(k)=1;
    end
end
I_ds=I_p.*f_CLM.*P;
plot(T,I_ds,'r:');
V_ds=150;
for k=1:length(T)
    if V_ds>=0 && V_ds<V_p(k)
        L_s(k)=0;
    else
        L_s(k)=2*w/pi*asinh(pi/(2*w*E_s(k))*(V_ds-V_p(k)));
    end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s.*(L_g-L_s));
P=1:length(T);
for k=1:length(T)
    if V_ds>=0 && V_ds<3/alp(k)
        P(k)=1-(1-alp(k)*V_ds/3)^(3);
    else
        P(k)=1;
    end
end
end

```

```

I_ds=I_p.*f_CLM.*P;
plot(T,I_ds,'m-');
V_ds=200;
for k=1:length(T)
    if V_ds>=0 && V_ds<V_p(k)
        L_s(k)=0;
    else
        L_s(k)=2*w/pi*asinh(pi/(2*w*E_s(k))*(V_ds-V_p(k)));
    end
end
f_CLM=(V_p0+3*E_s*L_g)/(V_p0+3*E_s.*(L_g-L_s));
P=1:length(T);
for k=1:length(T)
    if V_ds>=0 && V_ds<3/alp(k)
        P(k)=1-(1-3/alp(k)*V_ds/3)^3;
    else
        P(k)=1;
    end
end
I_ds=I_p.*f_CLM.*P;
plot(T,I_ds,'g--');
END

```

Appendix C

Code of Intrinsic Carrier Concentration-Temperature Characteristic Simulation

```
T=250:10:1000;
a=1000./T;
N_c=2.3*10^(18)*(T/300).^(3/2);
E_g=3.47-7.7*10^(-4)*(T.^2)./(T+600);
semilogy(a,n_i);
grid on;
hold on;
plot(a(6),n_i(6),'o');
text(1.9,n_i(6),'T=300K   n_i=1.9x10^-1^0cm^-^3 \leftarrow','FontSize',11);
xlabel('1000/T (1/K)');
ylabel('Intrinsic Carrier Concentration n_i (cm^-^3)');
END
```

Appendix D

Code of Saturation Electron Drift Velocity-Temperature Characteristic Simulation

```
V_gs=0;
V_ds=5;
q=1.6*10^(-19);
u_n=1300;
ep_s0=9*8.85*10^(-14);
sig_v=9800;
N_D=3.46*10^(16);
N_c=2.3*10^(18);
n_i=1.9*10^(-10);
V_t=0.026;
E=q*N_D/ep_s0*(2*ep_s0/(q*N_D)*(V_bi+V_ds-V_gs))^(1/2);
v_sat0=u_n*E;
T=300:10:1200;
v_sat=v_sat0-sig_v*T;
plot(T,v_sat);
grid on;
xlabel('Temperature T/K');
ylabel('Saturation electron drift velocity v_s_a_t/cm/s');
hold on;
V_ds=10;
E=q*N_D/ep_s0*(2*ep_s0/(q*N_D)*(V_bi+V_ds-V_gs))^(1/2);
v_sat0=u_n*E;
T=300:10:1200;
v_sat=v_sat0-sig_v*T;
plot(T,v_sat,'r:');
V_ds=25;
E=q*N_D/ep_s0*(2*ep_s0/(q*N_D)*(V_bi+V_ds-V_gs))^(1/2);
v_sat0=u_n*E;
T=300:10:1200;
v_sat=v_sat0-sig_v*T;
plot(T,v_sat,'m-.');
V_ds=50;
E=q*N_D/ep_s0*(2*ep_s0/(q*N_D)*(V_bi+V_ds-V_gs))^(1/2);
v_sat0=u_n*E;
T=300:10:1200;
v_sat=v_sat0-sig_v*T;
plot(T,v_sat,'g--');
END
```