

CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

DESIGN OF A TWO STAGE LOW NOISE AMPLIFIER

A graduate project submitted in partial fulfillment of the requirements

For the degree of Master of Science in

Electrical Engineering

By

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May 2015

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ACKNOWLEDGEMENT

“Gratitude is highest of all the feelings”

I begin my dissertation with gratitude to the God and my parents, Dr. Vishnumurthy Pachikanti, Vasantha Kumari Pachikanti whose gracious blessings have framed me to this extent of life.

I express my gratitude and honor to my guide and project advisor, Dr. Matthew Radmanesh, who has given me immense inspiration in taking up this task and for his constant encouragement and support. I am deeply indebted to him for the intellectual and moral support.

I sincerely express my gratitude to the other committee professors, Prof. Austin Chen and Prof. Benjamin F. Mallard for their constant support, generous help and whose valuable suggestions left an enduring impression on me.

My special thanks to my family physician Dr. A. Rosaiah, and my sister Dr. Naga Swetha Pachikanti for their constant care, encouragement and moral support and who felt my success as their own.

Finally, I extend my sincere thanks to Mohan Munukuntla and all who has provided me with study material, journals, valuable suggestions due to which I could accomplish the task of completing this dissertation.

Abhinav Pachikanti

CONTENTS

SIGNATURE PAGE.....	ii
ACKNOWLEDGMENT.....	iii
List of Figures.....	vi
List of Tables.....	viii
ABSTRACT.....	ix
CHAPTER 1. INTRODUCTION	
1.1 OVERVIEW.....	1
1.2 PROBLEM.....	3
1.3 SCOPE.....	3
1.4 OUTLINE.....	4
CHAPTER 2. DESIGN THEORY	
2.1 AMPLIFIER DESIGN.....	5
2.1.1 CLASSES OF AMPLIFIERS.....	5
2.1.2 AMPLIFIER BASED ON SIGNAL LEVEL.....	6
2.2 DC BIASING.....	7
2.3 DESIGN STEPS.....	9
2.4 STABILITY.....	11
2.5 GAIN.....	12
2.6 MATCHING DESIGN.....	13
CHAPTER 3. DESIGN PROCEDURE.....	14
3.1 STABILITY CHECK.....	15

3.2 MINIMUM NOISE AMPLIFIER.....	16
3.2.1 GAIN CALCULATION.....	16
3.2.2 INPUT & OUTPUT MATCHING FOR MNA.....	17
3.3 MAXIMUM GAIN AMPLIFIER.....	19
3.3.1 GAIN CALCULATION.....	19
3.3.2 UNILATERAL FIGURE OF MERIT.....	20
3.3.3 INPUT & OUTPUT MATCHING FOR MGA.....	21
3.4 OVERALL GAIN FOR COMBINING.....	23
3.5 NOISE FIGURE FOR CASCADED AMPLIFIER.....	23
CHAPTER 4. SIMULATION & RESULTS.....	24
4.1 VMMK-1218 TRANSISTOR.....	24
4.2 FIRST STAGE OF MINIMUM NOISE AMPLIFIER DESIGN.....	25
4.2.1 SIMULATION RESULT FOR MNA.....	26
4.3 SECOND STAGE OF MAXIMUM GAIN AMPLIFIER.....	28
4.3.1 SIMULATION RESULT FOR MGA.....	29
4.4 CASCADING TWO STAGE AMPLIFIER USING ADS.....	31
4.4.1 SIMULATION RESULT FOR TWO STAGE AMPLIFIER.....	32
CHAPTER 5. CONCLUSION.....	34
REFERENCES.....	35
APPENDIX-A RF/MICROWAVE E-BOOK.....	36
APPENDIX-B MATLAB.....	40
APPENDIX-C DATASHEET.....	47

List of Figures

Figure 1 BLOCK DIAGRAM OF AN AMPLIFIER.....	2
Figure 2 CHARACTERISTICS FOR FET TRANSISTOR	7
Figure 3 CIRCUIT DIAGRAM OF DC-BAIS	8
Figure 4 DESIGN STEPS	9
Figure 5 DESIGN OF MATCHING NETWORK.....	13
Figure 6 SMITH CHART MATCHING NETWORK FOR MNA.....	17
Figure 7 MATCHING NETWORK FOR MNA.....	18
Figure 8 SMITH CHART MATCHING NETWORK FOR MGA.....	21
Figure 9 MATCHING NETWORK FOR MGA.....	22
Figure 10 VMMK-1218 TRANSISTOR IN ADS	24
Figure 11 USING ADS, SCHEMATIC OF MNA	25
Figure 12 POWER GAIN Vs FREQUENCY MNA	26
Figure 13 NFmin Vs FREQUENCY MNA	26
Figure 14 INPUT VSWR Vs FREQUENCY MNA	27
Figure 15 OUTPUT VSWR Vs FREQUENCY MNA	27
Figure 16 USING ADS, SCHEMATIC OF MGA.	28
Figure 17 POWER GAIN Vs FREQUENCY MGA	29
Figure 18 NFmin Vs FREQUENCY MGA	29

Figure 19 INPUT VSWR Vs FREQUENCY MGA	30
Figure 20 OUTPUT VSWR Vs FREQUENCY MGA	30
Figure 21 SCHEMATIC OF TWO STAGE AMPLIFIER.....	31
Figure 22 POWER GAIN Vs FREQUENCY LNA.....	32
Figure 23 NFmin Vs FREQUENCY LNA	32
Figure 24 INPUT VSWR GAIN Vs FREQUENCY LNA	33
Figure 25 OUTPUT VSWR GAIN Vs FREQUENCY LNA	33
Figure 26 MAIN MENU.....	36
Figure 27 SPECIFICATIONS	37
Figure 28 STABILITY CHECK USING THE E-BOOK.....	38
Figure 29 GAIN CALUCATIONS	39

List of Tables

Table 1 SPECIFICATIONS.....	3
Table 2 S-parameter FROM DATA SHEET	14
Table 3 OBTAIN VALUES.....	34

Abstract

DESIGN OF A MICROWAVE TWO-STAGE LOW NOISE AMPLIFIER

AT 17GHz

BY

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MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

The goal of the project is to design a low noise amplifier to meet the specific noise figure less than 2dB and Gain more than be over $> 20\text{dB}$ at a frequency of 17GHz. To achieve low noise, the amplifier is designed in two stages in which 1st stage is minimum noise amplifier (MNA) and 2nd stage is a maximum gain amplifier (MGA).

The main goal of this amplifier is to achieve minimum noise and maximum possible gain. The performance of the amplifier is analyzed using ADS. A DC biasing circuit is designed to power the two stage amplifier.

CHAPTER 1. INTRODUCTION

1.1 OVERVIEW

Amplifier is an electronic device that amplifies the weak signals. Low noise amplifiers commonly find their use in wireless communications. Most of the RF and microwave receivers have amplifiers and they are used in commercial and military applications. The function of the low noise amplifier is mainly amplification of low-level signals and also to produce low noise. Taking an example of large signal levels, LNA does the amplification of the signal received with zero noise and channel interference.

LNA design in Radio Frequency circuits consists of characteristics like stability, noise figure, gain, utilization of power and its complexity. Transistor amplifiers also find their uses, at frequencies greater than 100 GHz in different applications in which size should be small, noise figure should be low, bandwidth should be wide and power capacity should be low to medium. A vast range of concepts like two port network, study of microwave transmission lines and smith chart techniques are used for the design of these amplifiers. Some of the transistors with the low noise amplifier ability are CMOS, BJT, and FET etc. In this project, LNA is designed using the Avago technologies VMMK-1218 Pseudomorphic High Electron Mobility Transistor (PHEMT) in a high frequency range.

LNA is an important part of communications where the receiver positioned at front end, it amplifies the weak signals captured by the antenna in the front and reduces losses. The main purpose of LNA is to have minimum noise and amplify the received signals to acceptable levels. In the first stage, the amplifier should have a high

amplification in order to get low noise levels. So JFETs, MESFETs, MOSFETs and HEMTs are usually used. In narrow band circuits, to improve the gain, input and output matching circuits are used. A low noise amplifier is one of a receiver's important parts and is placed as the first stage of a microwave receiver.

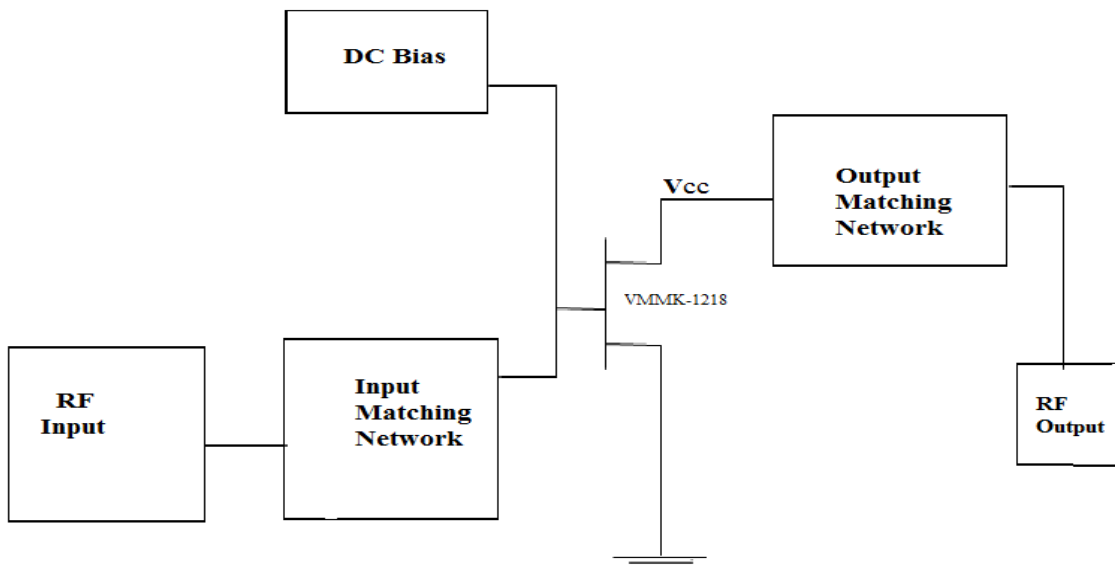


Figure 1 BLOCK DIAGRAM OF AN AMPLIFIER

1.2 PROBLEM

The goal of the project is to Design a Low Noise Amplifier at a frequency of 17GHz while obtaining a low noise figure and a high gain. Design of LNA can be implemented by studying proper matching techniques to achieve required gain and low noise.

Design specification to be done:

Frequency (GHz)	17
Gain (dB)	20
Noise Figure (dB)	2

Table 1 SPECIFICATIONS

1.3 SCOPE

The scope of the project can be done in two ways. The first one is analytical method which can simulate the gain and noise calculations using Mat lab. The second one is analyzed using the Advance Design System (ADS).

1.4 OUTLINE

Chapter 1: Deals with the introduction of Low noise amplifier and briefly gives information about the scope of the project and its background.

Chapter 2: Discusses the classes of amplifier like small signal and large signal amplifiers. Briefly explains the low noise amplifier applications and methodology.

Chapter 3: Illustrates the design procedures and matching networks required to design the two-stage LNA. Gain and noise figure calculations are also mentioned.

Chapter 4: Gives the simulation results of the two-stage LNA using ADS.

Chapter 5: Finally provides the conclusion of the whole project and also gives the recommendations to improve the performance of the amplifier design.

CHAPTER 2. DESIGN THEORY

2.1 Amplifier Design

Amplifier is an electronic device used for amplifying electrical signals amplitude. The amplifier increases voltage, current or power of any applied signal. Basically, the amplifiers are of four types: voltage amplifiers, current amplifiers, trans-conductance amplifiers and trans-resistance amplifiers.

An amplifier takes energy from a power supply and controls the output so that it matches the input signal shape and produces it with a greater amplitude than before. Thus the output of the power supply is to modulate by an amplifier, produce a stronger output signal than the input signal. An amplifier's working is basically quite opposite to the working of an attenuator as an amplifier provides gain, whereas on the other hand, an attenuator produces a loss.

2.1.1 CLASSES OF AMPLIFIERS

Operation of an amplifier is usually in one of the following classes:

- A. **Class A amplifiers:** In Class A mode, each transistor works in the active region in the amplifier.
- B. **Class B amplifiers:** This is the mode of operation in which each transistor operates in its active region for almost half of the signal cycle.
- C. **Class AB amplifiers:** In Class AB mode, for small signals, an amplifier operates in class A and for large signals, it operates in class B. They have active region for less than half of the signal cycle.

D. Class C amplifier: Class C is the mode in which the transistors are in its active region for the complete cycle of signal. They have the active region for almost half of the signal cycle.

2.1.2 Amplifier based on signal level

Microwave amplifiers are mostly classified into two types. Signal level is the basis of the Analysis in both types of amplifiers. Each mode has a different analytical style.

1) Small signal Amplifiers

They use small signal analysis. This method of analysis assumes the fluctuation of the signal from each side of the steady bias levels to be of a low small level, resulting in a very small part of the operating characteristic to be covered. Thus the mode of operation is linear.

2) Large signal Amplifiers

In this method, large signal analysis is used to analyze large signal amplifiers. Greater part of operating characteristics are covered which also include nonlinear parts. As they are used with active circuits that have a high amplitude signal. Also, large signal amplifiers are way more complexly designed in comparison to small signal amplifiers.

Since small signal amplifier is being designed, we do not need to take into account the nonlinear part in the operating device. All Amplifiers require optimization of overall noise figure or gain according to the design specification. So each design will be an interplay of circles of noise figure and constant gain.

Also, these two blocks should be properly isolated from each other so that there is no leakage of the RF signal into the DC circuit when it is going from the input to the output.

Since in the small signal mode the transistor has to operate in a linear region so it should operate in class 'A' mode.

2.2 DC Biasing

The first step in the design of the amplifier is to choose a transistor which meets specification design. For the design of a low noise device, the transistor should be DC biased at a suitable Q-point, so that it ensures the transistor operates in its active or linear region. This depends on noise figure, gain and type of the transistor as FET, P-HEMT, MOSFET, and MESFET and so on.

Q-point should be around the middle of the range for FET curves should be chosen such that it's operating in an active mode.

Drain voltage (V_d) = 3V and Drain-Source current (I_{ds}) = 20 mA.

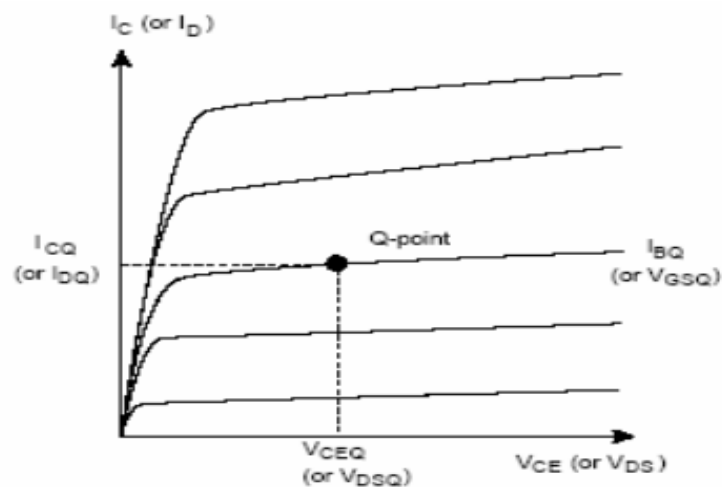


Figure 2 CHARACTERISTICS FOR FET TRANSISTOR

DC circuit should be totally separated from any path, so that RF/MW signals may travel to ensure that there is no leakage.

1. An inductor, also known as RF choke is connected between DC source and RF/MW circuit. A ferrite bead can be used for this.
2. A quarter wave transformer should be attached between DC source and RF circuit with a characteristics impedance that is high enough so that a path is created that has high impedance for any RF signal.
3. A capacitor with high impedance has to be connected as a load to the transformer to get an open circuit at the input having the RF circuit.

The above steps show how we create a high isolation between the DC and the RF circuits in order to operate the amplifier efficiently.

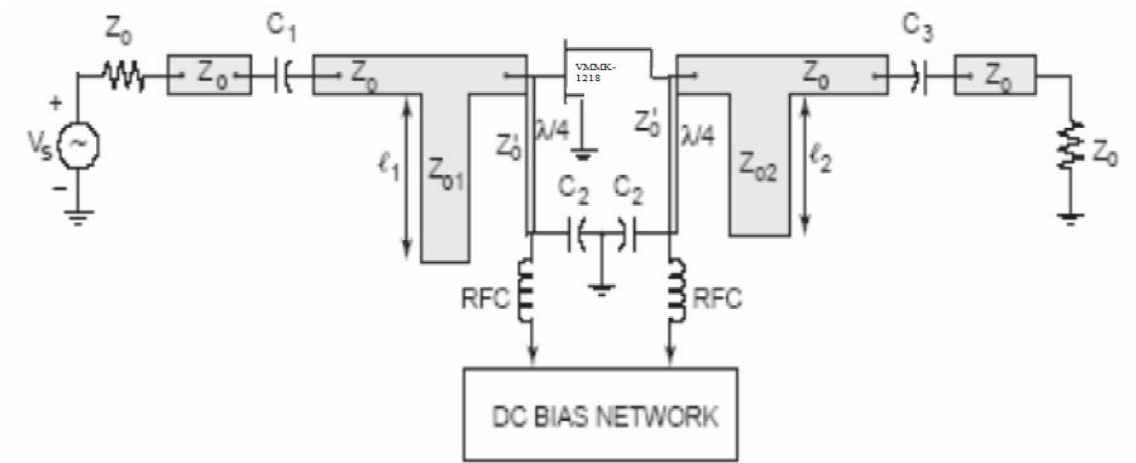


Figure 3 CIRCUIT DIAGRAM OF DC-BAIS

2.3 Design Steps

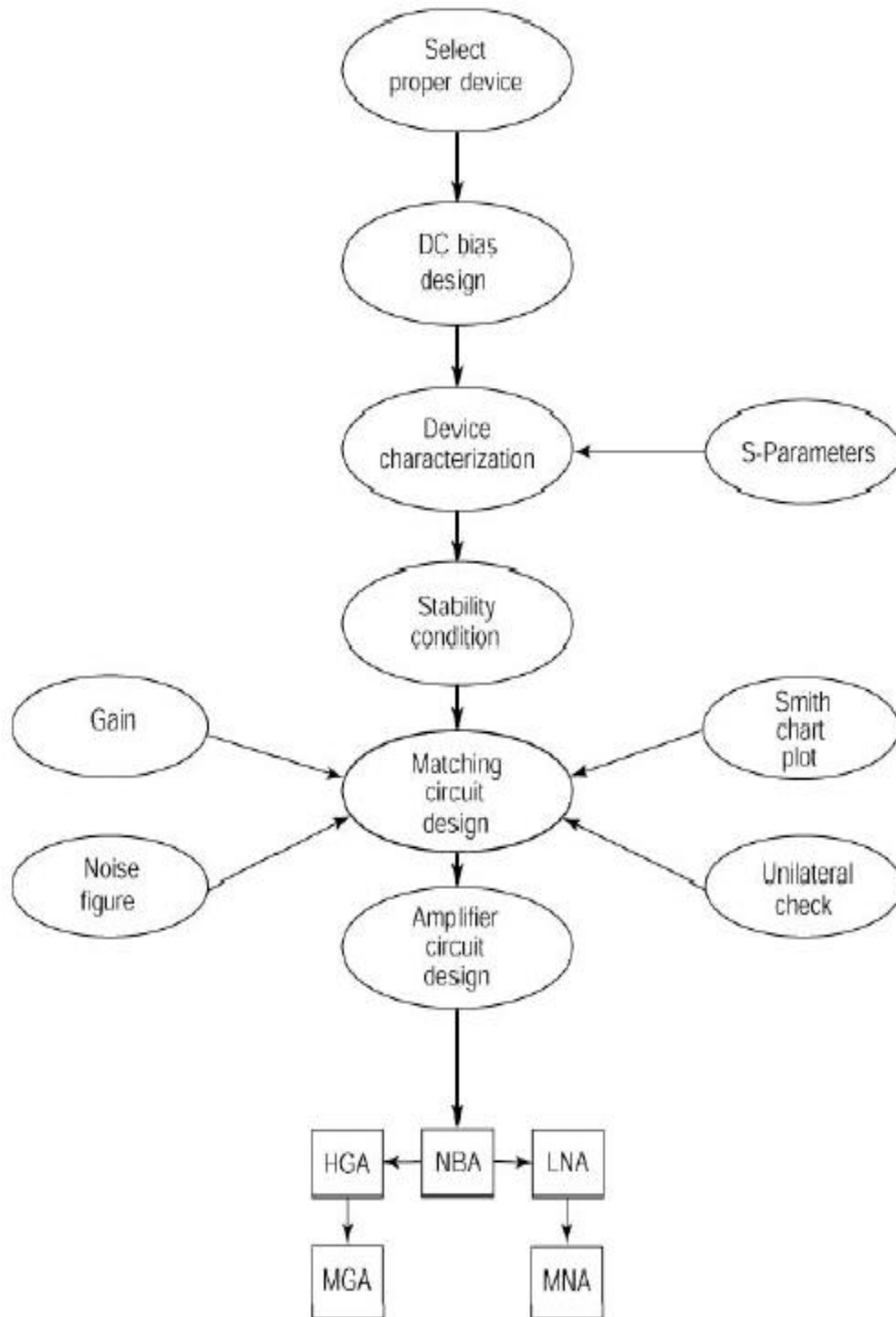


Figure 4 DESIGN STEPS

Step 1: Proper Device selection

Device should be selected based on required specifications of the amplifier.

Considering an example, in which we assume that for gain G , we have to choose transistor with $|S_{21}/S_{12}|$ greater than required gain G .

If we want noise figure F_o then F_{\min} of the transistor should be less than noise figure F_o .

Step 2: DC Bias Design

Now, according to selection of FET, bias the transistor in the midrange of I_D - V_{DS} curves respectively.

Step 3: Device Characterization

After proper device selection using DC bias, we know the Q-point using which we calculate S-parameter of transistor at that Q-point.

Step 4: Stability Conditions

On the particular selected frequency, stability conditions like stability factor K has to be checked which should be greater than 1 and magnitude of D should be less than 1. In case of the error, stable region has to be found by using methods like smith chart. Input and output stability circle has to be drawn on the chart and from that, stable region can be found.

Step 5: Design Matching Circuit

The matching network should be designed based upon the gain and noise requirements of the amplifier.

This gives us 2 cases:

A. If $S_{12}=0$, then unilateral design formulas are used.

B. If $S_{12}\neq 0$, first the unilateral figure of merit is calculated and in case of error range being small, unilateral design formula is used. Otherwise bilateral design formula is used.

Step 6: Amplifier Circuit Design Based on the type of Amplifier, design input and output matching networks.

A. Narrow-band Amplifier design (NBA)

B. High-gain amplifier design (HGA) & Maximum-gain amplifier design (MGA)

C. Wide-band Amplifier design (WBA)

D. Low-noise amplifier design (LNA) & Minimum-noise amplifier design (MNA)

2.4 Stability

For designing the LNA, S-parameters of a transistor are selected from the data sheet (Avago technologies VMMK-1218). Stability check has to be done to ensure that the transistor is unconditionally stable or conditionally stable.

Stability is checked by using the formulae:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{22}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

If $K > 1$ and $\Delta < 1$, it is unconditionally stable.

Otherwise, if $K < 1$ and $\Delta > 1$ it is conditionally stable.

2.5 Gain

Gain in an amplifier plays an important role in the design process. If we want to use the unilateral assumption and unilateral gain equations, two cases have to be considered:

- 1) If $S_{12} = 0$, then unilateral design formulas have to be used.
- 2) For $S_{12} \neq 0$, the unilateral figure of merit (U) has to be calculated and the error range has to be found and if it is very small, then unilateral assumption is used. Otherwise, bilateral design formulas are used.

Error Range

We need to determine the error involved in our analysis by checking the unilateral figure of merit (U). The unilateral design formula has to be used to find the error range.

$$U = \frac{|S_{12}||S_{21}||S_{11}||S_{22}|}{(1 - S_{11}^2)(1 - S_{22}^2)}$$
$$\frac{1}{(1 + U)^2} < \frac{G_T}{G_{TUmax}} < \frac{1}{(1 - U)^2}$$

When the transistor is unilateral, then the equations simplify as follows:

$$\Gamma_{IN} = S_{11}^*$$

$$\Gamma_{OUT} = S_{22}^*$$

In this case, the condition provides the maximum transducer gain ($G_{TU, max}$):

$$G_{TU, max} = G_{S, max} G_O G_{L, max}$$

Where

$$G_s = \frac{1 - |\Gamma_s|^2}{|1 - \Gamma_{IN}\Gamma_s|^2}$$

$$G_o = |S_{21}|^2$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

2.6 Matching Circuit Design

In the current network design, we compromise between the noise and gain since our main motto is to obtain a low noise figure and high gain respectively. When designing the circuit, allotted gain values for input matching network (G_s) as well as output (G_L) and the transistor gain (G_o) have to be allotted accordingly. Then we draw the input and output gain circles along with the noise figure circles on same smith chart. To obtain the desired noise figure circle, gain circle intersecting points have to be perfectly selected.

To design the matching networks we need to plot Γ_s for the input matching network and Γ_L for the output matching network.

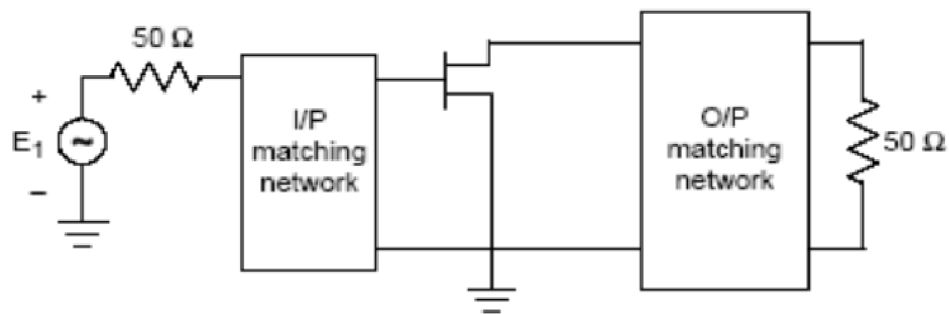


Figure 5 DESIGN OF MATCHING NETWORK

CHAPTER 3. DESIGN PROCEDURE

Using the transistor data sheet, S-parameter, F_{\min} and Γ_{opt} were selected at a frequency of 17GHz.

$$S_{11} = 0.8 \angle 113.80^\circ \qquad S_{12} = 0.06 \angle -46.49^\circ$$

$$S_{21} = 2.00 \angle -8.47^\circ \qquad S_{22} = 0.35 \angle -174.07^\circ$$

$$F_{\min} = 1.13 \text{ dB}$$

$$\Gamma_{\text{opt}} = 0.56 \angle -132.9^\circ$$

VMMK-1218 Typical Scattering Parameters and Noise Parameters, $T_A=25^\circ\text{C}$, $V_{ds}=3\text{V}$, $I_{ds}=20\text{mA}$ [1]

Freq GHz	S11			S21		S12		S22		MSG/MAG
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
2	0.90	-78.41	20.88	11.07	129.30	0.05	44.78	0.59	-45.41	29.71
3	0.85	-106.62	19.27	9.19	111.50	0.06	29.68	0.50	-61.56	26.11
4	0.82	-129.23	17.67	7.65	96.89	0.07	17.84	0.43	-74.78	23.29
5	0.80	-146.90	16.21	6.47	84.82	0.07	8.51	0.38	-85.37	21.29
6	0.79	-161.57	14.90	5.56	74.28	0.07	0.60	0.35	-94.96	19.70
7	0.78	-173.94	13.71	4.85	64.67	0.07	-6.02	0.32	-103.77	18.32
8	0.78	175.49	12.63	4.28	55.85	0.07	-12.05	0.31	-112.18	17.17
9	0.78	166.35	11.62	3.81	47.60	0.07	-17.59	0.30	-120.67	16.14
10	0.78	158.10	10.70	3.43	39.76	0.07	-22.09	0.29	-128.21	15.23
11	0.79	150.68	9.87	3.11	32.39	0.07	-26.72	0.29	-135.58	14.44
12	0.79	143.93	9.09	2.85	25.16	0.07	-30.99	0.30	-142.88	13.76
13	0.79	137.47	8.38	2.62	18.21	0.07	-34.81	0.31	-149.97	13.11
14	0.80	131.33	7.71	2.43	11.48	0.06	-38.24	0.31	-156.46	12.54
15	0.80	125.54	7.11	2.27	4.87	0.06	-40.97	0.33	-162.44	12.02
16	0.80	119.64	6.53	2.12	-1.87	0.06	-44.55	0.34	-168.20	11.55
17	0.81	113.80	6.00	2.00	-8.47	0.06	-46.49	0.35	-174.07	11.14
18	0.81	108.24	5.48	1.88	-14.69	0.06	-49.45	0.36	-179.63	10.72

Table 2 S-parameter FROM DATA SHEET

3.1 Stability check

At a selected frequency, check whether $K > 1$ and $\Delta < 1$. If it doesn't meet the requirements then find the stable region using smith chart by drawing the stability circles.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{11}S_{22}|}$$

$$= \frac{1 - |0.8|^2 - |0.35|^2 + |0.164|^2}{2|0.8 \cdot 0.35|}$$

$$= 1.033 > 1$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$= (0.8 \angle 114^\circ) \times (0.35 \angle -174^\circ) - (0.06 \angle -47^\circ) \times (2.00 \angle -9^\circ)$$

$$= 0.1643 \angle -6^\circ$$

3.2 Minimum Noise Amplifier

MNA is a special case of the low noise amplifier to achieve minimum noise figure level. In the MNA stage, the noise figure is obtained when $\Gamma_s = \Gamma_{opt}$, which gives a noise figure equal to the F_{min}

$$\Gamma_{opt} = \Gamma_s = 0.56 \angle -132.9^\circ$$

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_{opt}}{1 - S_{11}\Gamma_{opt}} \right)^*$$

$$= \left(0.35 \angle -174^\circ + \frac{(0.06 \angle -47^\circ) \times (2.00 \angle -9^\circ) \times (0.56 \angle -133^\circ)}{1 - (0.8 \angle 114^\circ) \times (0.56 \angle -133^\circ)} \right)^*$$

$$= \left(0.35 \angle -174^\circ + \frac{0.067 \angle 172^\circ}{0.595 \angle 14^\circ} \right)^* = (0.35 \angle -174^\circ + 0.112 \angle 158^\circ)^* = 0.45 \angle -179^\circ$$

3.2.1 Gain Calculation

$$G_L = \frac{1}{|1 - \Gamma_s|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2}$$

$$= \frac{1}{|1 - 0.56|^2} |2|^2 \frac{1 - |0.452|^2}{|1 - 0.35 \times 0.452|^2} = \frac{1}{0.1936} \times 4 \times \frac{0.796}{0.71}$$

$$= 3.16 \times 4 \times 1.13$$

$$= 11.23 = 10.1 \text{ dB}$$

3.2.2 INPUT & OUTPUT MATCHING FOR MNA.

For input matching network, we use Γ_S . And for an output matching network, we use Γ_L^* .

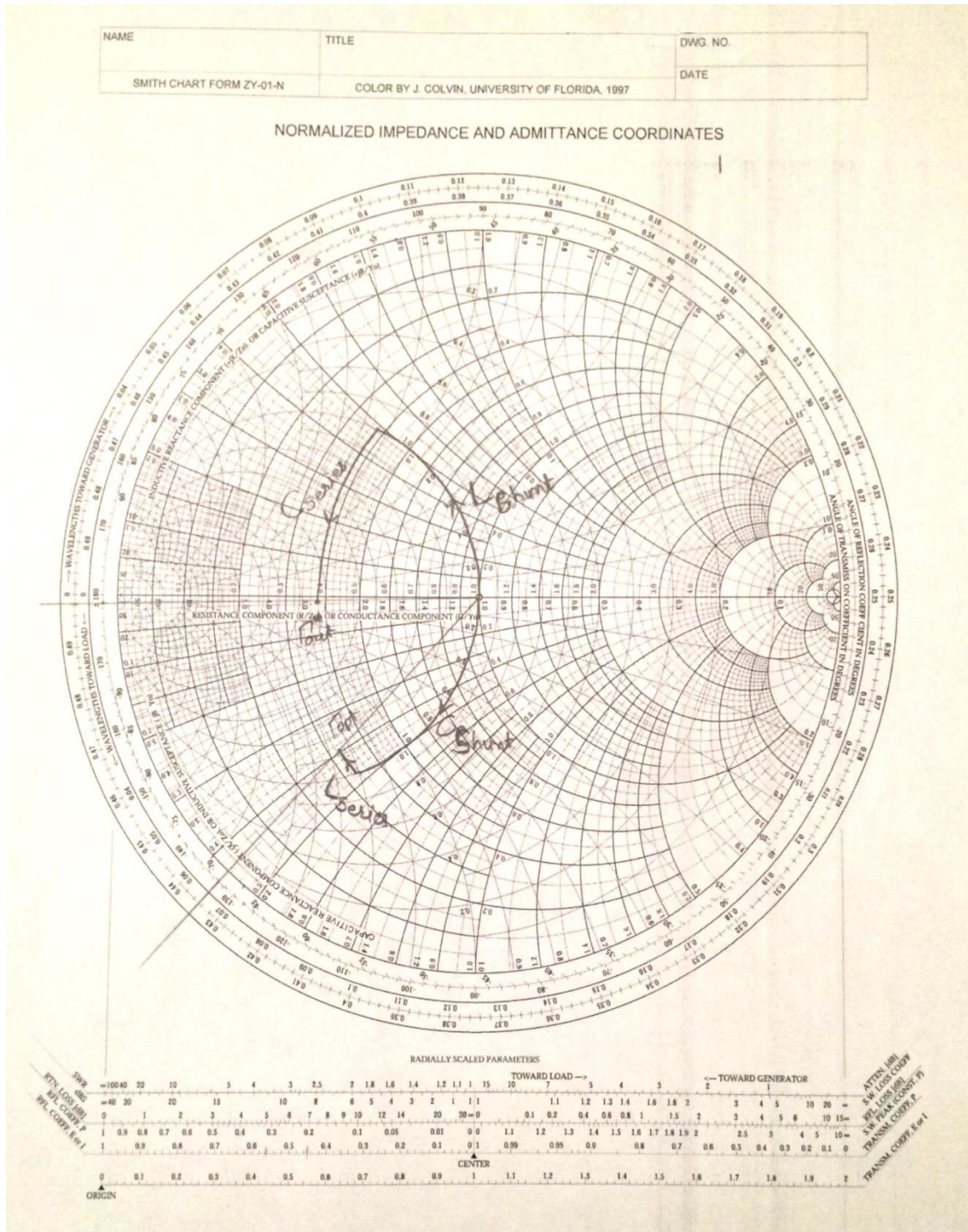


Figure 6 SMITH CHART MATCHING NETWORK FOR MNA

Input matching for MNA:

$$j \omega C_{\text{shunt}} = \frac{j1.42}{50}$$

$$C_s = \frac{j1.42}{2\pi \times 50 \times 17 \times 10^9}$$

$$C_s = 2.6588 \times 10^{-13}$$

$$C_s = 0.26588 \text{ pF}$$

$$j \omega L_{\text{series}} = j0.01 \times 50$$

$$L_s = \frac{0.07 \times 50}{2\pi \times 17 \times 10^9}$$

$$L_s = 3.27 \times 10^{-11}$$

$$L_s = 0.0327 \text{ nH}$$

Output matching for MNA:

$$\frac{1}{j\omega L_{\text{shunt}}} = \frac{-j1.3}{50}$$

$$L_s = \frac{50}{1.3 \times 2\pi \times 17 \times 10^9}$$

$$L_s = 3.6 \times 10^{-10}$$

$$L_s = 0.36 \text{ nH}$$

$$\frac{1}{j\omega C_{\text{series}}} = -j0.5 \times 50$$

$$C_s = \frac{1}{0.5 \times 50 \times 2\pi \times 17 \times 10^9}$$

$$C_s = 3.744 \times 10^{-13}$$

$$C_s = 0.3744 \text{ pf}$$

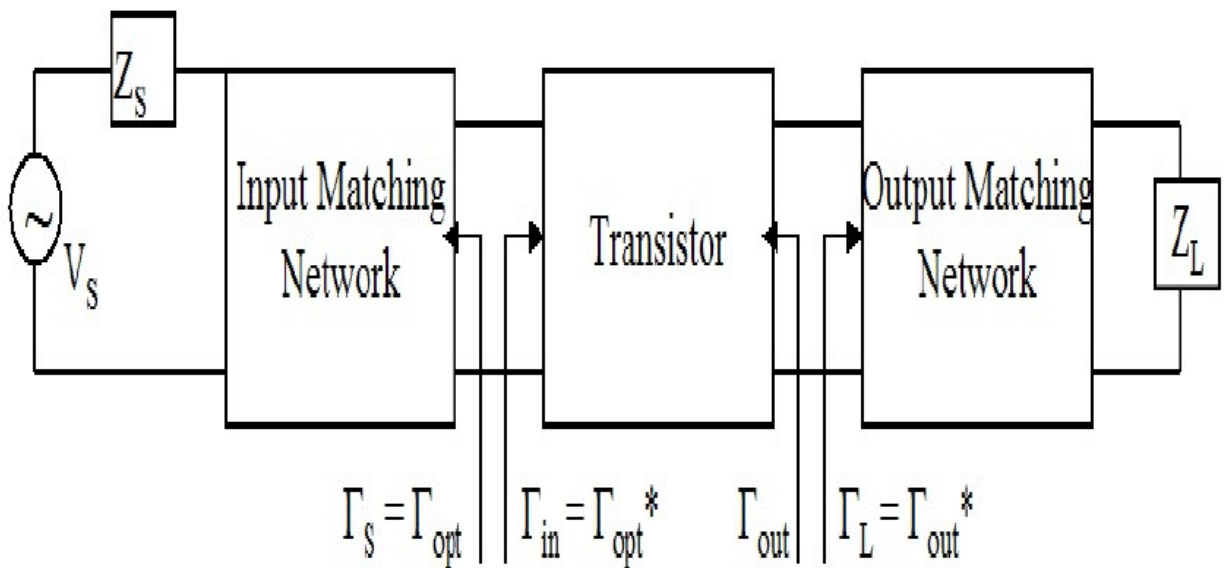


Figure 7 MATCHING NETWORK FOR MNA

3.3 Maximum Gain Amplifier

MGA is a special case of high gain amplifier, used in the second stage of LNA to meet maximum possible gain for the amplifier.

3.3.1 Gain Calculation

$$G_{Tu \max} = G_{s \max} G_o G_{L \max}$$

$$G_{s \max} = \frac{1}{1 - |S_{11}|^2} = 2.777$$

$$G_o = |S_{11}|^2 = 4$$

$$G_{L \max} = \frac{1}{1 - |S_{22}|^2} = 1.14$$

$$G_{Tu \max} = 11 \text{ dB.}$$

Now we have to calculate the noise figure of the Maximum Gain Amplifier

From the data sheet of the transistor we have:

$$r_n = \frac{R_n}{Z_o} = 0.08$$

$$F_{\min} = 1.18 \text{ dB}$$

$$F = F_{\min} + \frac{4r_n N}{|1 + \Gamma_{\text{opt}}|^2}$$

$$N = \frac{|\Gamma_s - \Gamma_{\text{opt}}|^2}{1 - |\Gamma_s|^2}$$

$$\Gamma_s = S_{11}^*$$

$$\Gamma_L = S_{22}^*$$

$$N = \frac{|0.24|^2}{1 - 0.64}$$

$$N = 0.16$$

$$F = 1.3121 + \frac{4(0.08)(0.16)}{1.56}$$

$$F = 1.345 = 1.28\text{dB}$$

3.3.2 Unilateral figure of merit

If the error range is less than $\pm 0.5\text{dB}$, then we can choose the unilateral figure to find the error of the designed amplifier.

By using the formulae:

$$U = \frac{|S_{11}| |S_{21}| |S_{12}| |S_{22}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$

$$= \frac{|0.8| |2| |0.06| |0.35|}{(1 - |0.8|^2)(1 - |0.35|^2)} = \frac{0.0336}{0.316} = 0.106$$

$$\frac{1}{(1+U)^2} = 0.817$$

$$\frac{1}{(1-U)^2} = 1.251$$

$$0.817 < \text{Range} < 1.251$$

$$-0.87 \text{ dB} < R < 0.97 \text{ dB}$$

3.3.3 INPUT & OUTPUT MATCHING FOR MGA

For input matching network, we use Γ_S as conjugate of S_{11}^* . And for an output matching network, we use Γ_L as conjugate of S_{22}^*

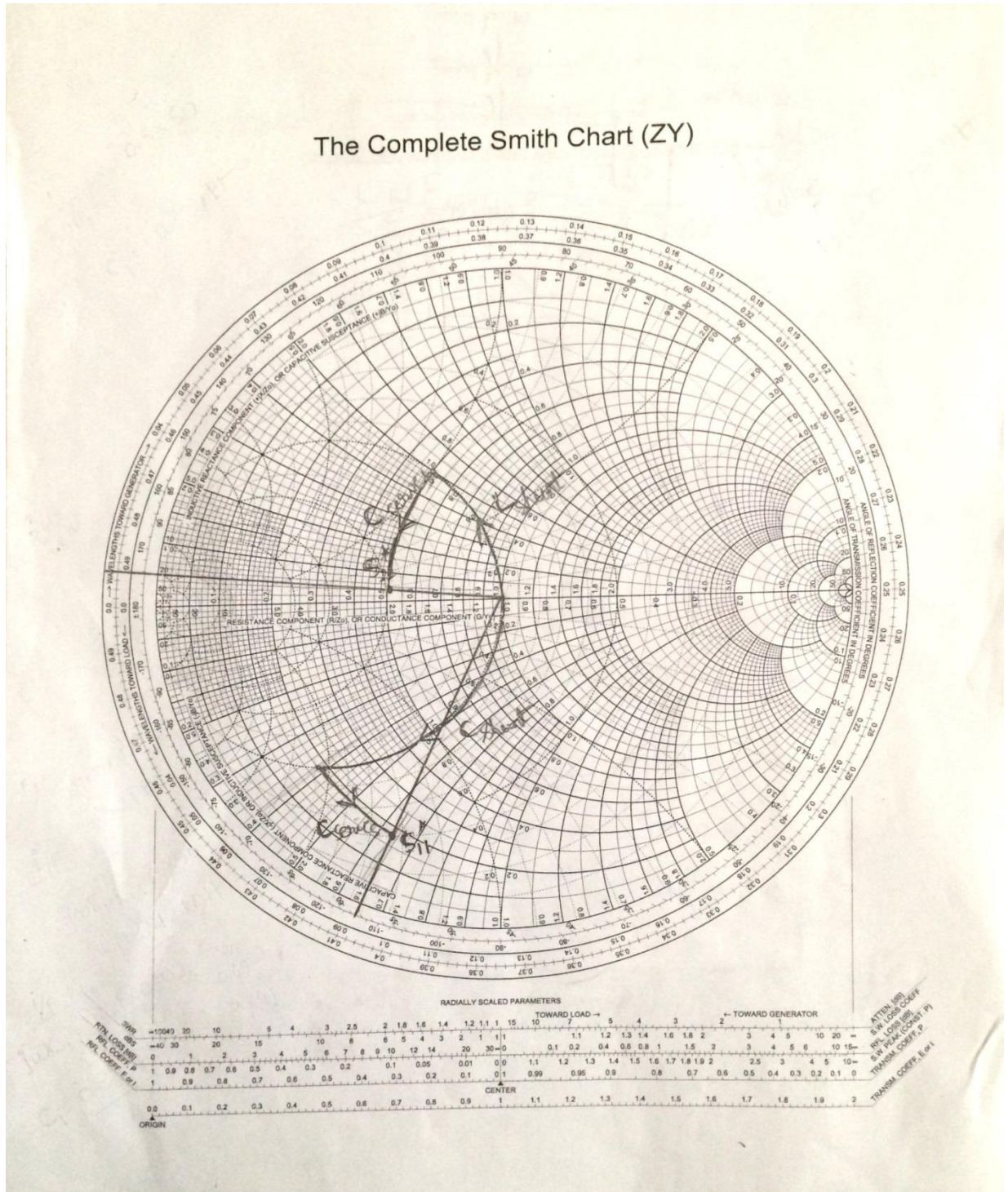


Figure 8 SMITH CHART MATCHING NETWORK FOR MGA

INPUT MATCHING FOR MGA:

$$\frac{1}{j\omega C_{series}} = -j0.036 \times 50$$

$$C_s = \frac{1}{0.036 \times 50 \times 2\pi \times 17 \times 10^9}$$

$$C_s = 5.2 \times 10^{-12}$$

$$C_s = 5.2 \text{ pf}$$

$$j\omega C_{shunt} = \frac{j2.1}{50}$$

$$C_s = \frac{j2.1}{2\pi \times 50 \times 17 \times 10^9}$$

$$= 3.932 \times 10^{-13}$$

$$= 0.393 \text{ pF}$$

OUTPUT MATCHING for MGA:

$$\frac{1}{j\omega C_{series}} = -j0.5 \times 50$$

$$C_s = \frac{1}{0.5 \times 50 \times 2\pi \times 17 \times 10^9}$$

$$C_s = 3.744 \times 10^{-13}$$

$$C_s = 0.3744 \text{ pf}$$

$$\frac{1}{j\omega L_{shunt}} = \frac{j1}{50}$$

$$L_s = \frac{50}{1 \times 2\pi \times 17 \times 10^9}$$

$$L_s = 4.681 \times 10^{-10}$$

$$L_s = 0.468 \text{ nH}$$

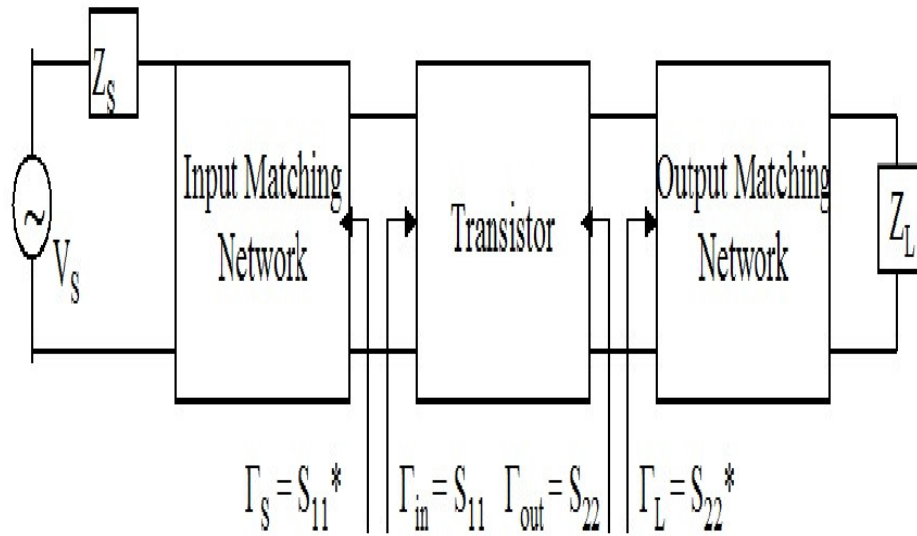


Figure 9 MATCHING NETWORK FOR MGA

3.4 Overall Gain

Overall gain = gain of first stage MNA (dB)+ gain of second stage MGA (dB)

$$= 10.09\text{dB}+11\text{dB}$$

$$=21.09\text{dB}$$

3.5 Noise Figure for Cascaded Amplifier

The overall noise figure of the two stage amplifier calculated as below:

$$F_1 = \text{Noise figure of first stage (MNA)} = 1.3121 = 1.18\text{dB}$$

$$F_2 = \text{Noise figure of second stage (MGA)} = 1.345 = 1.28\text{dB}$$

$$F_{\text{total}}=F_1+\frac{F_2-1}{G_1}=1.3121+\frac{0.345}{10.23}$$

Thus,we have

$$F_{\text{total}} = 1.345=1.28\text{dB}$$

Overall F = 1.28dB.

CHAPTER 4. SIMULATION & RESULTS

4.1 VMMK-1218 Transistor

After a lot of research I have chosen this transistor. We established an E-PHEMT FET from the Avago Technologies using VMMK-1218 transistor. It is an LNA with high gain and low noise design. The transistor is operated at optimal Q point as $V_{DS}=3V$ and $I_{DS}=20\text{ mA}$.

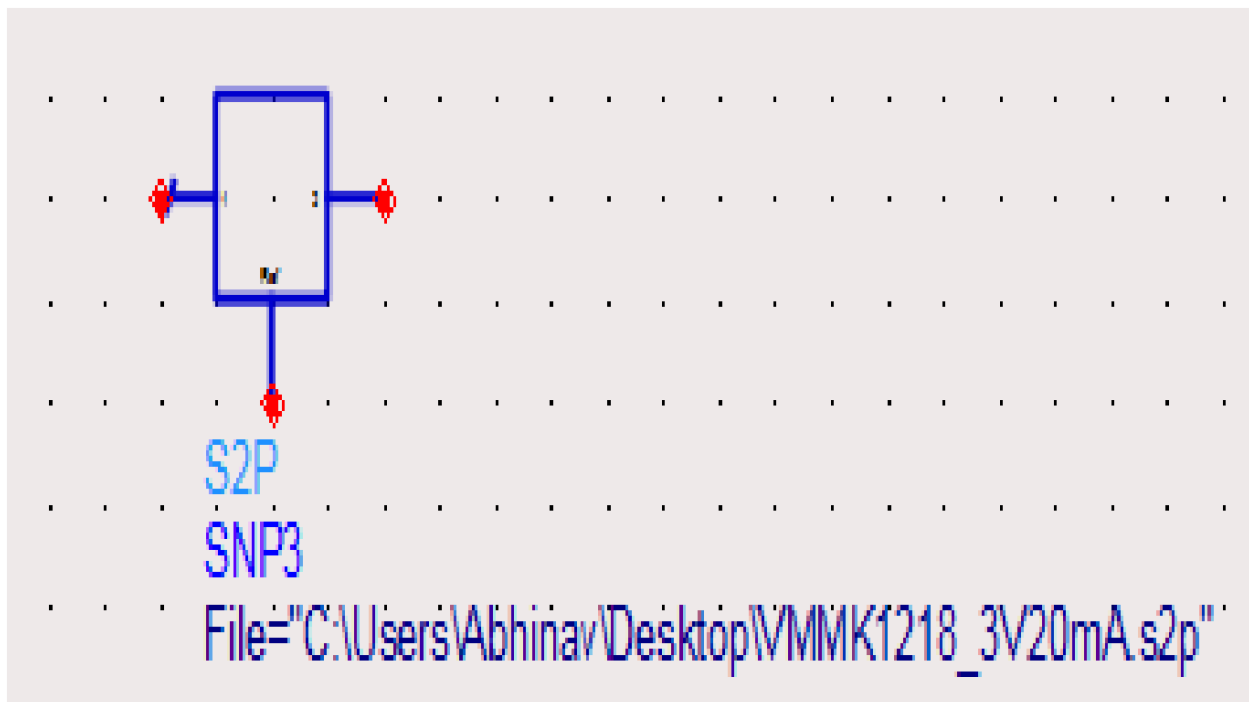


Figure 10 VMMK-1218 TRANSISTOR IN ADS

4.2 First-stage of Minimum Noise Amplifier Design

The first stage of MNA is designed analytically using a Smith chart. Both the input matching and output matching networks consist of inductors and capacitors respectively. The values are calculated analytically using MATLAB and RFMW design essentials. Later it is implemented and verified by using ADS simulation. The calculation of this design must match the simulation result, i.e. NF_{min} should equal to F_{min} and the power gain should be equal to gain calculation.

K and Δ calculations are calculated manually and verified by using MATLAB simulation, which satisfy the stability condition.

The operating temperature of this amplifier design is 16.85°C .

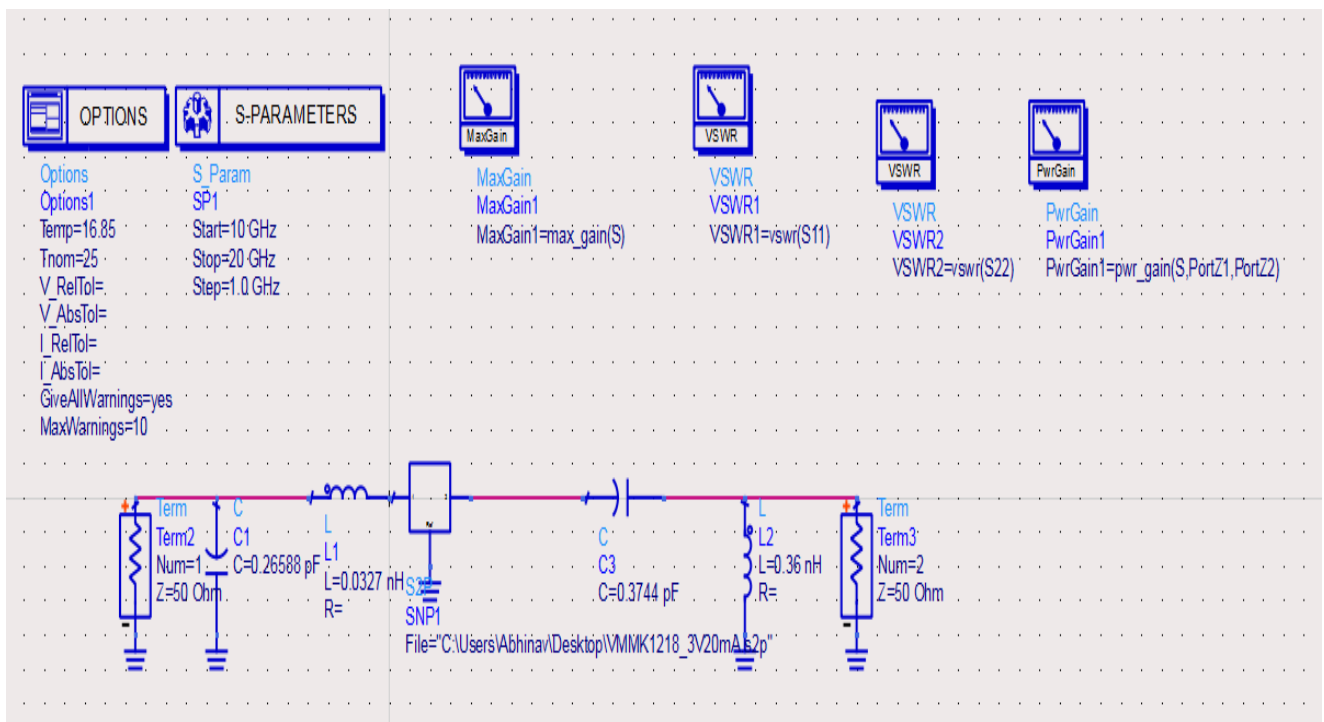


Figure 11 USING ADS, SCHEMATIC OF MNA

4.2.1 Simulation Result for MNA

The simulation output graph gives the gain as 10.01dB, NF_{\min} as 1.180dB and input and output VSWR values as 5.313 and 1.032.

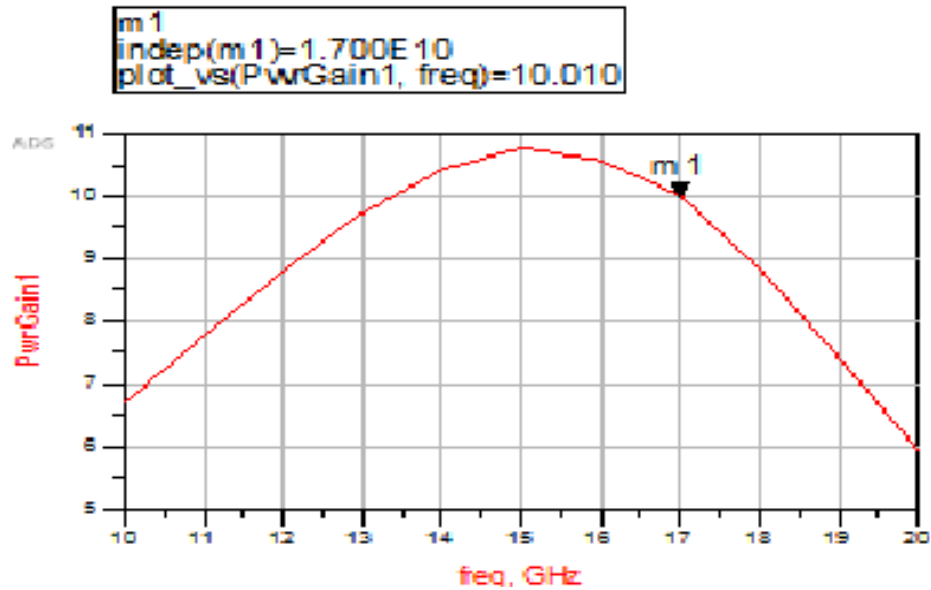


Figure 12 POWER GAIN Vs FREQUENCY MNA

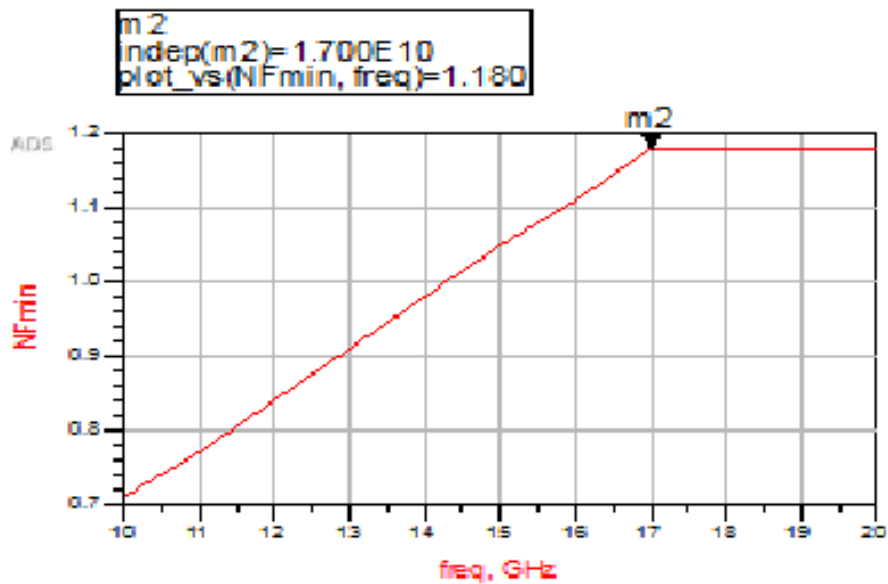


Figure 13 NFmin Vs FREQUENCY MNA

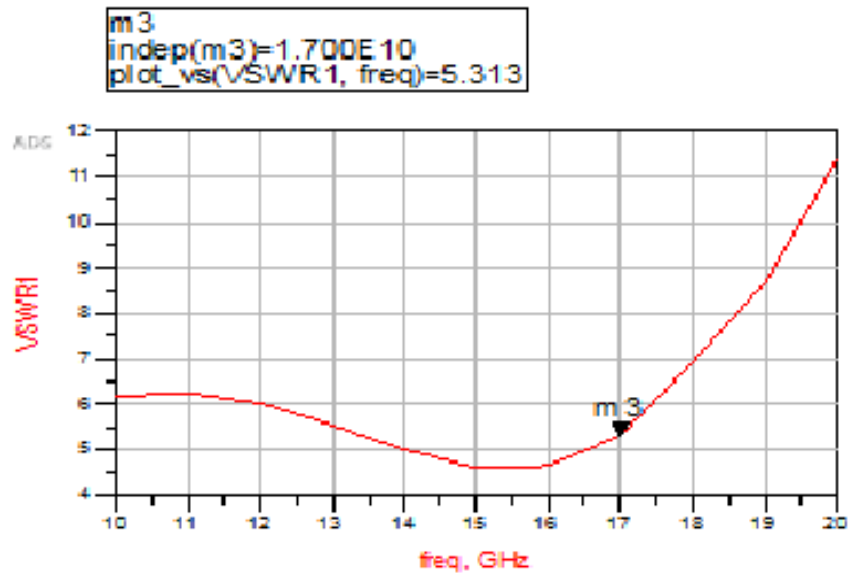


Figure 14 INPUT VSWR Vs FREQUENCY MNA

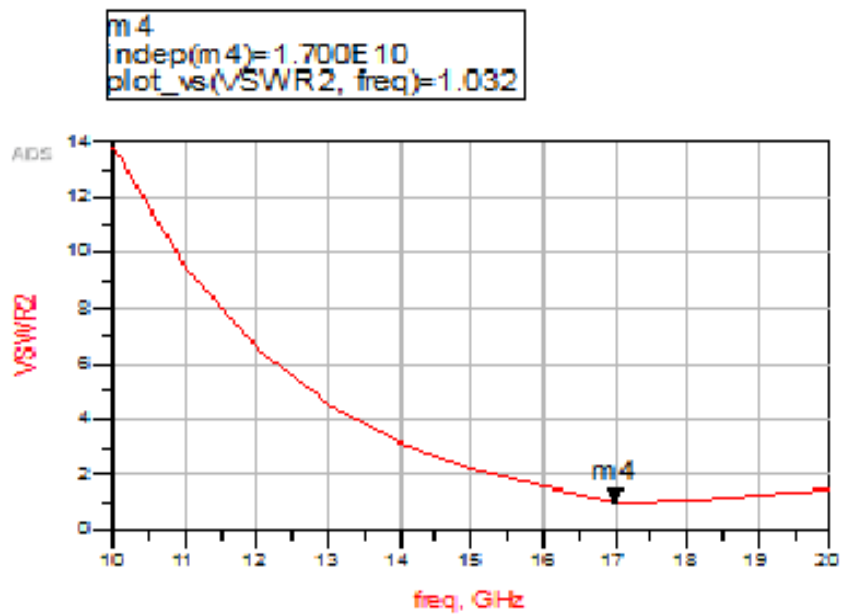


Figure 15 OUTPUT VSWR Vs FREQUENCY MNA

4.3 Second-Stage of Maximum Gain Amplifier

Similarly, the second stage of MGA is designed using smith charts and subsequently implemented by ADS. The calculation of this design almost matches with the simulation result, i.e. the power gain is equal to gain calculation. The design simulation is set to a temperature at 16.85°C.

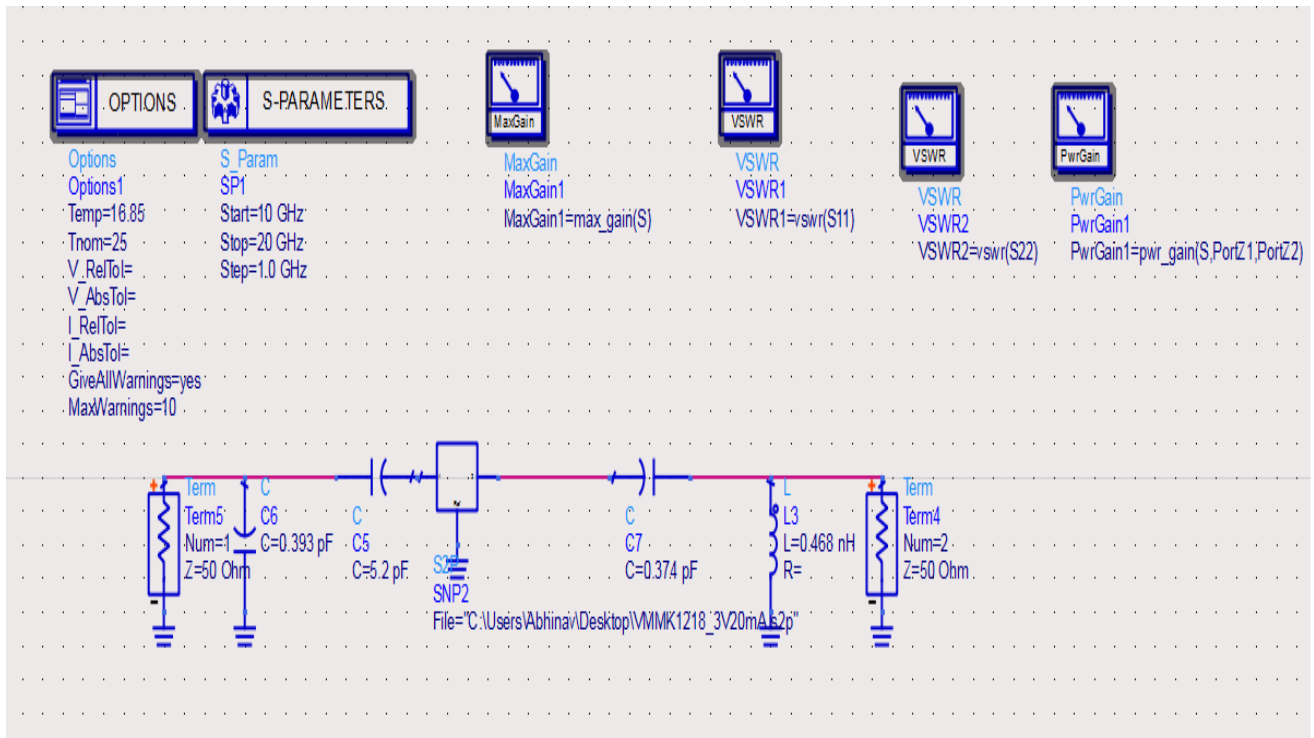


Figure 16 USING ADS, SCHEMATIC OF MGA.

4.3.1 Simulation Result for MGA

The simulation output graph gives the gain as 10.153dB, NF_{min} as 1.180dB and input and output VSWR values as 4.268 and 1.551.

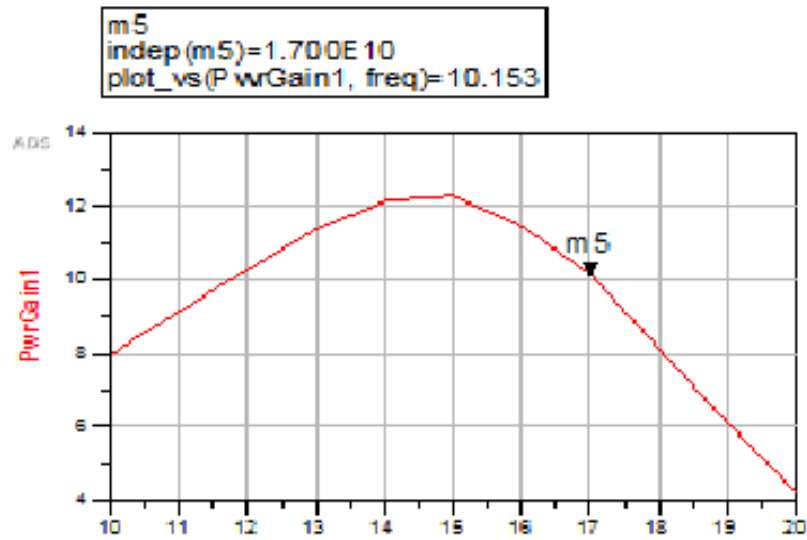


Figure 17 POWER GAIN Vs FREQUENCY MGA

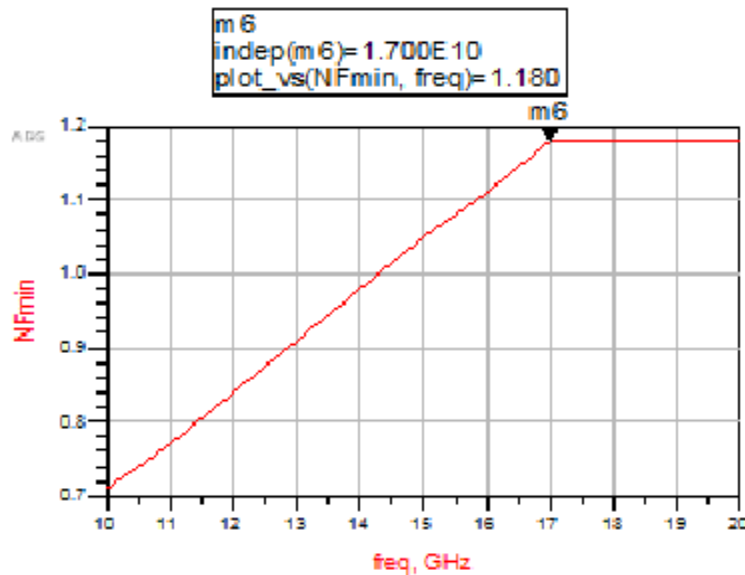


Figure 18 NFmin Vs FREQUENCY MGA

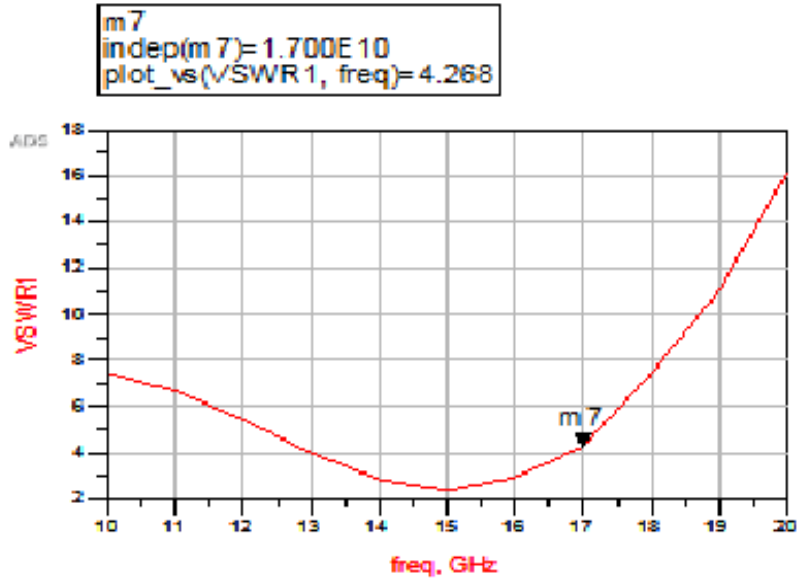


Figure 19 INPUT VSWR Vs FREQUENCY MGA

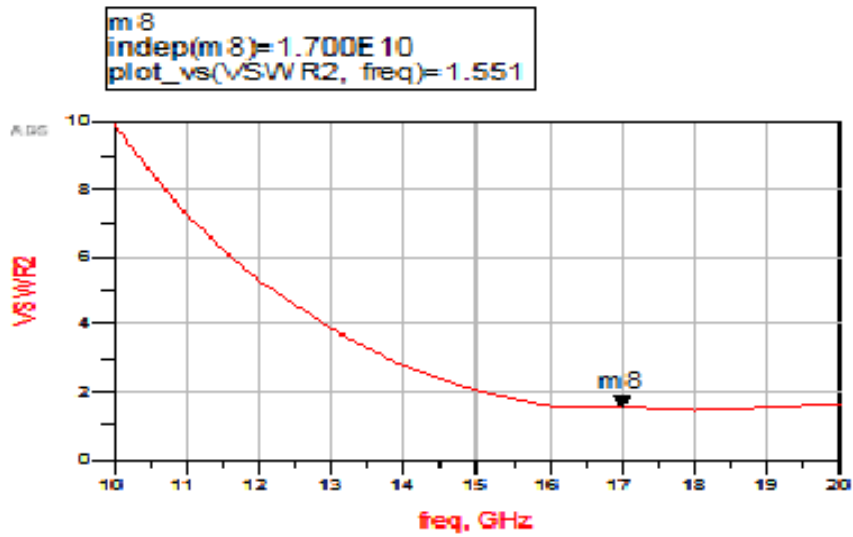


Figure 20 OUTPUT VSWR Vs FREQUENCY MGA

4.4 Cascading Two-Stage Amplifier using ADS

Using ADS, combining the first stage MNA and second stage MGA together and cascading as two stage amplifier design, is done. The design simulation is set to temperature at 16.85°C.

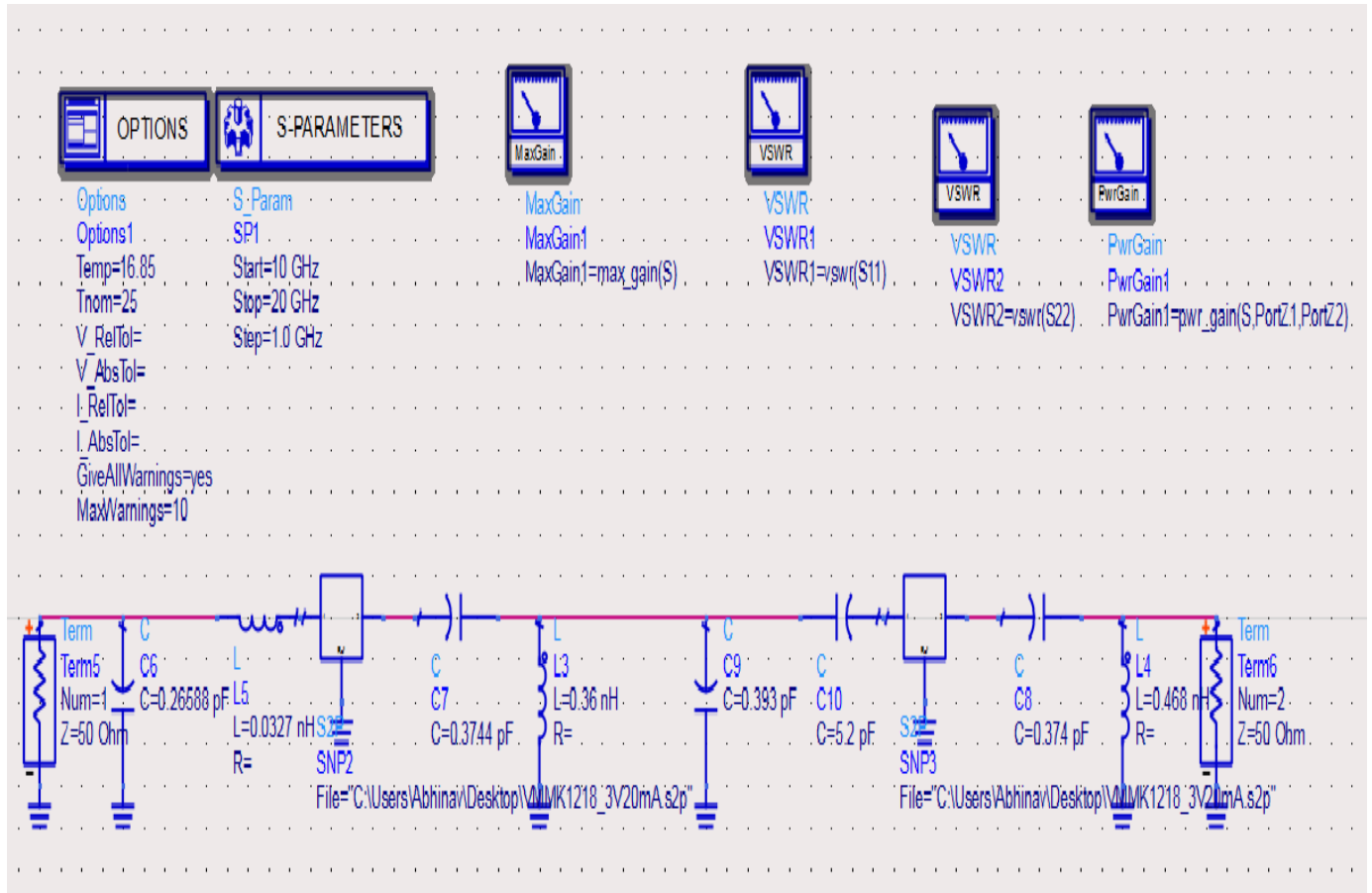


Figure 21 SCHEMATIC OF TWO STAGE AMPLIFIER.

4.4.1 Simulation Result for TWO-STAGE AMPLIFIER

The overall simulation result of cascading the two stage amplifier as the $NF_{min}=1.292$ and overall gain = 20.242 dB.

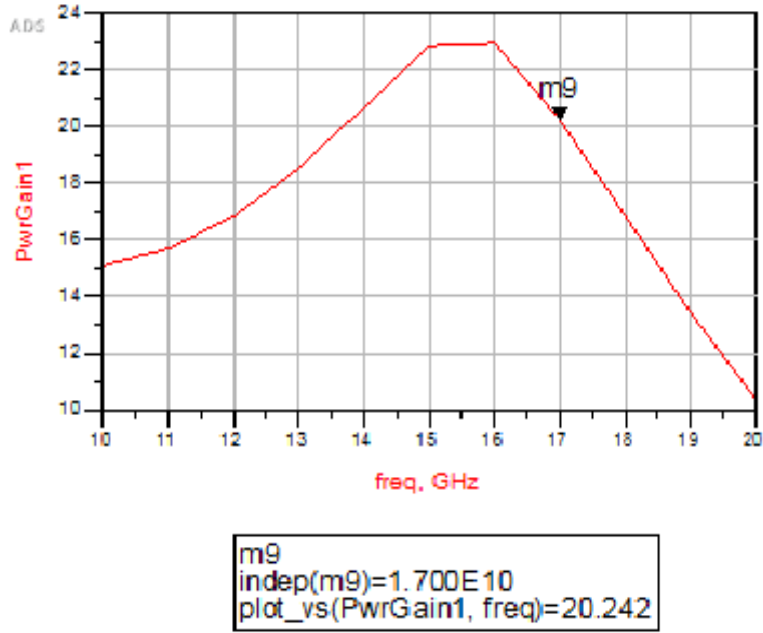


Figure 22 POWER GAIN Vs FREQUENCY LNA

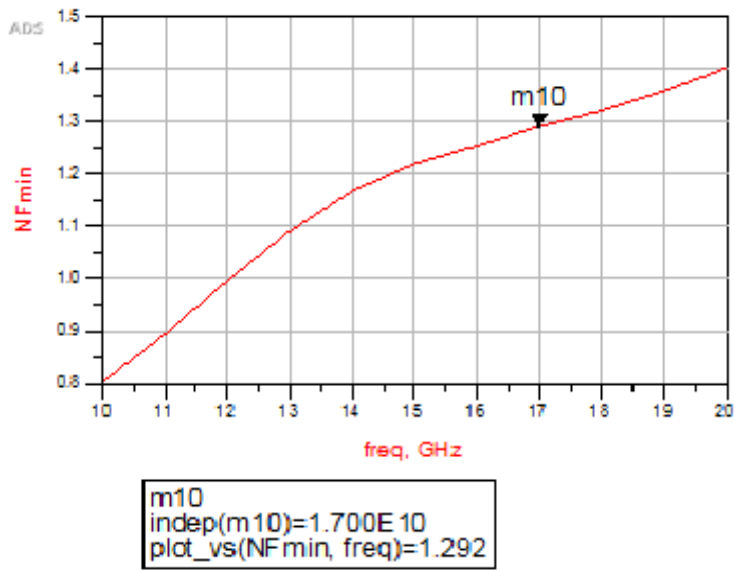
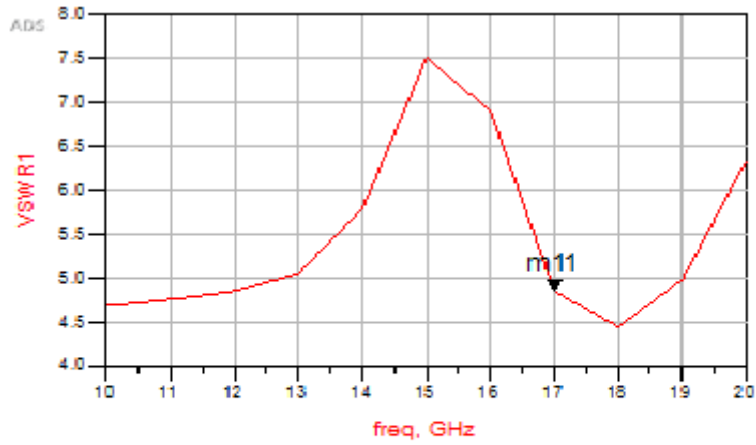


Figure 23 NFmin Vs FREQUENCY LNA

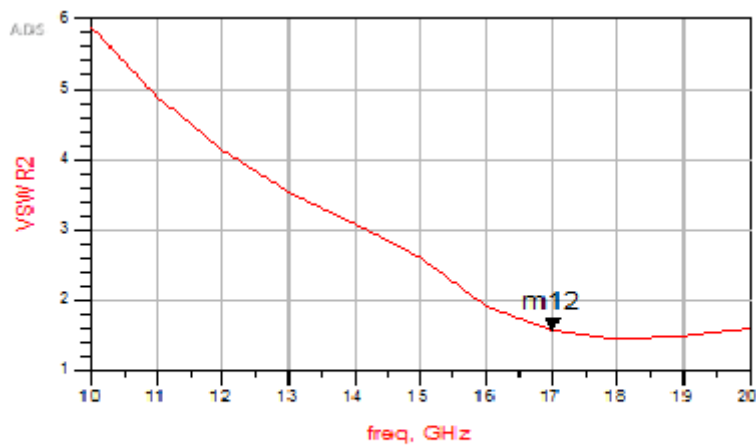


```

m11
indep(m11)=1.700E 10
plot_vs(VSWR1, freq)=4.850

```

Figure 24 INPUT VSWR GAIN Vs FREQUENCY LNA



```

m12
indep(m12)=1.700E 10
plot_vs(VSWR2, freq)=1.564

```

Figure 25 OUTPUT VSWR GAIN Vs FREQUENCY LNA

CHAPTER 5. CONCLUSION

Our two stage amplifier is designed for a gain of 20dB and a noise figure of 2dB. The simulation results indicate that we have received satisfactory results.

The first step of the design is to ensure that the transistor (VMMK-1218) is unconditionally stable at 17 GHz. To realize the low noise amplifier, we have used passive lossless elements for the design of matching networks.

We obtain a noise figure of 1.27 dB which is lower than the specified value and a gain of 21.09dB which is higher than the specified value. This proves that our goals were achieved in a very efficient way.

Specification	Goal	Hand Calucation	MATLAB Simulation	ADS Simulation
Frequency (GHz)	17	17	17	17
Total Gain(dB)	20	21.09	21.03	20.242
Noise Figure (dB)	2	1.28	1.26	1.292

Table 3 OBTAIN VALUES

REFERENCES

1. Radmanesh, Matthew M. *RF & Microwave Design Essentials*. page-590, AuthorHouse, 2007,
2. Radmanesh, Matthew M. *Advanced RF & Microwave Design Essentials*. page-429, AuthorHouse, 2009.
3. Pozar David M. *Microwave Engineering*. Wiley, Page-581, fourth edition 2005.
4. Liao, S.Y. *Microwave Circuit Analysis and Amplifier Design*. Upper Saddle River: Prentice Hall, 1987.
5. Gonzalez, G. *Microwave Transistor Amplifiers: Analysis and Design*, 2nd edition, Upper Saddle River: Prentice Hall.
6. Chang, K. *Microwave Solid-State Circuits and Applications*. New York:John Wiley & Sons, 1994.
7. Carson, R. S. *High –Frequency Amplifiers*. New York: Wiley Interscience, 1975.
8. Bahl, I. and P. Bhartia. *Microwave Solid State Circuit Design*. New York: Wiley Interscience, 1988.
9. Ha, T.T. *Solid-state Microwave Amplifier Design*. New York: John Wiley & Sons,1987.
- 10.http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5967452.
- 11.http://www.ijera.com/papers/Vol2_issue5/DH25647654.pdf
- 12.<http://www.colorado.edu/physics/phys3330/PDF/Experiment7.pdf>

Appendix A: RF/MICROWAVE E-BOOK

Other alternative methods that can be used to verify the calculation by using RF/Microwave E-book by Dr. Matthew Radmanesh.

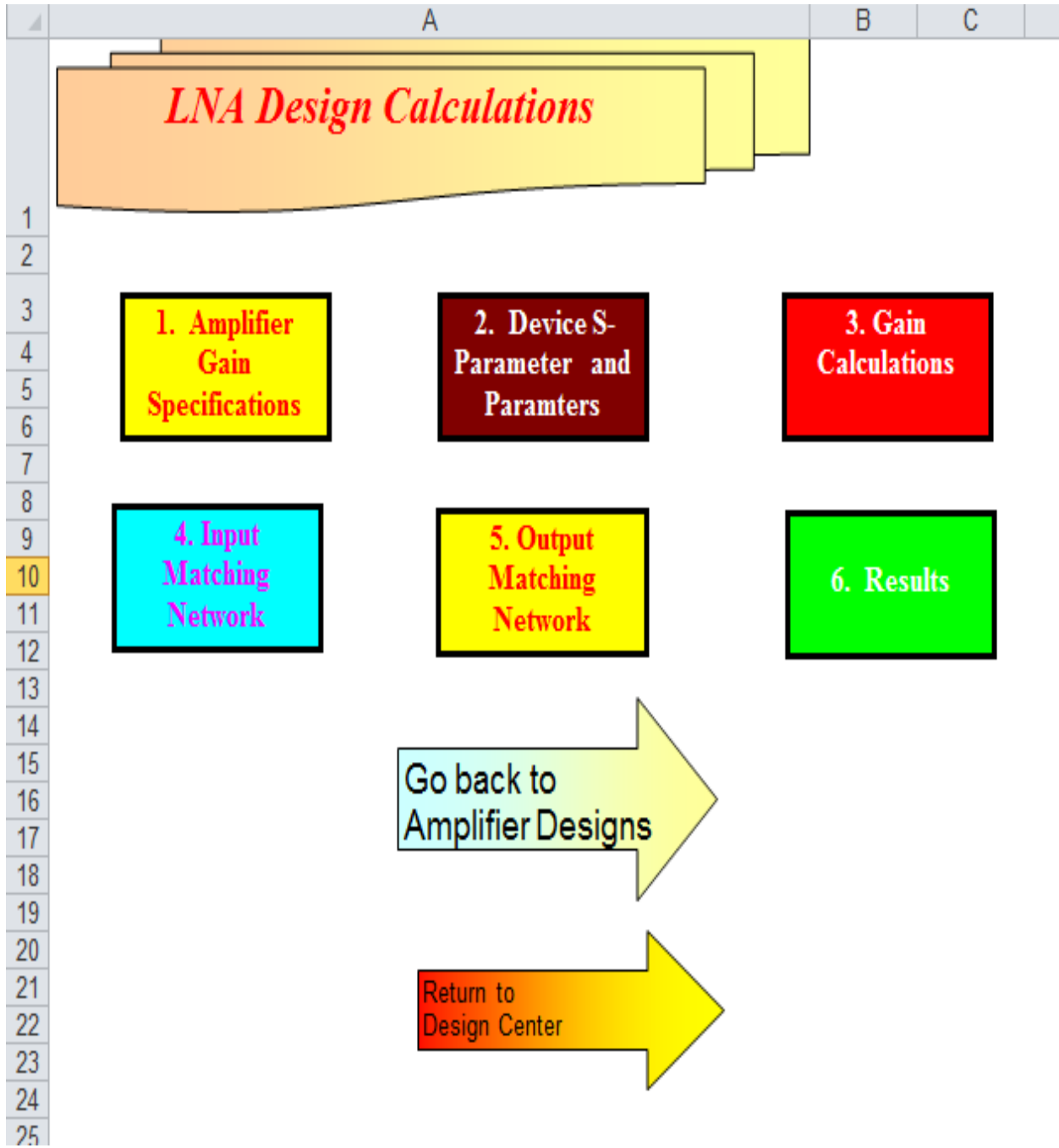


Figure 26 MAIN MENU

Amplifier Required Specifications

INPUT DATA

Enter the Noise Figure Limit	NF	2	dB
Enter the Desired Gain (G) such that $G > G_0$ (dB)	Gain:	20	dB
Enter the Center Frequency	Fc	17	GHz

Return to
Procedure Sheet

Goto Gain Calculation.

Figure 27 SPECIFICATIONS

	A	B	C	D	E	F	G	H	I	J
1	Device S-Parameter and Other Parameters									
2										
3										
4	INPUT DATA									
5	Parameter	Mag.	Angle							
6	S_{11}	0.8	113.8							
7	S_{21}	2	-8.47							
8	S_{12}	0.06	-46.49							
9	S_{22}	0.35	-174.07							
10	Γ_{opt}	0.56	-132.9							
11	Parameter	Value	Unit							
12	F_{min}	1.13	dB							
13	R_n	4	Ohm							
14										
15	SOLUTION:									
16	OUTPUT DATA									
17	$K=1.10$			$K>1$						
18	$\Delta=0.16 \angle -64.1^\circ$			$\Delta<1$						
19										
20	Device is unconditionally stable									
21										
22	Go to Input Matching Network									
23										
24										
25										

Figure 28 STABILITY CHECK USING THE E-BOOK

As the $K>1$ and $\Delta < 1$, It is unconditionally stable

Unilateral Gain Calculations

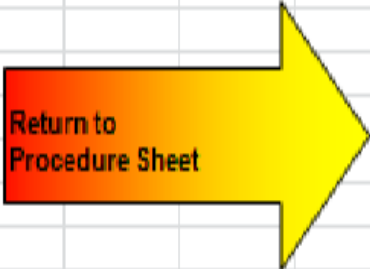
Data from Previous Steps

Parameter	Mag.	Angle
S_{11}	0.8	113.8
S_{21}	2	-8.47
S_{12}	0.06	-46.49
S_{22}	0.35	-174.07

Parameter	dB
Gain ($G_{Desired}$)	20

SOLUTION:

Parameter	dB	Ratio
$G_{s,max}$	2.78	2.78
$G_{L,max}$	1.14	1.14
G_c	4.0	4
G_{total}	11.0	12.7



INPUT DATA

and enter in G_s and G_L

Parameter	dB	Ratio
G_s	3.541	2.26
G_o	6.02	4.00
G_L	0.53	1.13
$(G_s+G_o+G_L)$	10.09	10.21

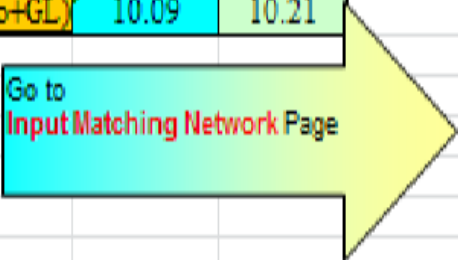


Figure 29 GAIN CALCUCATIONS

Appendix B: MATLAB CODE

```
magS11=input('magS11');

angS11=input('angS11');

magS12=input('magS12');

angS12=input('angleS12');

magS21=input('magS21');

angS21=input('angleS21');

magS22=input('magS22');

angS22=input('angleS22');

magGammaOpt=input('magGammaOpt');

angGammaOpt=input('angGammaOpt');

[f11 g11]=pol2cart(angS11*pi/180,magS11);

S11=f11+g11*i;

[f21 g21]=pol2cart((360+angS21)*pi/180,magS21);

S21=f21+g21*i;

[f12 g12]=pol2cart((360+angS12)*pi/180,magS12);
```

```
S12=f12+g12*i;
```

```
[f22 g22]=pol2cart(angS22*pi/180,magS22);
```

```
S22=f22+g22*i;
```

```
[f g]=pol2cart((360+angGammaOpt)*pi/180,magGammaOpt);
```

```
Gammaopt=f+g*i;
```

```
d= abs(S11*S22-S12*S21)
```

```
x= ['d ',num2str(d)]
```

```
K= (1-abs(S11*S11)-abs(S22*S22)+abs(d*d))/(2*abs(S12*S21));
```

```
x= ['K ',num2str(K)]
```

```
Gammas = Gammaopt;
```

```
x=['Gammas',num2str(Gammas)]
```

```
GammaL=conj(S22+((S12*S21*Gammaopt)/(1-(S11*Gammaopt))));
```

```
x=['GammaL',num2str(GammaL)]
```

```
maxgain= 1/(1-(abs(S11*S11)));
```

```
x=['maxgain',num2str(maxgain)]
```

```
gaindB=10*log10(maxgain);
```

```
x=['gaindB=',num2str(gaindB)]
```

```
Go=(abs(S21*S21));
```

```
x=['g0=',num2str(Go)];
```

```
GodB=10*log10(Go);
```

```
x=['GodB',num2str(GodB)]
```

```
maxG1=1/(1-(abs(S22*S22)));
```

```
x=['output maxgain=',num2str(maxG1)]
```

```
GlindB=10*log10(maxG1);
```

```
x=['gl in dB',num2str(GlindB)]
```

```
Transgain =(gaindB+GodB+GlindB);
```

```
x=['maximum gain=',num2str(Transgain)]
```

Result of MATLAB

magS11 - 0.8

angS11 - 113.7

magS12 - 0.06

angleS12- -46.4

magS21- 2

angleS21 - -8.47

magS22 - 0.35

angleS22- -174.07

magGammaOpt - 0.56

angGammaOpt- -132.9

d =

0.1610

K=

1.0975

Gammas

-0.3812-0.41022i

GammaL

-0.4527-0.0062929i

Gain values

maxgain2.7778

gaindB=4.437

GodB= 6.0206

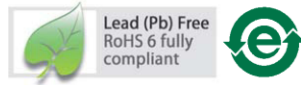
maximum gain=11.0251

Appendix C: Data Sheet

VMMK-1218 0.5 to 18 GHz Low Noise E-PHEMT in a Wafer Scale Package



Data Sheet



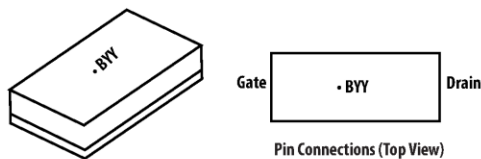
Description

Avago Technologies has combined its industry leading E-pHEMT technology with a revolutionary chip scale package. The VMMK-1218 can produce an LNA with high dynamic range, high gain and low noise figure that generates off of a single position DC power supply. The GaAsCap wafer scale sub-miniature leadless package is small and ultra thin, yet can be handled and placed with standard 0402 pick and place assembly.

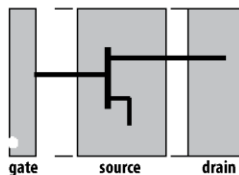
The use of 0.25 micron gates allow a ultra low noise figure (below 1dB from 500 MHz to 12 GHz) with respectable associated gain. With a flat transconductance over bias and frequency the VMMK-1218 provides excellent linearity of over 30 dBm and power over 15 dBm at one dB compression. This product is easy to use since it requires only positive DC voltages for bias and low matching coefficients for simple impedance matching to 50 Ω systems.

The VMMK-1218 is intended for any 500MHz to 18GHz application including 802.11abgn WLAN, WiMax, BWA 802.16 & 802.20 and military applications.

WLP 0402, 1mm x 0.5mm x 0.25 mm



Notes: Top view package marking provides orientation



Notes:
"b" = Device Code
"YY" = Year Code

Features

- Sub-miniature 0402 (1mm x 0.5mm) Surface Mount Leadless Package
- Low height (0.25mm)
- Frequency Range 0.5 to 18 GHz
- Enhancement Mode [1]
- 0.25 micron gate width
- Tape and Reel packaging option available
- Point MTTF > 300 years at 120°C channel temperature

Specifications

- 0.7 dB Fmin
- 9.0 dB Ga
- +22 dBm output 3rd order intercept
- +12 dBm output power

Applications

- Low Noise and Driver for Cellular/PCS and WCDMA Base Stations
- 2.4 GHz, 3.5GHz, 5-6GHz WLAN and WiMax notebook computer, access point and mobile wireless applications
- DBS 10 to 13 GHz receivers
- VSAT and SATCOM 13 to 18 GHz systems
- 802.16 & 802.20 BWA systems
- WLL and MMDS Transceivers
- General purpose discrete E-pHEMT for other ultra low noise applications

Notes:

1. The Avago enhancement mode pHEMT devices do not require a negative gate bias voltage as they are "normally off". They can help simplify the design and reduce the cost of receivers and transmitters in many applications from 500 MHz to 18 GHz



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 20 V (class A)
ESD Human Body Model = 100 V (Class 0)
Refer to Avago Application Note A004R:
Electrostatic Discharge, Damage and Control.

VMMK-1218 Absolute Maximum Ratings

Sym	Parameters/Condition	Unit	Max
Vds	Drain-Source Voltage ^[2]	V	5
Vgs	Gate-Source Voltage ^[2]	V	-5 to 1
Vgd	Gate-Drain Voltage ^[2]	V	-5 to 1
Ids	Drain Current ^[2]	mA	100
Igs	Gate Current	mA	1.6
Pdn	Total Power Dissipation ^[3]	mW	300
Pin	RF CW Input Power Max	dBm	10
Tch	Max channel temperature	C	+150
θjc	Thermal Resistance ^[4]	C/W	200

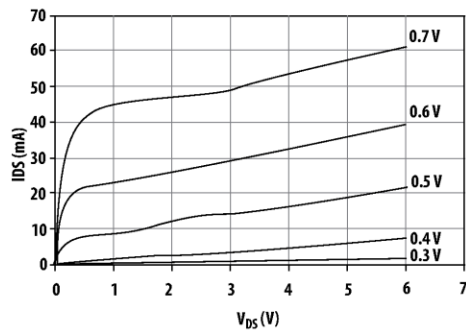


Figure 1. Typical I-V Curves. (VGS=0.1 V per step)

Notes:

1. Operation in excess of any of these conditions may result in permanent damage to this device.
2. Assumes DC quiescent conditions
3. Ambient operational temperature $T_A=25^\circ\text{C}$ unless noted.
4. Thermal resistance measured using 150°C Liquid Crystal Measurement Method
5. The device can handle + 10dBm RF input power provided I_{gs} is limited to 1ma

VMMK-1218 RF Specifications (on board) ^[6,7]

$T_A = 25^\circ\text{C}$, Freq = 10 GHz, Vds = 3V, Ids = 20mA, Zo = 50 Ω (unless otherwise specified)

Sym	Parameters/Condition	Units	Min	Typ.	Max
Vgs	Gate Voltage	V	0.48	0.58	0.68
Igs	Gate Current	uA		0.4	
Gm	Transconductance	mS		200	
Ga	Associated Gain	dB	6.7	9	10.2
NF	Noise Figure	dB		0.81	1.5
Fmin	Noise Figure min	dB		0.71	
P-1dB	1dB Compressed Output Power	dBm		+12	
OIP3	Output 3 rd Order Intercept Point	dBm		+22	

Notes:

6. Specifications are derived from measurements in a test circuit.
7. All tested parameters guaranteed with measurement accuracy $\pm 0.5\text{dB}$ for gain.

Product Consistency Distribution Charts [1]

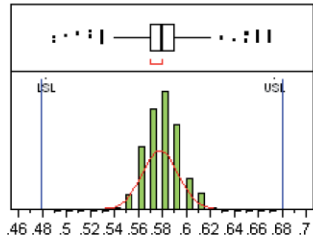


Figure 2. Gate Voltage @ $V_{ds} = 3V$ & $I_{ds} = 20mA$, LSL=0.48, Nominal=0.58, USL=0.68, CPK=2.2

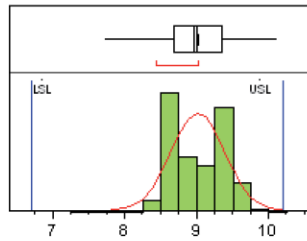


Figure 3. Gain @ 10 GHz, LSL=6.7, Nominal=9.0, USL=10.2, CPK=1.1

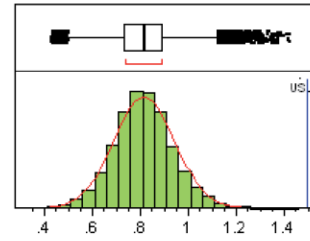


Figure 4. NF @ 10 GHz, Nominal=0.81, USL=1.50, CPK=1.8

Note:

1. Distribution data based at least 500 part sample size from two wafers during initial characterization of this product. Future wafers allocated to this product may have nominal values anywhere between upper and lower limits.

VMMK-1218 Typical Performance Curve

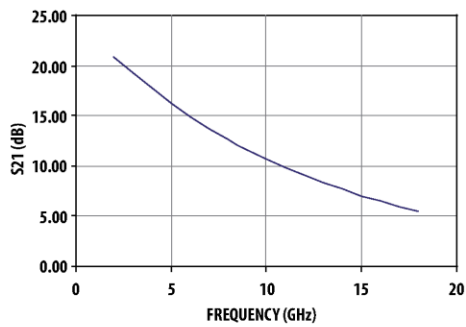


Figure 5. S21 vs. Frequency at 2V, 20mA

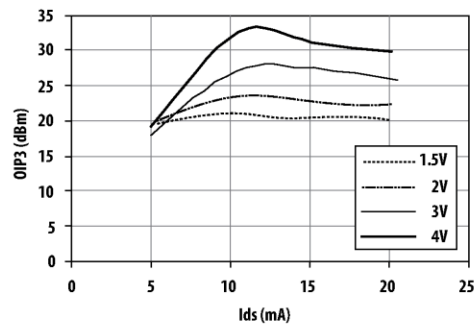


Figure 6. OIP3 vs. Ids at 10 GHz ($Z_i = Z_o = 50\Omega$)

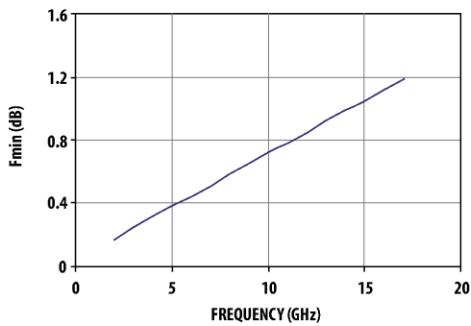


Figure 7. Fmin vs. Frequency at 2V, 20mA

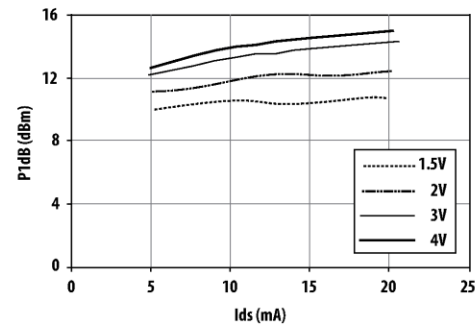


Figure 8. P1dB vs. Ids at 10 GHz ($Z_i = Z_o = 50\Omega$)

VMMK-1218 Typical Performance Curve

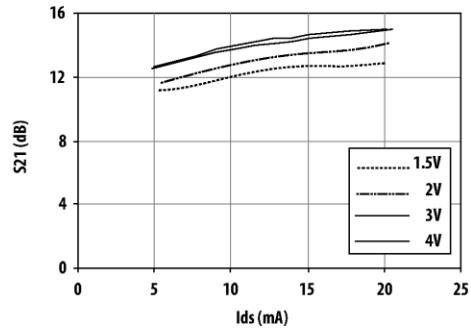


Figure 9. Gain vs. Ids at 10 GHz

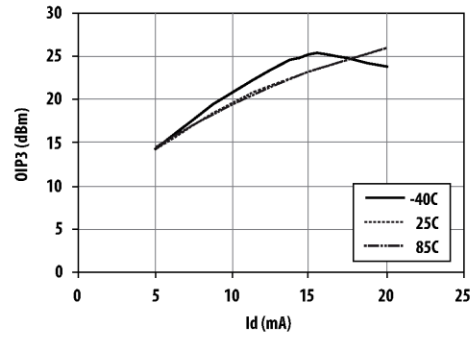


Figure 10. OIP3 vs. Ids at 2V over temperature at 10 GHz

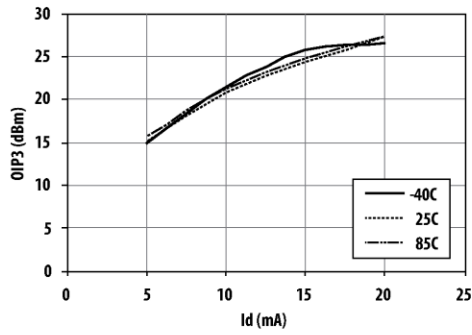


Figure 11. OIP3 vs. Ids at 3V over temperature at 10 GHz

VMMK-1218 Typical Scattering Parameters and Noise Parameters, $T_A=25^\circ\text{C}$, $V_{ds}=2\text{V}$, $I_{ds}=20\text{mA}$ [1]

Freq GHz	S11			S21		S12		S22		MSG/MAG
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
2	0.89	-78.16	20.92	11.12	129.71	0.06	44.50	0.54	-55.65	29.35
3	0.85	-106.33	19.31	9.23	112.05	0.07	29.40	0.47	-76.55	25.87
4	0.81	-128.95	17.70	7.68	97.65	0.08	17.41	0.41	-94.12	23.11
5	0.79	-146.66	16.25	6.49	85.78	0.08	7.80	0.37	-108.21	21.15
6	0.78	-161.38	14.93	5.58	75.40	0.09	-0.22	0.34	-120.69	19.57
7	0.78	-173.77	13.74	4.86	66.04	0.09	-7.10	0.32	-131.78	18.21
8	0.77	175.63	12.65	4.29	57.40	0.09	-13.35	0.31	-141.77	17.06
9	0.77	166.49	11.64	3.82	49.36	0.09	-18.82	0.31	-151.17	16.03
10	0.78	158.16	10.71	3.43	41.75	0.08	-24.10	0.30	-159.09	15.12
11	0.78	150.76	9.87	3.12	34.59	0.08	-28.99	0.31	-166.30	14.31
12	0.78	143.93	9.09	2.85	27.60	0.08	-33.20	0.31	-173.04	13.61
13	0.78	137.52	8.38	2.62	20.89	0.08	-37.50	0.32	-179.45	12.97
14	0.79	131.39	7.71	2.43	14.43	0.08	-41.46	0.32	-174.80	12.39
15	0.79	125.61	7.11	2.27	8.03	0.08	-45.30	0.33	-169.68	11.86
16	0.79	119.69	6.53	2.12	1.59	0.07	-49.20	0.34	-164.86	11.37
17	0.80	113.87	6.01	2.00	-4.80	0.07	-52.04	0.35	-160.03	10.95
18	0.80	108.30	5.50	1.88	-10.80	0.07	-55.52	0.36	-155.48	10.54

Typical Noise Parameters

Freq GHz	Fmin	Γ opt	Γ opt	Rn/50	Ga
	dB	Mag.	Ang.		dB
2	0.17	0.727	30.9	0.1	20.9
3	0.24	0.624	46.2	0.1	19.16
4	0.31	0.534	61.1	0.09	17.57
5	0.38	0.457	75.8	0.08	16.12
6	0.44	0.394	90.1	0.08	14.83
7	0.51	0.344	104.1	0.07	13.69
8	0.58	0.307	117.8	0.07	12.69
9	0.65	0.283	131.2	0.06	11.84
10	0.72	0.273	144.3	0.06	11.14
11	0.78	0.276	157.1	0.06	10.59
12	0.85	0.292	169.6	0.06	10.19
13	0.92	0.322	-178.2	0.06	9.94
14	0.99	0.365	-166.3	0.06	9.83
15	1.05	0.421	-154.8	0.06	9.87
16	1.12	0.49	-143.5	0.07	10.07
17	1.19	0.573	-132.6	0.08	10.41

Note:

1. S-parameters are measured in 50 Ohm test environment.

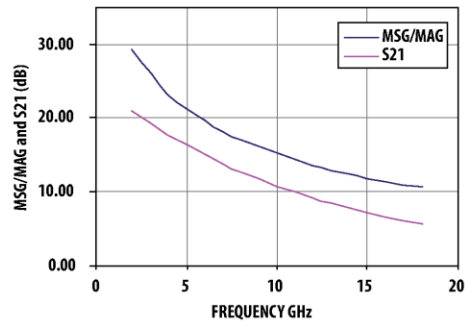


Figure 12. MSG/MAG and S21 vs. Frequency at 2V 20 mA

VMMK-1218 Typical Scattering Parameters and Noise Parameters, $T_A=25^\circ\text{C}$, $V_{ds}=1.5\text{V}$, $I_{ds}=20\text{mA}$ [1]

Freq GHz	S11			S21		S12		S22		MSG/MAG
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
2	0.89	-78.70	20.79	10.95	129.60	0.07	44.02	0.52	-63.66	28.91
3	0.84	-106.97	19.15	9.07	111.99	0.08	28.78	0.46	-87.65	25.57
4	0.80	-129.59	17.52	7.52	97.71	0.09	16.70	0.42	-107.45	22.87
5	0.79	-147.25	16.06	6.35	86.00	0.09	7.26	0.39	-123.04	20.94
6	0.78	-161.95	14.74	5.46	75.76	0.10	-1.08	0.37	-136.55	19.39
7	0.77	-174.30	13.53	4.75	66.54	0.10	-7.98	0.36	-148.06	18.04
8	0.77	175.11	12.45	4.19	58.04	0.10	-14.20	0.35	-158.27	16.90
9	0.77	165.97	11.42	3.72	50.15	0.09	-19.91	0.35	-167.52	15.86
10	0.77	157.70	10.49	3.35	42.68	0.09	-25.19	0.35	-175.45	14.95
11	0.77	150.33	9.65	3.04	35.68	0.09	-30.03	0.35	177.45	14.14
12	0.77	143.54	8.87	2.78	28.84	0.09	-34.60	0.36	171.04	13.44
13	0.78	137.15	8.15	2.56	22.27	0.09	-38.83	0.36	164.96	12.80
14	0.78	131.00	7.49	2.37	15.98	0.09	-43.10	0.37	159.55	12.22
15	0.78	125.21	6.88	2.21	9.72	0.08	-47.12	0.37	154.60	11.66
16	0.79	119.39	6.31	2.07	3.42	0.08	-51.06	0.38	150.08	11.18
17	0.79	113.54	5.80	1.95	-2.83	0.08	-54.94	0.39	145.54	10.75
18	0.79	107.95	5.29	1.84	-8.68	0.08	-58.30	0.40	141.40	10.32

Typical Noise Parameters

Freq GHz	Fmin dB	Γ_{opt} Mag.	Γ_{opt} Ang.	Rn/50	Ga dB
2	0.16	0.717	32.4	0.10	21.86
3	0.24	0.620	48.1	0.10	19.89
4	0.31	0.536	63.5	0.09	18.08
5	0.39	0.464	78.4	0.08	16.45
6	0.47	0.405	93.0	0.08	14.99
7	0.55	0.359	107.1	0.07	13.70
8	0.63	0.326	120.7	0.06	12.59
9	0.70	0.305	134.0	0.06	11.64
10	0.78	0.297	146.9	0.06	10.87
11	0.86	0.302	159.3	0.06	10.27
12	0.94	0.319	171.3	0.05	9.84
13	1.02	0.349	-177.1	0.05	9.59
14	1.09	0.392	-165.9	0.05	9.51
15	1.17	0.447	-155.1	0.05	9.59
16	1.25	0.515	-144.8	0.06	9.85
17	1.33	0.596	-134.8	0.08	10.29

Note:

1. S-parameters are measured in 50 Ohm test environment.

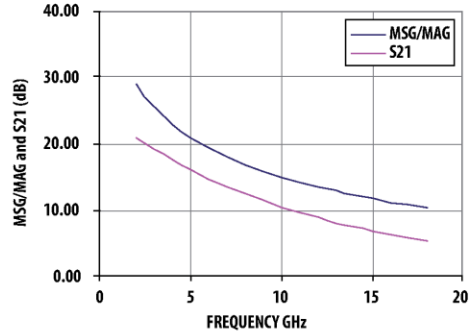


Figure 13. MSG/MAG and S21 vs. Frequency at 1.5V 20 mA

VMMK-1218 Typical Scattering Parameters and Noise Parameters, $T_A=25^\circ\text{C}$, $V_{ds}=3\text{V}$, $I_{ds}=20\text{mA}$ [1]

Freq GHz	S11			S21		S12		S22		MSG/MAG
	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	dB
2	0.90	-78.41	20.88	11.07	129.30	0.05	44.78	0.59	-45.41	29.71
3	0.85	-106.62	19.27	9.19	111.50	0.06	29.68	0.50	-61.56	26.11
4	0.82	-129.23	17.67	7.65	96.89	0.07	17.84	0.43	-74.78	23.29
5	0.80	-146.90	16.21	6.47	84.82	0.07	8.51	0.38	-85.37	21.29
6	0.79	-161.57	14.90	5.56	74.28	0.07	0.60	0.35	-94.96	19.70
7	0.78	-173.94	13.71	4.85	64.67	0.07	-6.02	0.32	-103.77	18.32
8	0.78	175.49	12.63	4.28	55.85	0.07	-12.05	0.31	-112.18	17.17
9	0.78	166.35	11.62	3.81	47.60	0.07	-17.59	0.30	-120.67	16.14
10	0.78	158.10	10.70	3.43	39.76	0.07	-22.09	0.29	-128.21	15.23
11	0.79	150.68	9.87	3.11	32.39	0.07	-26.72	0.29	-135.58	14.44
12	0.79	143.93	9.09	2.85	25.16	0.07	-30.99	0.30	-142.88	13.76
13	0.79	137.47	8.38	2.62	18.21	0.07	-34.81	0.31	-149.97	13.11
14	0.80	131.33	7.71	2.43	11.48	0.06	-38.24	0.31	-156.46	12.54
15	0.80	125.54	7.11	2.27	4.87	0.06	-40.97	0.33	-162.44	12.02
16	0.80	119.64	6.53	2.12	-1.87	0.06	-44.55	0.34	-168.20	11.55
17	0.81	113.80	6.00	2.00	-8.47	0.06	-46.49	0.35	-174.07	11.14
18	0.81	108.24	5.48	1.88	-14.69	0.06	-49.45	0.36	-179.63	10.72

Typical Noise Parameters

Freq GHz	Fmin dB	Γ_{opt} Mag.	Γ_{opt} Ang.	Rn/50	Ga dB
2	0.16	0.72	30.40	0.10	20.29
3	0.23	0.62	45.50	0.10	18.62
4	0.30	0.53	60.30	0.09	17.08
5	0.37	0.45	74.80	0.08	15.69
6	0.44	0.39	89.10	0.08	14.44
7	0.50	0.34	103.00	0.07	13.34
8	0.57	0.30	116.70	0.07	12.37
9	0.64	0.28	130.10	0.07	11.55
10	0.71	0.27	143.20	0.06	10.87
11	0.77	0.27	156.00	0.06	10.34
12	0.84	0.29	168.60	0.06	9.95
13	0.91	0.31	-179.20	0.06	9.70
14	0.98	0.36	-167.20	0.06	9.59
15	1.05	0.41	-155.50	0.06	9.63
16	1.11	0.48	-144.10	0.07	9.81
17	1.18	0.56	-132.90	0.08	10.13

Note:

- S-parameters are measured in 50 Ohm test environment.

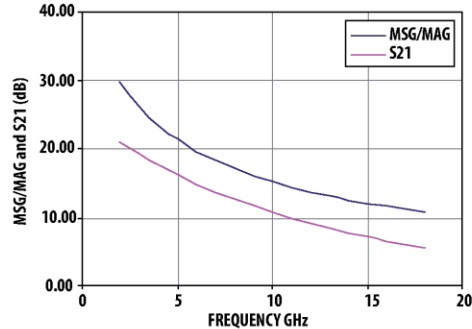


Figure 14. MSG/MAG and S21 vs. Frequency at 3V 20 mA

Small Signal Model Parameters

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Vd (V)	1.5	Vd (V)	1.5	Vd (V)	1.5	Vd (V)	1.5
Id (mA)	5	Id (mA)	10	Id (mA)	15	Id (mA)	20
Gm	0.1162	Gm	0.2019	Gm	0.2374	Gm	0.3249
tau	0.00188	tau	0.002388	tau	0.002702	tau	0.00271
Cgs	0.5131	Cgs	0.6732	Cgs	0.8077	Cgs	0.929
Rgs	0.2126	Rgs	0.02638	Rgs	0.02069	Rgs	0.0304
Cgd	0.06932	Cgd	0.06226	Cgd	0.0777	Cgd	0.07133
Cds	0.1587	Cds	0.1574	Cds	0.1606	Cds	0.1597
Rds	334.70	Rds	187.10	Rds	154.10	Rds	123.80

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Vd (V)	2	Vd (V)	2	Vd (V)	2	Vd (V)	2
Id (mA)	5	Id (mA)	10	Id (mA)	15	Id (mA)	20
Gm	0.1159	Gm	0.1992	Gm	0.1992	Gm	0.3199
tau	0.002146	tau	0.002394	tau	0.002394	tau	0.00257
Cgs	0.5661	Cgs	0.7445	Cgs	0.7445	Cgs	1.04381
Rgs	0.2293	Rgs	0.01936	Rgs	0.01936	Rgs	0.01756
Cgd	0.07976	Cgd	0.0726	Cgd	0.0726	Cgd	0.0606
Cds	0.1631	Cds	0.16078	Cds	0.16078	Cds	0.1607
Rds	357.50	Rds	222.00	Rds	222.00	Rds	141.70

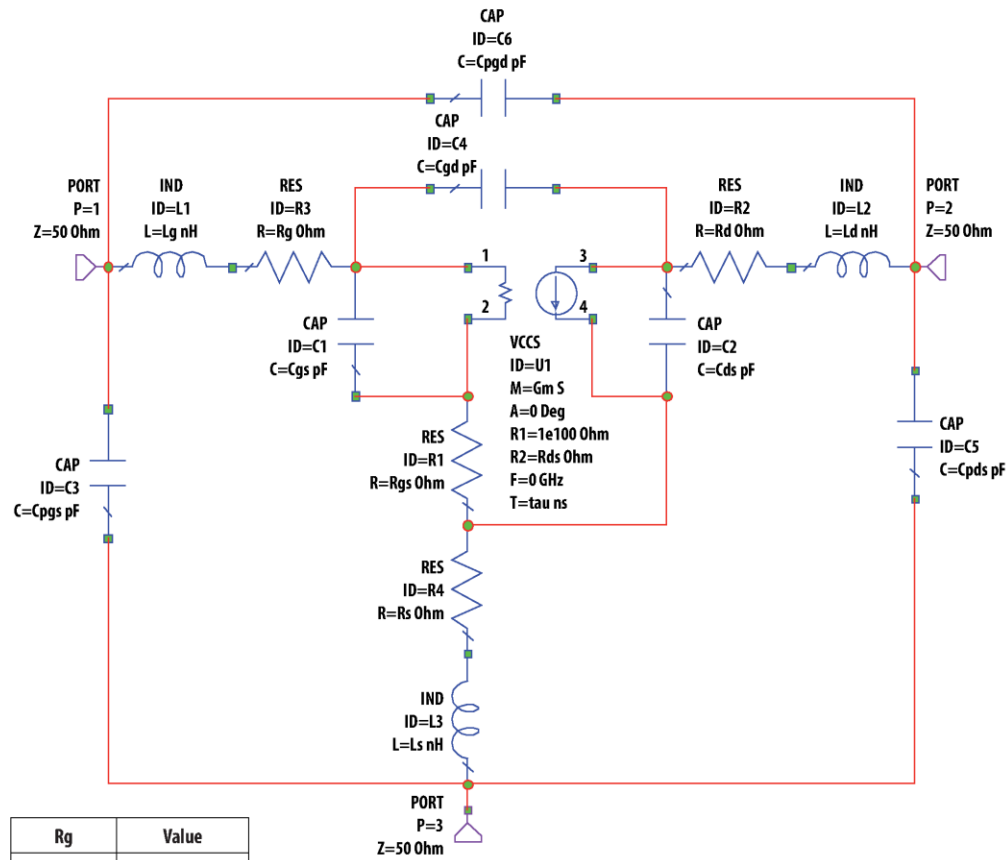
Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Vd (V)	3	Vd (V)	3	Vd (V)	3	Vd (V)	3
Id (mA)	5	Id (mA)	10	Id (mA)	15	Id (mA)	20
Gm	0.1112	Gm	0.193	Gm	0.258	Gm	0.3119
tau	0.00249	tau	0.0025	tau	0.00252	tau	0.002487
Cgs	0.6365	Cgs	0.8786	Cgs	1.08192	Cgs	1.26
Rgs	0.007447	Rgs	0.1353	Rgs	0.01	Rgs	0.0271
Cgd	0.06521	Cgd	0.0582	Cgd	0.053	Cgd	0.04772
Cds	0.1603	Cds	0.1595	Cds	0.1601	Cds	0.1595
Rds	438.90	Rds	260.60	Rds	209.10	Rds	172.90

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Vd (V)	4	Vd (V)	4	Vd (V)	4	Vd (V)	4
Id (mA)	5	Id (mA)	10	Id (mA)	15	Id (mA)	20
Gm	0.1088	Gm	0.1909	Gm	0.2509	Gm	0.3053
tau	0.00264	tau	0.002635	tau	0.002613	tau	0.00261
Cgs	0.6765	Cgs	0.9774	Cgs	1.203	Cgs	1.412
Rgs	0.00818	Rgs	0.1478	Rgs	0.01263	Rgs	0.02727
Cgd	0.05762	Cgd	0.05065	Cgd	0.04603	Cgd	0.04153
Cds	0.1565	Cds	0.1573	Cds	0.1574	Cds	0.1579
Rds	564.30	Rds	312.10	Rds	242.20	Rds	200.30

S Parameter Measurements

The S-parameters are measured on a .016 inch thick RO4003 printed circuit test board, using G-S-G (ground signal ground) probes. Coplanar waveguide is used to provide a smooth transition from the probes to the device under test. The presence of the ground plane on top of the test board results in excellent grounding at the device under test. A combination of SOLT (Short - Open - Load - Thru) and TRL (Thru - Reflect - Line) calibration techniques are used to correct for the effects of the test board, resulting in accurate device S-parameters. The reference plane for the S Parameters is at the edge of the package.

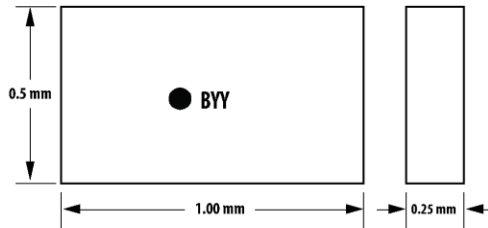
VMMK-1218 ADS Model



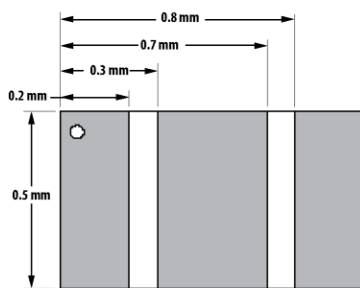
Rg	Value
Rg	4.729
Rd	1.29495
RsG	2.283
C pgs	0.0475
C pds	0.0318
C pgd	0.00417
Ls	0.000559
Lg	0.32446
Ld	0.2602

Outline Drawing

Top and Side View



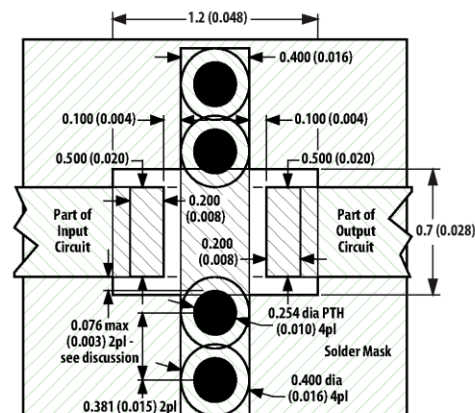
Bottom View



Notes:

- indicates pin 1
- Dimensions are in millimeters
- Pad Material is minimum 5.0 um thick Au

Suggested PCB Material and Land Pattern



Notes:

- 0.010" Rogers RO4350

Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

Manual Assembly for Prototypes

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers or from topside if using a vacuum collet.
- Recommended attachment is solder paste. Please see Figure 8 for recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
- Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. Excessive solder will degrade RF performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 to 40 sec. Verify that the profile will not expose device beyond these limits.
- Clean off flux per vendor's recommendations.
- Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

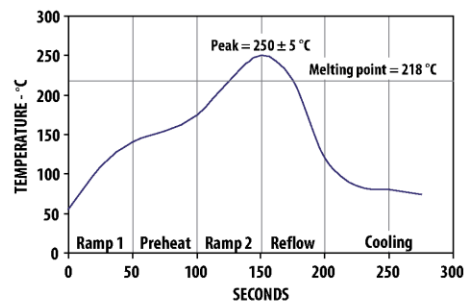
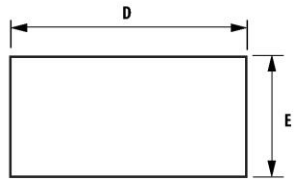


Figure 15. Suggested Lead-Free Reflow Profile for SnAgCu Solder Paste

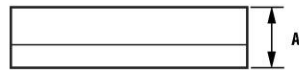
Part Number Ordering Information

Part Number	No. of Devices	Container
VMMK-1218-BLKG	100	antistatic bag
VMMK-1218-TR1G	5000	7" Reel

Package Dimension Outline

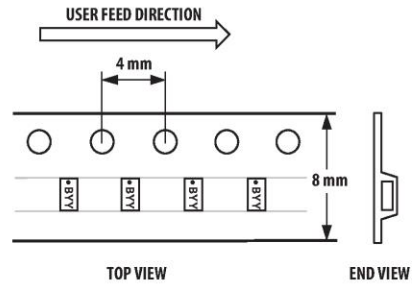
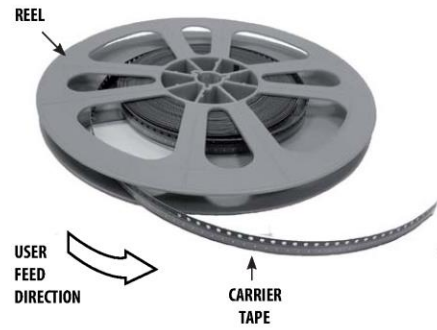


Symbol	Min (mm)	Max (mm)
D	1.004	1.085
E	0.500	0.585
A	0.225	0.275

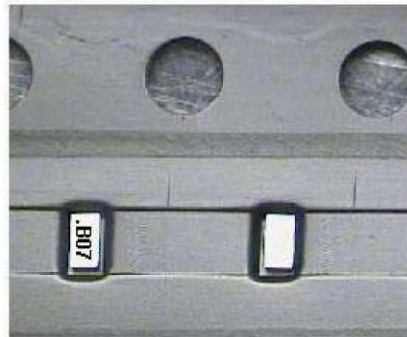


Notes:
All dimensions are in mm

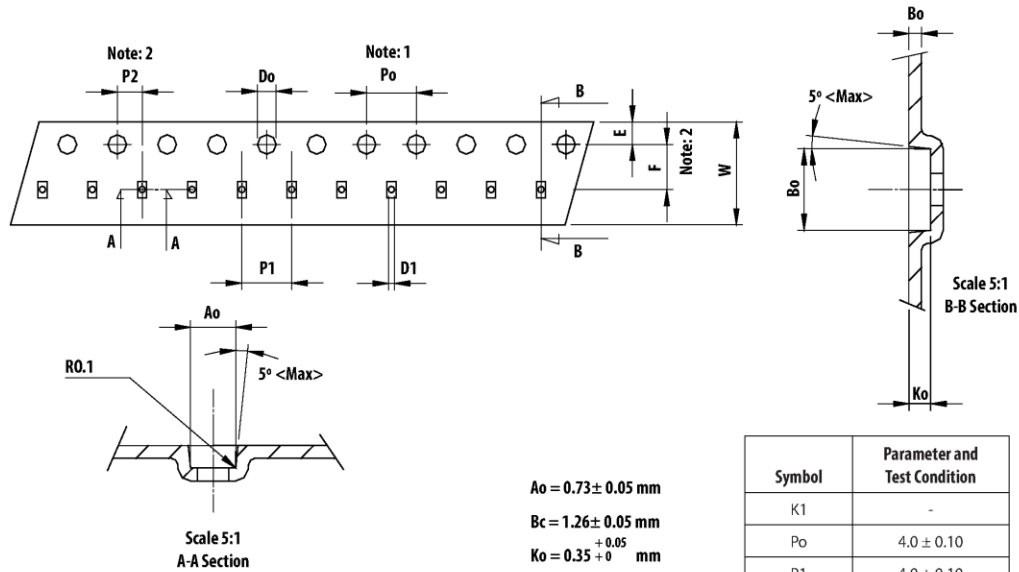
Device Orientation



Notes:
"B" = Device Code
"YY" = Month Code



Tape Dimensions



Notes:

- 10 sprocket hole pitch cumulative tolerance is ±0.1 mm
- Pocket position relative to sprocket hole measured as true position of pocket not pocket hole
- Ao & Bo measured on a plane 0.3mm above the bottom of the pocket to top surface of the carrier
- Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
- Carrier camber shall be not than 1mm per 100mm through a length of 250mm

Unit: mm

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AV02-1081EN - February 2, 2012

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