An Analytical Model of Drain Induced Barrier Lowering Effect for Gallium Arsenide (GaAs) MESFET's

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ABSTRACT

An Analytical Model of Drain Induced Barrier Lowering Effect for Gallium Arsenide (GaAs) MESFET's

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Master of Science in Electrical Engineering

The phenomena of DIBL (Drain Induced Barrier Lowering) effect on the short channel Gallium Arsenide (GaAs) MESFET's has been developed based on one dimensional Poisson’s equation. An analytical model for the exact threshold voltage shift effect on the non-linear short channel Gallium Arsenide (GaAs) MESFET is showcased. An effect of short channel device to the threshold voltage, drain-source applied voltage $V_{DS}$, ratio of Channel length and the channel depth (L/a), and Channel doping carrier Concentration $N_D$ has been incorporated in the present model. The model shows that threshold voltage and channel doping concentration $N_D$ are key parameters and justify a fair basis to the short channel apparatus and circuit design.
CHAPTER 1

1.1 INTRODUCTION:

GaAs “Metal Semiconductor Field Effect Transistors” MESFETs will be mostly used for digital and the applications because for their high frequency characteristics [1-3]. Properties of Gallium Arsenide based nonlinear circuits requires the utilization of an exact MESFET model if the expected as well as attained circuit properties are nearly related. For understanding the physical mechanism and operations of shot channel a general DC model is required. The model which we choose should predict all the characteristics of the device regardless of size or the characterization of all variables which can be change during fabrication. Apart from that, the practical results must match the theoretical calculations with much more accurateness.

“A much selection of nonlinear devices which we use to calculate the GaAs MESFET DC characteristics satisfy the required standards [4]. There are mainly four used models in designing of circuits, those are the (i) the Curtice model, (ii) the Statz model [5], (iii) the Kacprzak–Materka model [6], and (iv) the Rodriguez model for the simulation of large signal GaAs FET devices [7] and a comparison of these models is given in Rodriguez et al model” [8].

In order to develop or design a high-yield or low-cost microwave circuits, sufficient models of all components are needed. The first model of nonlinear GaAs MESFET’s was proposed by Curt-ice. The relations between capacitance to voltage were to be a first degree of approximation, these are assumed to be independent from current–voltage relation, and were explained and calculated form the simple diffusion capacitance. Later, Statz proposed predictions which are the modified equations which resulted in more accuracy for measured S- parameters, which are valid all areas of MESFET operation. The charges at device terminals are also concerned by these equations. Presently, lot of work is still going on in the area of nonlinear capacitance MESFET modeling. Designing accurate device simulations not only requires perfect device models, but also we need to extract all the parameters accurately.
In recent years, the device surface in the environment of the gate has been indirectly addressed in the advent of the low-temperature gown passive and gate-overlapping technology using GaAs MESFET. Devices which are utilized in this technology demonstrated in the dramatic improvement in the breakdown voltage of gate-drain, which in turn dramatically enhanced the output power of the devices [9].

“In recent years, the GaAs MESFET has increasingly been adopted in large-signal microwave applications such as power amplifiers and oscillators. As is well known, an essential prerequisite for computer-aided design software to obtain a reliable design depends critically on an accurate large signal model for GaAs MESFET, especially its nonlinear behavior. Therefore, much work has been undertaken and varieties of analytical models have been developed to describe the operation characteristics of a GaAs MESFET. Among the field-effect transistor nonlinear characteristics, the most important ones are the drain–source performance and the nonlinear gate charge with respect to drain–source and gate–source voltages. It is worth noting that the accuracy of the charge model affects the simulation results for frequency-dependent characteristics such as S-parameters, as well as nonlinear properties including distortion, harmonic analysis, and third-order inter modulation product, and adjacent channel power ratio”. “Therefore, there is a need for an accurate GaAs MESFET charge model for the design of microwave nonlinear circuits, especially applicable to power amplifiers” [10].

The main damaging effects of performance properties in GaAs MESFET devices have been determined on the surface of the device. Different speculative studies from past years it leads to the conclusion, that surface played a key role in the device characterization mainly, the break-down voltage and inconstancy in current voltage graphs and surface related parameters those have direct affect on the performance of a device power.

“Gallium arsenide devices have been widely used since the late 1960s for microwave applications, and they are still dominating this field. The use of GaAs for digital circuit applications began in the early 1970s, and it has developed over the years
into a well-established LSI technology, with an increasing number of VLSI applications in recent years. Two examples of digital circuit are the GaAs supercomputer CRAY-3 under development at Cray Research”[11]. Manufacturers nowadays using plug-in compatible GaAs devices instead of present, silicon based computer architecture and those are also replacing ICs (Integrated Circuits) like disc controllers and cache memories which increases device performance.

GaAs technology is trice more expansive than Silicon technology, depending on process complexity in to consideration, but its usage is tested in field of applications that require low power consumption and very high speed. From the increasing volume of portable electronic equipment, from phones to computers, the GaAs logic families are becoming attractive for system designers because their low power dissipation property.

The accurate models of the device with active and passive circuit elements are required for the design of the high speed gallium arsenide digital integrated circuits. Along with the use gallium arsenide integrated circuits the modeling had increased considerably, but the models using gallium arsenide still have a long difference to cover to reach the accuracy of the existing silicon MOSFET models. The lack of inadequate and non-proprietary model used for simulation of the circuit is restricting the use of gallium arsenide technology.

Recently however, “a large number of GaAs MESFET models have been proposed and some have been implemented in SPICE with far better results than the old, inadequate models. As the model complexity increases, however, it gets more difficult to extract the model parameters from measurement data, and it becomes necessary to resort to nonlinear optimization techniques. A lot of work has been undertaken and varieties of analytical models have been developed to describe the operation characteristics of a GaAs MESFET. Among the field-effect transistor FET’s nonlinear characteristics, the most important ones are the drain–source performance and the nonlinear gate charge with respect to drain–source and gate–source voltages. It is worth noting that the accuracy of the charge model affects the simulation results for frequency-dependent characteristics
such as -parameters, as well as nonlinear properties including distortion, harmonic
analysis, and third-order inter modulation product, and adjacent channel power ratio”
[12].

There are many ways in modeling MESFET gate charge capacitances are
explained in (i) Physical model [13-15], (ii) Table-based model [16 and 17], and (iii)
Empirical model. “Among these three, the empirical model is the most commonly used
approach in GaAs MESFET nonlinear modeling, which uses analytical functions to
describe bias dependence of the capacitances. The existing empirical MESFET charge
models can be classified into two groups. In the first group, analytical equations are
found to fit and separately while the terminal charge conservation is not considered.
These models may be difficult to implement in circuit simulators whose capacitance is
always the derivative of an internal state variable. In addition, the simulation may have
convergence problems as charge conservation is not maintained. In the second group,
analytical equations are proposed for terminal charge, and the capacitor values are
derived from the partial derivatives of charge with respect to the appropriate voltages.
These models are capable of accurately describing capacitance performance in some
device operation regions. However, normally the inaccuracy is still most significant in the
linear region, saturation knee region, and sub threshold region” [18].

1.2 Non Linear Microwave Circuits Utilizing GaAs MESFET:

In the simulation of nonlinear microwave circuits which uses “GaAs MESFET
devices shows that the simulation accuracy of the circuit from an ac point of view should
be quite sensitive to the accuracy by which the gate-drain and gate-source capacitances of
the device are modeled as the voltage function has been discussed with emphasis on the
Statz approach. From this point of view it restricts the bias area from which the accuracy
of these models remains high from the microwave point of view”[19].

“The MESFET is a three terminal device just like any other transistor as shown in
figure 1. The terminals are named as source, gate and drain. Charge carriers flow from
the source to the drain via a channel. The channel is defined by doping the epitaxial layer grown on semiconductor and offers good conduction. The flow of charge carriers in the channel is controlled by a Schottky barrier gate. The main advantages of a MESFET compared to its counter parts are high electron velocity inside the channel; smaller transit time leading to faster response and fabrication of active layer on semi-insulating GaAs substrates to decrease the parasitic capacitances”[19].

![Figure 1 Schematic cross-section diagram of the GaAs MESFET.](image)

A number of different GaAs FET models exist, and each of them can be classified among several different categories. When models are classified according to how they are derived, they can be grouped into physically based model, empirical model and experimental model. The models can be grouped into small-signal model, large signal model, when the FET models are classified according to the type of performance predicted by researchers, [20].

The high performance analog circuit and digital circuits with recent technologies as GaAs E/D and D MESFET technology is designed. These are most important to get such reliable simulation result of the circuit. Today, the device models and the 5 input parameters which had been used for these models do not meet those necessities rottenly. Most of the presently used circuit simulation of GaAs MESFET is more or less nonmaterial curve fitting models, which make task more complicated in getting the simulation results from the measurement data.

The empirical model can be easily implemented into circuit simulators. Thus, they are most widely used by circuit designers and in device libraries. Both small-signal and
large-signal models are important for nonlinear MESFET modeling. As mentioned earlier, power amplifiers are the main applications of GaAs MESFETs. MESFET devices exhibit nonlinear behavior in power amplifiers. Thus, accurate large signal MESFET models are particularly critical for the performance prediction of nonlinear microwave circuits. Although much work has been done in large signal modeling of GaAs MESFET, accurate linear and nonlinear models are still in great demand [21].

1.3 Characteristics Of GaAs MESFET:

Figure 2 to figure 5 show all “the simulated and the observed I–V characteristics of four different GaAs MESFETs. The proposed model is compared to Ahmed et al. model. The proposed model shows excellent accuracy when compared to Ahmed et al. model for all devices and for almost all bias voltages. The main deficiency of Ahmed et al. model is that the effects of gate bias, $V_{GS}$, on output conductance, $g_d$, in the saturation region of operation of the devices have been ignored. For sub-micron MESFETs, the transconductance $g_d$ depends not only on $V_{DS}$ but also on $V_{GS}$ for small-signal devices and also for the simulation algorithm” [22].

The calculated and the experimental GaAs MESFETs I–V characteristics for the parameters of $I_{ds}=192$ mA, $V_{t+\Delta V_{t}}=-2.0$ V where $\Delta V_{t}$ is geometrical increase in the threshold voltage, the simulated model with values $\alpha=1.7008$, $\gamma=-0.0666$ and $\lambda=0.0797$ and proposed values are $\alpha=1.7869$, $\gamma=-0.1776$ and $\lambda=0.0826$.

where

- $\alpha$: Voltage where the drain current characteristics saturates
- $\gamma$: Electric threshold voltage change and
- $\lambda$: Empirical constant related to the output conductance of the device are shown in figure 2.
Figure 2 GaAs MESFETs I–V characteristics for values $\alpha=1.7008$, $\gamma=-0.0666$ and $\lambda=0.0797$ [22]

The calculated and the experimental GaAs MESFETs I–V characteristics for the parameters of $I_{dss}=350$ mA, $V_t+\Delta V=-2.8$ V, the simulated model with values $\alpha=1.2877$, $\gamma=-0.3581$ and $\lambda=0.0211$ and proposed values are $\alpha=1.2144$, $\gamma=-0.1258$ and $\lambda=0.0122$ are shown in figure 3.

Figure 3 GaAs MESFETs I–V characteristics for values $\alpha=1.2877$, $\gamma=-0.3581$ and $\lambda=0.0211$. [22]

The calculated and the experimental GaAs MESFETs I–V characteristics for the parameters of $I_{dss}=192$ mA, $V_t+\Delta V=-2.0$ V, the simulated model with values $\alpha=1.7504$, $\gamma=-0.0618$ and $\lambda=0.0771$ and proposed values are $\alpha=1.8278$, $\gamma=-0.1635$ and $\lambda=0.0803$ are shown in figure 4.
Figure 4 GaAs MESFETs I–V characteristics for values
\( \alpha=1.7504, \gamma=-0.0618 \) and \( \lambda=0.0771 \). [22]

The calculated and the experimental GaAs MESFETs I–V characteristics for the parameters of \( I_{dss}=220 \) mA, \( V_t+\Delta V_t=-2.25 \) V, the simulated model with values \( \alpha=1.4007, \gamma=-0.2362 \) and \( \lambda=0.1110 \) and proposed values are \( \alpha=1.4077, \gamma=-0.1533 \) and \( \lambda=0.1078 \) are shown in figure 5.

Figure 5 GaAs MESFETs I–V characteristics for values
\( \alpha=1.4007, \gamma=-0.2362 \) and \( \lambda=0.1110 \). [22]
2.0 Nature and Properties of Gallium Arsenide material:

Gallium arsenide (GaAs) is a material with the gallium and arsenic elements. It is Zinc blende cubic crystals at a melting-point of 1238 °C, density: 5.3176 g/cm³. It is insoluble in water but slightly soluble compound at pH 7 in 0.1 M phosphate buffer. Gallium arsenide decomposes with evolution of arsenic vapor at temperatures higher than 480 °C and produce arsine gas when reacting with strong acid reducing agents to [23]. “GaAs is a III–V compound semiconductor composed of the element gallium (Ga) from column III and the element arsenic (As) from column V of the periodic table of the Elements. GaAs was first created by Goldschmidt and reported in 1929, but the first reported electronic properties of III–V compounds as semiconductors did not appear until 1952” [24]. The crystal of GaAs is made of 2 sub lattices, with each of face centered cubic (FCC) and offset with respect to each other by half the diagonal of the FCC cube. This type of crystal formation is called as zinc or cubic blended. The below figure 6 shows a unit cube of the GaAs and the general properties and material characteristics are listed in the below table.

Figure 6 Gallium Arsenide Crystal Lattice
Table 1 Properties of GaAs at Room Temperature.

<table>
<thead>
<tr>
<th>Property</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crystal Structure</td>
<td>Zinc Blende</td>
</tr>
<tr>
<td>Lattice Constant</td>
<td>5.65 Å</td>
</tr>
<tr>
<td>Density</td>
<td>5.32 g/cm³</td>
</tr>
<tr>
<td>Atomic Density</td>
<td>$4.5 \times 10^{22}$ atoms/cm³</td>
</tr>
<tr>
<td>Molecular Weight</td>
<td>144.64</td>
</tr>
<tr>
<td>Bulk Modulus</td>
<td>$7.55 \times 10^{11}$ dyn/cm²</td>
</tr>
<tr>
<td>Shear Modulus</td>
<td>$3.26 \times 10^{11}$ dyn/cm²</td>
</tr>
<tr>
<td>Coefficient of Thermal Expansion</td>
<td>$5.8 \times 10^{-6}$ K⁻¹</td>
</tr>
<tr>
<td>Specific Heat</td>
<td>0.327 J/g-K</td>
</tr>
<tr>
<td>Lattice thermal Conductivity</td>
<td>0.55 W/cm²°C</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>12.85</td>
</tr>
<tr>
<td>Band Gap</td>
<td>1.42 eV</td>
</tr>
<tr>
<td>Threshold Field</td>
<td>3.3 kV/cm</td>
</tr>
<tr>
<td>Peak Drift Velocity</td>
<td>$2.1 \times 10^7$ cm/s</td>
</tr>
<tr>
<td>Electron Mobility (undoped)</td>
<td>8500 cm²/V-s</td>
</tr>
<tr>
<td>Hole Mobility (undoped)</td>
<td>400 cm²/V-s</td>
</tr>
<tr>
<td>Melting Point</td>
<td>1238 °C</td>
</tr>
</tbody>
</table>
2.1 Structural Properties of GaAs:

“One of the important characteristics that are attributed to GaAs is its superior electron mobility brought about as the result of its energy band structure as shown in the figure 7 below. Gallium Arsenide (GaAs) is a direct gap material with a maximum valence band and a minimum conduction band and is supposed to coincide in k-space at the Brillion zone centers. In the graph shown below, we can see that the some valleys in the band structure are narrow and some are sharply curved. These curves and narrow differ corresponding to the electrons with low effective mass state, while valleys that are wide with gentle curvature are characterized by larger effective masses. The curvature of the energy versus electron momentum profile clearly shows the effective mass of electrons travelling through the crystal. The minimum point of gallium arsenide’s conduction band is near the zero point of crystal-lattice momentum, as opposed to silicon, where conduction band minimum occurs at high momentum. Now, mobility, \( \mu \), depends upon Concentration of impurity N, Temperature T, and is also inversely related to the electron effective mass, \( m^* \)” [25].

---

**Figure 7 Energy band diagrams of gallium Arsenide and Silicon. [25]**

“GaAs is a direct band gap semiconductor, which means that the maximum of the valance band is directly below or under the minimum of the conduction band. Transitions
between the conduction band and the valance band require only a change in energy, but no change in the momentum, until indirect band-gap semiconductors for example silicon (Si). These are the property which makes GaAs a very important material for the designing and manufacturing the semiconductor lasers and the light emitting diodes, because the photons is emitted when an electron changes its energy state from the conduction band to the valance band. Instead, “an incident photon can excite an electron from the valence band to the conduction band, allowing GaAs to be used in photo detectors” [26].

2.2 Mobility and Drift Velocity of GaAs, Si and GaN:

GaAs has many advantages than silicon in the field of microwave. Mainly, saturated drift velocity, higher mobility and the capability of producing devices on the semi-insulating substrate. In the semiconductor during the time of collisions with other carrier and the lattice of the semiconductor, the carrier will attain a velocity which will be the function of electric field strength. When an electron is subjected to an electric field, it will experience a force which can be written as ‘\( F = -qE \)’ and electron will be enhanced along the field. The velocity with which the carrier is enhanced is defined as the drift velocity (\( v \)). The variations for different semiconductors are shown in figure 8.

![Figure 8 Drift velocity of electrons in Si, GaAs, SiC and GaN](image)

From the point of the conservation of momentum, it is shown that the drift velocity (\( v \)) will be proportional to the applied electric field

\[
V = -(q\tau)E/m^* 
\]  

(1)
The electron mobility (m) is also known as the proportionality factor which depends on the electron effective mass (m*) and the mean free time between collisions (tc). The electron mobility is measured in the units of cm²/V-s.

“Mobility is an important parameter for carrier transport because it describes how strongly the motion of an electron is influenced by an applied electric field. From the equation above, it is evident that mobility is related directly to the mean free time between collisions, which in turn is determined primarily by lattice scattering and impurity scattering. The lattice scattering increases with temperature and becomes dominant at high temperatures and lattice scattering is a result of thermal vibrations of the lattice. Therefore, the mobility decreases with increasing temperature. The impurity scattering, which is a result of the movement of a carrier past an ionized dopant impurity, becomes less significant at higher temperatures” [27].

“Although the peak mobility of GaAs in the linear region can be as much as six times greater than that of silicon (Si) at typical field strengths, the advantage of GaAs may be only as much as a factor of two” [28]. This shows the point that GaAs devices are much better to work at better frequencies than Silicon. The growth in the speed of operation mainly depends on the aspects such as the electric field regime and the circuit capacitance in which the devices are operated.

2.3 Fabrication Overview and Process Design:

The overall step-by-step MESFET fabrication processes are described here by referring each step to a particular Standard Operating Procedure (SOP) number. The fabrication process starts by inspection and cleaning of the wafer following specific procedures and ends at contact metallization and finally packaging, but only up to metallization processes are presented here. A number of theoretical calculations are also provided here to predict the device characteristics and the important parameters. The calculations of implant profile, sheet resistance, gate built-in potential, Pinchoff and Threshold voltage are done using the process parameters used in the laboratory. Finally, comparisons of the theoretical calculations with the simulation results are provided.
2.4 GaAs MESFET Fabrication Process:

The overall MESFET fabrication processes are described below in a numbered fashion below. This schedule describes a four mask, double implant process in formation of GaAs MESFETs with implanted channels. The four mask levels are:

1. Channel implant
2. Source/drain implant
3. Ohmic contact formation
4. Schottky gate formation

The masks are all light field and positive resist is used throughout the process. The basic fabrication process for constructing GaAs MESFETs uses a simple four mask, double ion implantation process as shown in Figure 9.
This process begins with the preparation of the GaAs wafer which is usually selected to have a (100) surface, zero intentional doping and a very high resistivity (> 108 ohm-cm) making it semi-insulating. This type of substrate is used to reduce parasitic capacitances and for device isolation. To prepare the substrate, the GaAs wafer is slightly etched to remove about 100 nm to remove surface oxide, contamination and damage from packaging and handling. A silicon nitride insulating layer is then deposited by reactive sputtering to a thickness of 100 nm. This capping layer protects the GaAs surface during the entire processing operation and helps to prevent loss of As from the surface by decomposition of the GaAs during high temperature processing.

The first masking step (mask #1) in the fabrication is the formation of the channel regions between the drain and source regions using a silicon ion implantation process. Since the GaAs substrate is semi-insulating, implantation of silicon ions is used to form a lightly doped but conducting, n-type region. The energy and dose for the silicon implantation is determined from the pinch-off voltage required for the MESFET. Positive resist is used to define the channel location (area of the wafer surface to be implanted) and implantation is done through the silicon nitride cap layer. After implantation, the silicon nitride is slightly etched (about 30 nm deep) in order to mark the wafer surface before the resist is removed for subsequent alignment of masks for the drain and source and gate regions. The resist is then stripped off the wafer leaving the nitride intact.
Formation of the drain and source regions for the MESFET is done in the next masking step (mask #2) in a similar fashion. Positive resist is again used to define the area of implant and implantation is done through openings in the resist and through the silicon nitride cap layer. The energy and dose for the silicon implantation is now determined by the need for low resistance, ohmic source/drain regions contacting the ends of the channel. Higher doping levels are required (> 1018 /cm3) to provide low resistance contacts and to form low resistance, ohmic metal-semiconductor contacts for contacting metal to the MESFET's source and drain regions. The resist is then removed (stripped) after the implant.

Since implantation produces severe damage to the semiconductor lattice, a thermal annealing step is needed after the implant to repair the damage and to activate the implanted species. After removal of the resist from the source/drain implant, the wafer is rapid thermally annealed at an elevated temperature for a brief period (seconds). The silicon nitride cap on the wafer during this process helps to control the decomposition of the GaAs surface which can occur by the preferential loss of As. This completes the formation of the active regions in the device.

Next, to make electrical contacts to the device's source and drain regions, resist is applied and patterned (mask # 3) and openings in the silicon nitride are etched down to the semiconductor surface over the source and drain regions. After patterning, the resist is treated in chlorobenzene to swell its top surface and produce an overhanging ledge at the top of the resist in the windows. The underlying silicon nitride is etched away in the windows to expose the underlying GaAs surface. The contact metal Au/Ge/Ni is then deposited, patterned and the excess metal removed (lifted off) by dissolving the resist in a solvent. This same lithography process and liftoff technique is also used to pattern the aluminum Schottky metal (mask #4) to form the gate electrode for the MESFET.

The MESFET's fabrication is now complete and the device is ready for testing and electrical characterization. The fabrication process outlined above is a basic one with a minimum of mask levels and processing. More sophisticated fabrication processes may
contain more mask levels, for example to define a second layer of metal for interconnection of devices. Over the course of this quarter, we will proceed systematically through this fabrication process by performing a set of process steps each week. The aim is to complete the device fabrication by the end of the eighth week so that the electrical characters of the devices and test structures can be done in the last two weeks.

2.4.1 Typical Example of GaAs MESFET Fabrication process:

"The bellow steps are the detailed process of GaAs MESFET fabrication.

1. Initially cleaning of wafer.
2. Deposition of silicon nitride cap by using reactive sputtering technique.
   a. cap thickness = 100 nm
3. By using positive resist we should pattern for channel implant.
   a. resist thickness = 1.6μm
4. Silicon ion-implantation for device channel regions.
   a. maximum ion energy = 180keV
   b. ion species = Si+ (singly ionized)
   c. dose = 5 x 1012 /cm2
5. Shallow etching of silicon nitride for alignment registration purposes
6. In buffered HF solution and plasma etching.
7. Resist stripping and ashing in oxygen plasma.
   a. Target resist thickness = 0.8μm
9. Silicon ion implantation of device source and drain regions.
   a. Maximum ion energy = 200keV
   b. Ion species = Si+ (singly ionized)
   c. Dose > 1 x 1013 /cm2
10. Resist stripping and ashing in oxygen plasma.
11. Annealing of ion implants using rapid thermal annealing (SOP # 203).
   a. Maximum temperature = 850 °C
b. Ambient = forming gas  
c. Time = 90 to 120 seconds

12. Resist patterning for ohmic contact formation.
   a. Target resist thickness = 0.8μm

13. Silicon nitride etching for ohmic contacts.

14. CF4 plasma etching to semiconductor surface.

15. Final wet etch cleaning of exposed GaAs surface in 50 %HCl.

16. Deposition of AuGe/Ni metal for ohmic contacts to source and drain using

17. E-beam evaporation and patterning by liftoff technique.

18. Ohmic contact alloying by rapid thermal heating.
   a. Maximum temperature = 475 – 500 °C
   b. Ambient = forming gas
   c. Time = 120 seconds

   a. Target resist thickness = 1.6μm

20. Silicon nitride etching for Schottky gate formation.

21. CF4 plasma etching to semiconductor surface.

22. Final wet etch cleaning of exposed GaAs surface in 50 %HCl.

23. Aluminum metal deposition for Schottky gate formation using e-beam evaporation and patterning by liftoff technique.” [28]

2.5 Ion Implantation:

Gallium arsenide (GaAs) MESFETs are mostly used in a variety of military applications as well as commercial applications such as in wireless communication. MESFET is the main component in MMIC (Monolithic Microwave Integrated Circuit) technology and most utilized component in power amplifiers and high-speed IC switches. The stable and highly reliable components are really critical to get success in both the fields.

We are presenting a study in the side-gating effects which can be witnessed on GaAs MESFET Monolithic Microwave Integrated Circuit. Side-gating (SG) or back-gating effect occurs sometimes in MESFET ICs fabrication in SI GaAs. When we apply
negative voltage to adjacent electrodes it exhibits itself a significant fall-down in drain current, or to the backside of the substrate. Such an effect will make an cross talk or undesired coupling between adjacent devices, this can limit scale of the integration for GaAs ICs. It is challenging for both amplifier and switch applications i.e. this is very important to research and know the origins of that effect.

The active regions of SAGFET were formed by ion implantation into the semi-insulating (SI) liquid-encapsulated Czochralski (LEC) GaAs wafer through a 400 A nitride cap. A buried P layer was generated using a blanket Be implant. The depletion-mode channel was created by a first blanket Si implant followed by a second selective Si implant. A Twin metallization was used to form the 0.5-pm Schottky gate contact. SiN/Si02 spacers were fabricated next to the gate, after which a self-aligned implant and anneal followed. Boron isolation was used to minimize the cross talk between adjacent FETs. A gold layer was added to the gate finger to reduce parasitic gate resistance. Finally, the device was passivated with a silicon nitride protection layer.

Devices examined at high speed SPDT switches uses, the ion-implanted SAG GaAs technologies. The Conventional REG MESFETs will have a very high breakdown voltage \( V \) and small gate leakage current \( I_1 \), due to the reduced field strength at the surface and below the REG. However, because of the uncertainty in recessed depth, the uniformity of breakdown voltage \( V \), and saturation current of drain-source \( I_g \) are very week. In effective to that, the SAG-FETs which are mainly used in digital and analog Integrated Circuits shows good control in current \( I \), and \( V_{bk} \) with low pinch-off voltage \( V_p \), and more drain source \( I_{ds} \). They are cheaper because they require very few steps of process.

Ion implantation has many advantages over diffusion:

1. Direct control of the dopant and width of dopant
2. Possibility for uniformity
3. Able to create abnormal shapes of the dopant (can use masks)
4. Room temperature operation
2.5.1 Implantation System:

The ion-implanter is a very high voltage particle accelerator which produces a very high-velocity ray which has impurity ions which will penetrate through the surface of semiconductor targeted wafer. The basic parts of the system are shown schematically in Figure 10. This system includes: 1. Ion source, 2. Mass spectrometer, 3. High voltage accelerator, 4. Scanning system, 5. Target chamber.

![Figure 10 Schematic of ion implanter](image)

2.5.2 Impurity diffusion for Ion Implantation:

Many semiconductors use a diffusion process to place impurities in the semiconductor but GaAs evaporates at the temperatures required for diffusion. To introduce the dopants a process called ion implantation is required. This shows many benefits compared to diffusion process for the addition of impurity atoms into semiconductor wafer and has became a workhorse technology in modern integrated-circuit fabrication. In this section, we first briefly introduce the implantation system and theories. Then source/drain and channel doping profiles are predicted by doing theoretical calculations and software simulation for the parameters that we use in the implantation. Based on the doping profile calculated, other MESFET parameters such as barrier height, built-in potential and sheet resistance are also calculated in the following sections.
When an ion enters into the surface of the wafer, it will collide with the atoms in the lattice and will collide with electrons present inside the crystal. Each electronic or nuclear collision will make electron in reducing the energy of the element until it will come to rest within the target finally. Collision within the crystal is known as statistical process, and the profiles of these inserted impurities can be expressed with GDF (Gaussian distribution function). The distribution is shown as below

\[ N(x) = N_p e^{-\frac{(x-R_p)^2}{2\Delta R_p^2}} \]  

(2)

where

- \( N_p \) = peak concentration
- \( R_p \) = projected range
- \( \Delta R_p \) =projected range straggle

\( R_p \) is known as the projected range which is equal to the average distance of an ion travel before it comes to rest. The \( N_p \) (peak concentration) which occurs at \( x = R_p \). Because of the statistical nature of the process, some ions will be “lucky” and will penetrate beyond the projected range \( R_p \), and some will be “unlucky” and will not make it as far as \( R_p \). The distribution characterizes the standard deviation \( \Delta R \), which is known as the straggle.

The total number of ion implantation per unit area is the implanted dose \( Q \), which can be calculated from the integration of impurity concentration under the curve, given by

\[ Q = \sqrt{2\pi} N_p \Delta R_p \]  

(3)

Implantation doses can range from \( 10^{10} \) /cm\(^2\) to \( 10^{18} \) /cm\(^2\), and the ion-implantation is mainly used to replace a step in a two-step diffusion process which is pre-deposition. Doses in the range of \( 10^{10} \) /cm\(^2\) to \( 10^{13} \) /cm\(^2\) are required for threshold adjustment in MOS technologies and are almost impossible to achieve using diffusion.
2.6 Crystal Defects

There is no perfect crystalline semiconductor material, and GaAs crystals, in spite of that the effort to control the growth of the crystal, which contain a many crystal defects, impurities and dislocations. The nature of this defect and the observed effect are explained by the method of their fusion into the material, the general growth conditions and defects can have both desirable and undesirable effect on the electronic properties of GaAs as shown in Figure 11.

![Figure 11 Crystal Defects in GaAs](image)

2.7 Point Defects

The point defects are the Confined defects in the atomic dimensions; these can takes place any perfect crystal lattice. The point defects can also have interstitials, vacancies-atoms, some misplaced-atoms, and these effects intentionally introduce dopant impurities, which are induced accidentally during the process of material growth. The study of these defects is very needed due to effect created by these defects shown on the all kind of properties i.e. electronic properties and it also effect the relation between the diffusion and type of defects in the materials with crystalline structure. There will be a deliberate change in the electrical characteristics of a semiconductor by the incision of
impurities inside the material in the process. However, the defects which are existing intrinsically also play an important role in the behavior of GaAs.

There are more intrinsic defects which can be observed in GaAs. “EL2, an important defect in GaAs, is present in material grown from an arsenic rich melt. This defect is donor-like in character and is located at the middle of the energy gap” [31]. The manner with which this material is grown determines the effect and concentration of defects. The defects which are intrinsically within GaAs include vacancies of gallium and arsenic, the overpressure of arsenic determines the concentration of effect during processing. These vacancy defects are observed to be neutralized [29], by the deep donor-like, and by deep acceptor-like [30]. These are very thermally established and can tolerate for processing temperatures till 900°C, and will perform as an electron trap. Main effects of these defects are the ability of converting the p-type GaAs materials into semiinsulating materials, and are thermally stable. We can clearly observe the point defect in the GaAs material in the figure 12 shown below.

![Figure 12 Point defects in GaAs](image)

Figure 12 Point defects in GaAs
2.8 Impurities in GaAs:

During processing of GaAs some chemical defects, due to doping impurities are introduced inadvertently or deliberately into crystalline materials as contamination. Generally, the substitution impurities will be in active electronically, else many other are naturally interstitial and are inactive electronically. Dopants will be classified as donors and acceptors. A donor is the atom with more electrons and it will be replaced in the crystal the donor which has more electrons can easily donate or removed by the conduction current. The acceptor is the one which has a vacancy to accept an electron which will capture and prevent an electron from being added to the conduction band.

Figure 13  The diagram of Energy band in GaAs material with impurities.

The energy band diagram in Figure 13 shows the addition of impurities in GaAs material. It is also showing the levels in conduction and valence band within 3kT of Shallow donor or acceptor, respectively. It requires very less energy for the transition of electron from the impurity energy level to the level with the nearest band edge, these are completely ionized at T=3K. The Fermi level will shift to the impurity levels from the center of band which reflects. The Fermi level will shift nearer to conduction band and will decrease with the increase of donor doping concentration according. We can also make similar description by using acceptor impurities. The deep impurities are the impurities which are at the center of the band gap. The performances of the devices are generally decreased by these deep impurities by decreasing the carrier lifetime.
“There are both deep and shallow impurities, are present in GaAs in the form of complexes with gallium or arsenic. One of the most common is silicon. This group IV element can be used to give either p-type GaAs by incorporating it at low temperatures, or n-type GaAs by processing it at high temperatures. Another group IV element, carbon, is also used extensively to provide p-type GaAs. Chromium (Cr) behaves as an acceptor, with an impurity level close to the center of the energy gap. This property makes it very useful for counter doping n-type GaAs to make it semi-insulating. Other elements such as copper, oxygen, selenium, and tin are also used as Schottky contact in GaAs processing to form the desired n- or p-like behavior” [32].

2.9 Static Domain Effect in GaAs devices:

When the Gunn domain is formed in a typical GaAs MESFET structure its position varies under the gate and the displacement is much more dependent on $V_{Gs}$ than on $V_{DS}$. The domain size $X_{dom}$ is more directly associated with $V_{DS}$ and depends only weakly on $V_{Gs}$. The domain height will be the function of $V_{Gs}$ and reaches maximum value of approximately one-third of the active layer thickness ‘a’[33] as shown in figure 14.

![FIGURE 14 “Physical Insight of GaAS MESFET with Domain effect”](image)
The location of $E_{\text{max}}$ is always near to the gate edge, on the drain side, it varies only slowly with $V_D$s and coincides with $x_c$ or $V_{G_S}$ approaching zero. Thus, the location of the field $E_{\text{out}}$, external to the domain proposed by Suhr and Eastman [34] to be exactly at the gate edge, may give an over-evaluation of this field up to two orders of magnitude because its maximum is just located at this position, as confirmed by the simulations shown here.
CHAPTER 3

Theory of MESFET

3.0 Physics of MESFET:

The Metal-Semiconductor-Field-Effect-Transistor (MESFET) comprises of a leading channel positioned between source and drain contact area are shown in the figure-15. Flowing of charge carriers from drain to source are regulated by a Schottky metal entryway. The channel control is acquired when fluctuating depletion layer width underneath the metal contact which tweaks thickness of the directing channel and in this manner the present.

![Fig 15 “MESFET Cross-sectional view”](image)

The important feature of the MESFET is its higher portability of the charge carriers in the channel and it is contrasted with the MOSFET. On account of the charge carriers are found in reversal layer of an MOSFET will have a wave equation which will amplify into the oxide, the versatility-moreover pointed to the surface portability-is less than a large part of the portability of mass material. As the depletion layer disconnects charge carriers from the surface, their portability will be near to that of mass material. Higher versatility advances to a higher current, the trans-conductance which transits frequency of apparatus.
The higher travel frequencies of MESFET make it especially of interest in microwave circuit. Whereas the important feature of the MESFET furnishes a predominant microwave speaker or circuit, the disadvantage by the diode turn-on is effortlessly accepted. Ordinarily depletion-mode apparatuses are utilized inasmuch as they furnish a more imposing current and more expansive transconductance and the circuits hold just a couple transistors, with the control of threshold is not a constraining element. The buried channel likewise yields a preferable uproar exhibition as trapping and discharge of transporters into and from surface states and defects is wiped out.

3.1 Basic Operation in GaAs MESFET:

The overall electrical characteristics of the GaAs MESFET are mainly determined by the electrical property of the semiconductor material and the nature of the physical contact to the material. Knowledge of the device physical structure and properties is helpful for both device modeling and circuit design. In the second part of this chapter, a brief description of MESFET operation is presented. It covers the basic construction of the device, the major operating regions, the small signal equivalent circuit, important nonlinear properties, and some second order effects [40].

A variety of models have been proposed for the GaAs MESFET. For small signal models, the difference of various models lies in the equivalent circuit topology selection and the way the equivalent circuit parameters are extracted. For nonlinear models, according to how these models are derived, they can be classified into physical model, empirical model, experimental model and the more recently developed black-box model, various MESFET models have been used by both device and circuit designers. Different applications and designs place different requirements on the model. Therefore, an understanding of the features of various modeling approaches is helpful for choosing the right model, and constructing new models for different application. The second part of
this chapter gives an overview of GaAs MESFET models, including the nonlinear and the small signal models [41].

3.1.1 GaAS Devices Description and Operation:

A GaAs MESFET cross-section view will be shown in Figure-16, which illustrates its basic structure. Three metal electrode contacts are shown to be formed onto a thin semiconductor active channel layer. Drain and source are ohmic contacts, while gate is a Schottky barrier. The gate metal forms a Schottky barrier diode, which gives a depletion region between the drain and source. The gate depletion region and a semi-insulating substrate form the boundary of the conducting channel. A potential applied at the drain causes electrons to move to the drain from the source. Any potential applied on the gate makes a change in shape of depletion region and a subsequent change in current flow.

![GaAs MESFET Cross-sectional view](image)

**Figure-16 “GaAs MESFET Cross-sectional view” [42]**

The most critical dimension is the “length” of the gate along the carrier path for microwave operations. The shorter the gate length, the higher becomes the signal frequency. If the FET is to handle a large amount of signal current, the gate width must be increased appropriately [42].

“The MESFET is a form of semiconductor technology which is very similar to a junction FET or JFET. As the name of the MESFET indicates, it has a metal contact directly onto the silicon, and this forms a Schottky barrier diode junction. The material
that is used in this form of semiconductor technology is GaAs (gallium arsenide). The substrate for the semiconductor device is semi-insulating for low parasitic capacitance, and then the active layer is deposited epitaxial. The resulting channel is typically less than 0.2\μm thick. The doping profile is normally non-uniform in a direction perpendicular to the gate. This makes for a device which has good linearity and low noise. Most devices are required for high speed operation, and therefore an n-channel is used because electrons have a much greater mobility than holes that would be present in a p-channel” [43].

The TPG (Titanium-Platinum-Gold) layered structure makes a gate contact from a wide variety of materials which includes Aluminum and Platinum itself and Tungsten. This will provide high barrier height due to this leakage current will be reduced. This is especially important for the devices which are operated in enhancement mode and which need a junction with forward bias.

“The gate length to depth ratio is an important as this determines a number of the performance parameters. Typically it is kept at around four as there is a trade-off between parasitic, speed, and short channel effects” [44]. The ion-implantation forms drain and source regions. The AuGe (Gold-Germanium alloy) is the normal forms drain contacts for GaAs MESFETs.

MESFETs has two main structures which are used regularly, as shown in Figure 17 and Figure 18

1. **Self-aligned source and drain**

   This type of arrangement decreases channel and gate contact will enclose the entire length. This could be finished on the grounds that the gate is formed initially, the gate contact must have the ability to withstand for high temperatures, this will result in the utilization of more materials being suitable. However in place that the tempering process needed after the arrangement of the drain and source regions by particle implantation,
2. Non-Self-Aligned drain and source

In this type of MESFETs, the gate are set on a segment of the channel. The gate contact doesn’t shields the holes in the length of the channel. This comes into picture due to drain and source contacts forms generally before the gate.

3.1.2 GaAs MESFET I-V Characteristics

The current voltage relationships of a MESFET are illustrated in Figure 19. The channel current is plotted as a function of applied drain-source potential for different gate-source voltage levels. Three regions of operation can be identified from the figure. They are the linear region, the saturation region and the breakdown region. In the linear region, current flow is approximately linear with drain voltage. As drain potential increases, the depletion region at the drain end of the gate becomes larger than at the
source end. Since the device is taking constant current through the channel region, the electrical field increases as the channel region narrows, and therefore a related increase in electron velocity occur [45].

“However, if the gate reverse bias is increased while the drain bias is held constant, the depletion region widens and the conductive channel becomes narrower, reducing the current. When \( V_{gs} = V_p \), the pinch-off voltage, the channel is fully depleted and the drain current is zero, regardless of the value of \( V_{ds} \). Thus, both \( V_{gs} \) and \( V_{ds} \) can be used to control the drain current. When the MESFET is operated under such bias voltages, where both \( V_{gs} \) and \( V_{ds} \) have a strong effect on the drain current, it is said to be in its linear or voltage controlled resistor region channel near the drain becomes narrower, the electrons must move faster.

Figure 19 I-V characteristics of MESFET

However, the electron velocity cannot, increase indefinitely; the average velocity of the electrons in GaAs cannot exceed a velocity called the saturated drift velocity, approximately 1.3x10^7 cm/s. If \( V_{ds} \) is increased beyond the value that causes velocity saturation (usually only a few tenths of a volt), the electron concentration rather than velocity must increase in order to maintain current continuity. Accordingly, a region of electron accumulation forms near the end of the gate. Conversely, the transit time of electrons is the time required to cross the channel and move at saturated velocity into the wide area between the gate and drain, an electron depletion region is formed” [46].
“The consumption district is decidedly charged due to the positive benefactor particles staying in the precious stone. As \( V_{ds} \) is expanded further, as indicated, logically a greater amount of the voltage expansion is dropped over this district to uphold the electrons to cross it and less is dropped over the unsaturated part of the channel. This district is called a dipole layer or charge area. In the long run, a focus is arrived at where further build in \( V_{ds} \) is dropped completely over the charge area and does not significantly expand the channel current. As of right now, the electrons move at soaked float velocity over a huge part of the channel length. The point when the MESFET is worked in this way, which is the typical mode of operation for minor indicate units, it is said to be in its immersed district” [47].

3.1.3 Transconductance and output resistance

The important characteristic which plays main role in analog applications is output conductance of the device. Output conductance will play an important role for getting maximum voltage gain achievable by the device and those are particularly necessary for defining properties of optimum output matching. Generally, for a device to have low value output conductance is desirable, or, equivalently, an extremely high output resistance. Figure 20 shows measured microwave output resistance for a MESFET device. As expected from Figure 10, the output resistance is low at low drain-source bias levels and increases dramatically as the device reaches saturation. This is true for all the curves except for a gate bias level of \(-1V\). At this bias level, the active channel is nearly pinched-off by the depletion region. Device dimensions and channel material properties both affect output resistance of the MESFET. As in the case of channel current, the magnitude of the device output conductance (the inverse of the resistance) is directly proportional to device gate width.
For device with equivalent gate widths, short gate lengths typically result in lower output resistances. The output resistance can also be reduced by increasing channel doping concentrations, $N_d$, or the device epi-thickness. The device trans conductance can be defined as the slope of the $I_{ds}-V_{gs}$ characteristics which held constant with the drain-source voltage.

In GaAs MESFET’s and JFET’s the Trans-conductance($g_m$) and its phase angle shows required low-frequency scattering. The trans-conductance which we measure at High frequencies is considerable lesser than what we measure at low frequencies. The transition frequency has a dip appearing around the phase angle. 10 Hz to few 10kHz is the typical range of transition frequencies. More than that, there is a strong influence on the trans-conductance due to the (i) Surface treatment,(ii) Gate voltage,(iii) Temperature, and (iv) Device structure. The low frequency dispersion of Trans-conductance ($g_m$) will have intense effect on the FET-based MMIC’s microwave behaviors [51]. To clarify and to regulator this effect required in achieving controllable and reliable device.

**3.1.4 Capacitance $C_{gs}$, $C_{gd}$ and $C_{ds}$**

The behavior of depletion region beneath the gate of a MESFET is determined by the bias applied to the device terminals. The variation of the space charge region is caused by both gate-to-source potential and gate-to-drain potential. Gate charge $Q_g$ is considered to be the space charge beneath the gate that varies with gate bias and drain bias. The plot for the gate to drain capacitance and gate source capacitance with regards
to the drain to source voltages is shown in figure 21 and figure 22 [50].

The $C_{gs}$ (gate-source capacitance) is the derived from the space charge with regards to the $V_{gs}$ (gate-source bias), when $V_{gd}$ (gate-drain voltage) is constant:

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}}$$  \hspace{1cm} (1)

Figure-21 Plot of Drain- Source Voltage and Gate-Source Capacitance

The $C_{gd}$ (gate-drain capacitance) is smaller than $C_{gs}$ (gate to source) under normal bias conditions. However, it is critical in perfect S-parameter prediction. The $C_{ds}$ (drain-source capacitance) in the equivalent circuit is introduced to model

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}}$$  \hspace{1cm} (2)
3.2 Device Models of GaAs:

In a typical application, models are used to predict or estimate performance information that is not available or easily obtainable by direct measurement. Small signal, large-signal and noise models are utilized to obtain information about device characteristics. Small-signal models can offer the designer the ability to predict performance of devices with gate width dimensions that have been scaled from previously measured devices. Another use of these models is to interpolate or extrapolate measured data to frequencies not covered by measurements. Noise models are used to predict the noise figure for arbitrary circuit topologies, which incorporate a particular device, or to predict the ultimate noise performance of a device [51].

A large-signal model provides a means of obtaining performance information concerning nonlinear operation of a device or device-circuit combination. Models are classified according to how they are derived. Empirical models are derived from describing observed characteristics with arbitrary functions. Physically based models are derived from the physical principles that apply to the device structure. And many models have aspects of both empirical and physical derivations. Physically based models are useful to circuit and device designers who have some control over the fabrication process because they allow simultaneous optimization of both the devices and the circuits in which they are to be used.

Additionally, a physical model is useful for predicting the effects of process variations on the electrical behavior of a device. If the statistical distribution of the process parameters is known, yield predictions can also be obtained. Using such an approach, performance prediction information may be obtained purely from physical data describing the device (i.e., device geometry and semiconductor material properties). No electrical characterization of individual devices is required. But purely physical models are not as perfect as needed for the most circuit design applications. To perform design analysis we require assumptions and approximations. Even the most sophisticated multidimensional numerical device simulation techniques make simplifying assumptions
that can severely limit their accuracy. For example, surface state effects, traps, non-homogeneous interfaces, etc., are typically neglected in these analyses. Yet these phenomena have major effect on microwave performance of modern devices.

A second problem with physically based models is that information concerning the physical design of the device can often be difficult or impossible to obtain-especially for the circuit designer utilizing purchased devices. This problem may be solved by extracting the physical parameter values from measured data in the same way that empirical parameter values are determined. In contrast, empirical models are capable of prediction accuracies that approach measurement capability [52].

The primary difficulty with this approach is that large amounts of monotonous characteristics of data are often required to obtain such accuracy. In addition, minor changes in the device geometry or material require the performance of complete characterizations. Such models are also of questionable value when performing design centering or yield analyses because the empirical parameter distributions do not vary independently. Because physical models are typically less accurate than their empirical counterparts, one attractive implementation is to use an empirical model to simulate nominal device performance and then use the physically based model to predict the deviations about this nominal behavior resulting from process parameter variations. In this chapter, we will give some details of several models. The section is divided into two sections according to the type of performance predictions for which the models are used in large signal model and small signal model [53].

3.2.1 The small-signal Model:

MESFET model is very necessary for microwave active circuit design. This model provides a dynamic link between calculated 24S-parameters and the process of electrical properties in device. Each of the elements in the equivalent circuit as shown in Figure 23 provides a tolerate element approximately some aspects of the device physics. A properly chosen topology, in addition to being physically meaningful, provides an
excellent match to measured S-parameters over a very wide frequency range. When element values are properly extracted, the model is usable above the measurement frequency range, providing the possibility of extrapolating device performance to frequencies beyond some equipment’s measurement capabilities. In addition, with the given gate width one can scale the equivalent circuit element, thereby enabling the designer which predicts S-parameters for different sized devices from a given foundry. The ability to includes device gate width scaling as part of circuit design process is important in MMIC design applications [54].

![Small signal model equivalent circuits](image)

Figure 23 Small signal model equivalent circuits

3.2.2 Large Signal Model:

Several researchers had advanced the empirical model that describes the operational characters of the GaAs MESFET. From these models are analytical and all are skilled of describing the properties of large-signal microwave MESFETs with some success. The MESFET models discussed in this section are available in many of the popular large-signal circuits. For any given device and application, the optimal choice of all these models depend on different considerations which includes availability of the model, computational efficiency, and prediction [55].
Large signal models are required for circuit simulation that is involved in predicting either large signal or nonlinear performance. As in Figure 24 a typical model of equivalent circuits for the MESFET large-signal models is shown. The equivalent circuits are divided into the intrinsic and the extrinsic parasitic elements. The extrinsic elements will have Parasitic capacitance associated with the gate of a MESFET device $C_{pg}$, Parasitic capacitance associated with the drain of a MESFET device $C_{pd}$, Parasitic gate inductance of a MESFET device $L_g$, Parasitic drain inductance of a MESFET device $L_d$, $L_s$, Parasitic source inductance of a MESFET device, Parasitic gate resistance of a MESFET device $R_g$, Parasitic drain resistance of a MESFET device $R_d$, and Parasitic source resistance of a MESFET device $R_s$, is independent of biasing conditions.

The main nonlinear elements include the drain source current ($I_{ds}$) gate capacitances $C_{gs}$ and $C_{gd}$, and diode $D_{gs}$ Gate-to-Source junction diode and $D_{gd}$ Gate-to-Drain junction diode $D_{gs}$, represents the forward-bias gate current, which is important in modeling device breakdown under inverted drain-source bias condition. Diode $D_{gd}$ gate to drain junction diode is included to model avalanche drain-gate current. With these nonlinear properties, the important are drain source current and the gate capacitances. They are included in most nonlinear GaAs MESFET models.
CHAPTER 4

NUMERICAL CALCULATIONS

The cross-sectional view of the n-channel GaAs MESFET is presented in the figure 25 below. At the drain and source the ohmic contacts are created, the gate is formed with a recessed structure in the N-type Gallium Arsanide channel with the schottky contact.

![Cross-sectional view of GaAs](image)

**Figure 25 Cross-sectional view of GaAs**

Two-dimension Poisson equation used in channel region, [56] is derived from

\[
\frac{\partial^2 \Phi(x,y)}{\partial x^2} + \frac{\partial^2 \Phi(x,y)}{\partial y^2} = \frac{qN_d^+}{\varepsilon}
\]  

(1)

From the above equation

Whereas

\( \Phi(x,y) \) Total electrostatic potential,

\( N_d^+ \) Ionization doping concentration,

\( q \) The electronic charge

\( \varepsilon \) permittivity.

The boundary conditions in the rectangular region are

\[ \Phi(0,y) = \Phi_{ss} + V_{DS} \]

\[ \Phi(0,y) = U(0) = \Phi_{s0} \]
\[
\frac{\partial \Phi(x,y)}{\partial y} + \frac{\partial U(y)}{\partial y} = 0
\]  

(2)

In the above equation
- \(\Phi_{n+i}\) Designated as the built-in potential across the gate/drain-to-substrate,
- \(U(y)\) 1-D Poisson solution,
- \(V_{DS}\) Applied drain voltage,
- \(\Phi_{s0}\) Potential at gate-channel surface
- \(L, a\) Length and depth of device channel.

From the Ref.[57] and Ref.[58], the potential \(\Phi(x,y)\) in the eq.(1) above is expressed as a superposition of two functions, \(U(x,y)\) and \(\Psi(x,y)\)” [57].

\[
\Phi(x,y) = U(x,y) = \Psi(x,y)
\]  

(3)

Where as from above equation \(U(x,y)\) and \(\Psi(x,y)\) should satisfy the following conditions

\[
\frac{\partial^2 \Psi(x,y)}{\partial x^2} + \frac{\partial^2 \Psi(x,y)}{\partial y^2} = 0
\]

\[
\frac{\partial^2 U(x,y)}{\partial x^2} + \frac{\partial^2 U(x,y)}{\partial y^2} = \frac{qNd + \epsilon}{\epsilon}
\]  

(4)

“At the threshold shift, the termination of all the field lines of the gate on the ionized donor charges which is in the completely depleted region of the channel. As the channel length is reduced, a portion of the vertical field lines at the surface terminates on source and drain instead”[58].

\[
E_{ys \min} = \left. \frac{\partial \Phi(x,y)}{\partial y} \right|_{y=0, x=x_0}
\]  

(5)

\[
X_0 = \beta L
\]  

(6)

Where

\[
\beta = \frac{L_{GS} + \frac{L}{2}}{L_{DS}}
\]

\(L_{GS}\) space length between gate and source
\(L_{GD}\) space length between drain and gate for the devices of asymmetric
Comparing to the $E_{ys\ min}$ is closely placed at center of channel of the device which has structure symmetrically between the gate and source terminals and to the low drain voltage operation.

$$E_{ys\ min} = \frac{\partial \phi(x,y)}{dy} \Big|_{y=0, x= \beta L} = \frac{qNd+}{\varepsilon_0 \varepsilon r} h(x) + \Delta E_{ys\ min}$$  \(7\)

Where $\Delta E_{ys\ min}$ is

$$\Delta E_{ys\ min} = \frac{\pi}{2a \sin \frac{\pi x}{2a}} \left\{ \left[ \frac{4(\phi_{ss} - \phi_{s0})}{\pi} \right] \frac{16}{\pi^3} \frac{qNd+}{\varepsilon} a * a \right\} \sinh \left( \frac{\pi \beta L}{2a} \right) +$$

$$\left[ \frac{4(\phi_{ss} - \phi_{s0}) + V_{ds}}{\pi} \right] \frac{16}{\pi^3} \frac{qNd+}{\varepsilon} a * a \right\} \sinh \left( \frac{\pi(1-\beta) L}{2a} \right)$$  \(8\)

To make the device off, a "voltage must be applied to gate to compensate the electric field. Thus the threshold voltage can be expressed" as [59].

$$V_T' = V_T + a \Delta E_{ys\ min}$$  \(9\)

The relation between the threshold voltage and the drain voltage can be obtained through [61].

$$V_T = V_{T0} + \lambda V_{DS}$$  \(10\)

There some unknowns in the above equations, they are formulated below [62].

$$\Phi_{bi} = \Phi_{bn} - \frac{Kt}{q} \ln \frac{N_C}{qNd}$$

$$\Phi_p = \frac{q*Nd+ * a^2}{2\varepsilon s}$$

$$\Phi_{n+i} = \Phi_{ss} = \frac{Kt}{q} \ln \frac{Nds*Na}{Ni2}$$

$$V_{T0} = \Phi_{bi} - \Phi_p$$

Where

$N_d$=Source to Substrate doping concentration

$N_C$=Effective density of states in the conduction band at 300K

$N_A$=Substrate doping concentration

$N_D$=Doping concentration
A physics based analytical model has been developed to study the behavior of the drain induced barrier lowering (DIBL). An analysis of the threshold voltage for short channel device on the \( \frac{L}{a} \) (channel length/channel depth) ratio, drain applied voltage \( V_{ds} \) and channel doping concentration \( N_d \) have been consider in this analytical model to study the behavior of DIBL effect.

The Figure 26 shows a plot of threshold voltage \( V_t \) versus drain voltage \( V_{ds} \) for channel doping concentration \( N_d \) of \( 4 \times 10^{17} \, \text{cm}^{-3} \) and source and drain \( N_d^+ \) of \( 10^{19} \, \text{cm}^{-3} \). The plot shows that the threshold voltage linearly increases with the increment of drain-source voltage \( V_{ds} \) and the device behaves as depletion (normally-on) type MESFET. The behavior of threshold voltage indicates that GaAs based MESFET has a short channel,

**Figure 26 Plot of drain Voltage (V_{ds}) versus threshold voltage (V_t)**

The Figure 26 shows a plot of threshold voltage \( V_t \) versus drain voltage \( V_{ds} \) for channel doping concentration \( N_d \) of \( 4 \times 10^{17} \, \text{cm}^{-3} \) and source and drain \( N_d^+ \) of \( 10^{19} \, \text{cm}^{-3} \). The plot shows that the threshold voltage linearly increases with the increment of drain-source voltage \( V_{ds} \) and the device behaves as depletion (normally-on) type MESFET. The behavior of threshold voltage indicates that GaAs based MESFET has a short channel,
where the electric field at high drain voltage makes the drain induced barrier lowering to reduce the threshold voltage. The plot has been drawn using the Equation (10).

![Plot of Threshold voltage (V_t) versus channel length](image)

**Figure 27** Plot of Threshold voltage (V_t) versus channel length for different N_d and the ratio of channel length and active channel depth

Figure 27 is presents a plot of threshold voltage (V_t) versus channel length (L) for different N_d and the ratio of channel length and active channel depth (L/a). The threshold voltage exponentially increases with the increment of channel length from 1.5x10^{-4} cm to 1.8x10^{-4} cm. The maximum value of threshold voltage can be obtained by selecting doping concentration of 10^{17} cm^{-3} and 2x10^{17} cm^{-3} for L/a = 2 and 3. The minimum value of threshold voltage can be obtained by selecting doping concentration of 10^{17} cm^{-3} and 2x10^{17} cm^{-3} for L/a = 2 and 3.
Figure 28 Plot of channel Doping Concentration (N<sub>d</sub>) ratio versus Threshold voltage (V<sub>t</sub>) for different substrate concentration (Na)

The figure 28 shows a plot of threshold voltage (V<sub>t</sub>) versus channel doping concentration (N<sub>d</sub>) for different substrate concentration N<sub>a</sub> = 1x10<sup>15</sup> cm<sup>-3</sup>, 5x10<sup>15</sup> cm<sup>-3</sup> and 10<sup>16</sup> cm<sup>-3</sup>. The plot shows that the threshold voltage significantly reduces with channel doping concentrations. The properties of the plot show that the channel doping concentration significantly control the threshold voltage compared to the substrate concentration. It can be anticipated that the enhancement and depletion MESFET can be fabricated by changing the channel doping concentration. This plot has been formed by using the Equation (8) and (9).
Figure 29 Plot of Extent electric field induced by DIBL $\Delta E_{ys\ min}$ and drain-source voltage ($V_{ds}$) for different channel doping concentrations $N_d$

Figure 29 Plot of extent electric field induced by DIBL $\Delta E_{ys\ min}$ and s drain & source voltage ($V_{ds}$) for different channel doping concentrations $N_d = 1 \times 10^{17}\ cm^{-3}$, $2 \times 10^{17}\ cm^{-3}$, $3 \times 10^{17}\ cm^{-3}$ and $4 \times 10^{17}\ cm^{-3}$. The extent electric field induced by DIBL $\Delta E_{ys\ min}$ linearly increases with the increment of drain-source voltage due to large electric field generated at the drain side. The plot describes that large channel concentration gives high value of extent electric field induced by DIBL $\Delta E_{ys\ min}$. This plot concludes the effect of high doping is required to reduce the DIBL effect of GaAs MESFET. This plot has been formed by using the Equation (8) and (10).
Figure 30 Doping Concentration $N_d$ versus extent electric field

induced by DIBL $\Delta E_{ys\text{min}}$

Figure 30 presents an interesting plot of doping Concentration $N_d$ versus extent electric field induced by DIBL $\Delta E_{ys\text{min}}$. The extent electric field induced by DIBL $\Delta E_{ys\text{min}}$ linearly increases with the increment of doping concentration. This plot shows that large doping concentration gives the significant effect on extent electric field induced by DIBL $\Delta E_{ys\text{min}}$. This plot has been drawn by using the Equation# 8.
Figure 31 Plot of Channel Length (L) versus Electric field $E_{ys\,min}$

Figure 31 is a plot of Channel Length (L) versus Electric field $E_{ys\,min}$. The electric field $E_{ys\,min}$ linearly increases with the increment of the channel length for channel doping concentration of $10^{16}$ cm$^{-3}$. It is observed that the electric field is small for narrow channel length compared to higher channel length. Hence the narrow channel length with low electric field suppresses the DIBL effects. The plot has been framed by using the Equation# (7) and (8).
CONCLUSION 6

The analytical model mainly describes the DIBL effect on short channel MESFETs device. A relationship of drain voltage model derived from the 2D Poisson’s equation has been established to find the properties of sub threshold region. The threshold voltage linearly increases with the increment of drain-source voltage $V_{ds}$ and the DIBL effect is occurred when the threshold voltage exponentially increases with the increment of channel length.

The DIBL effect is extent electric field in the drain region induced by DIBL $\Delta E_{ys_{\text{min}}}$, which is linearly increasing with the increment of drain-source voltage due to large electric field generated at the drain side. The large doping concentration gives the significant effect on extent electric field induced by DIBL $\Delta E_{ys_{\text{min}}}$. The electric field $E_{ys_{\text{min}}}$ linearly increases with the increment of the channel length for channel doping concentration. It is observed from the study that the DIBL effect is a dominant factor for short channel devices.
BIBLIOGRAPHY

REFERENCES

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[60] Chunlin Zhu,Rusli,Chin-Che Tín,Soon Fat Yoon,Jaeshin Ahm,"Drain-induced barrier lowering effect and its dependence on the channel doping in 4H-SiC MESFETs", Proceedings. 7th International Conference on Solid-State and Integrated Circuits Technology, 2004 p.2309
APPENDIX –A

k  Boltzmann constant

T  Absolute temperature at 300K

ε  Permittivity of semiconductor

q  Electronic charge

L  Channel length

μ  Carrier mobility

N_A  Substrate doping concentration

N_D  Doping concentration

N_ds  Source to Substrate doping concentration

L_{GS}  Space between gate and source

L_{DS}  Space between drain and source

α  Optical absorption coefficient

a  Active channel thickness

D  Diffusion constant for post-implanted annealing process

t  Annealing time

R_p  Implant range parameter

σ  Straggle parameters

\phi_{s0}  Potential at gate-channel surface

\phi_{n+i}  Built in potential across gate/drain - substrate
$V_{bi}$  Built-in voltage of active channel and substrate junction

$V_{BS}$  Substrate-to-source voltage

$V_{GS}$  Gate-source voltage

$V_T$  Threshold voltage

$V_P$  Pinch off voltage

$V_{DS}$  Drain-source voltage

$N_C$  Effective density of states in the conduction band at 300K

$R$  Surface recombination rate

$n_i$  Intrinsic carrier concentration

$E_{ys \ min}$  Surface Electric Field

$\Delta E_{ys \ min}$  Extent Electric Field induced by DIBL Effect

$a\Delta E_{ys \ min}$  DIBL-induced Short channel threshold voltage shift

APPENDIX –B

Mat lab codes

%********** Results for 'Drain Voltage Vs Threshold Voltage'***********%

clear all;
cle;
close all;
Na= 3*(10^15);

ni = 1.79*(10^6);

Nd = 4*(10^17);

Nds=1*(10^19);

Nc = 4.7*(10^17);
\[ q_{ss} = 0.0259 \cdot \log\left(\frac{Na \cdot Nds}{ni^2}\right); \]

\[ q_{so} = 0.8; \]

\[ E = 1.2 \times 10^{-14}; \]

\[ q = 1.60218 \times 10^{-19}; \]

\[ a = 0.5 \times 10^{-4}; \]

\[ L_{gs} = 0.25 \times 10^{-4}; \]

\[ L_{ds} = 1.25 \times 10^{-4}; \]

\[ SI_{bn} = 1.24; \]

\[ SI_{bi} = SI_{bn} - (0.0259 \cdot \log(Nc/Nd)); \]

\[ SI_{bp} = \frac{q \cdot Nd \cdot (a^2)}{2 \cdot E}; \]

\[ V_{to} = SI_{bi} - SI_{bp} \]

\[ L_{m} = 0.5; \]

\[ L = 1.5 \times 10^{-4}; \]

\[ v_{ds} = [0.2, 0.4, 0.6, 0.8, 1, 1.2, 0, 1.4]; \]

\[ \text{for } i = 1:8 \]

\[ V_{t} = V_{to} + (L_{m} \times v_{ds}(i)); \]

\[ b = \frac{L_{gs} + (L/2)}{L_{ds}}; \]

\[ f = \pi \sqrt{(2 \cdot a \cdot \sin((\pi \cdot L)/(2 \cdot a)))}; \]

\[ k = \frac{(16 \cdot q \cdot Nd \cdot (a^2))/((\pi^3) \cdot E)}{((\pi^3) \cdot E)}; \]

\[ h = \frac{4 \cdot (q_{ss} - q_{so} + v_{ds}(i))}{\pi}; \]

\[ p = \sin((\pi \cdot b \cdot L)/(2 \cdot a)); \]

\[ g = h + (v_{ds}(i)/\pi); \]

\[ j = \sin((\pi \cdot (1-b) \cdot L)/(2 \cdot a)); \]
\[ Ey = f^*(((h*k)*p) + ((g*k)*j)); \]

\[ Vt1(i) = (Vt + (a*Ey)); \]

end

Vt1

Ey

hold on;
plot(vds,Vt1,'-rs');
title('Drain Voltage Vs Threshold Voltage');
xlabel('Drain Voltage, Vds, (V)');
ylabel('Threshold Voltage, Vt, (V)');
text(0.4,-1.219,\textarrow\text{Vds=0.4v,Vt= 1.219}', 'FONTSIZE',12)
grid on;

%********* Results for 'Channel Length Vs Threshold Voltage'***********%
clc;
close all;

Na = 3*(10^{15});

ni = 1.79*(10^6);

Nd = [1*(10^{17}) 2*(10^{17})];

Nds = 1*(10^{19});

Nc = 4.7*10^{17};

qso = 0.8;
E = 1.2*(10^-14);
q = 1.60218*(10^(-19));
a = 0.5*(10^-4);
Lgs = 0.25*(10^-4);
Lds = 1.25*(10^-4);
vds = 10;
SIbn=1.24;
Lm=0.5;
qss = 0.0259 *(log((Na*Nds)/(ni^2)));
La= [ 2 3 ];
L1=[1.50*(10^-4) 1.55*(10^-4) 1.6*(10^-4) 1.65*(10^-4) 1.7*(10^-4) 1.75*(10^-4) ];
a1=[ 0.75*(10^-4) 0.775*10^-4 0.8*(10^-4) 0.825*(10^-4) 0.85*(10^-4) 0.875*(10^-4) 0.9*(10^-4) 0.925*(10^-4) ];
L2=[1.50*(10^-4) 1.55*(10^-4) 1.6*(10^-4) 1.65*(10^-4) 1.7*(10^-4) 1.75*(10^-4) ];
a2=[ 0.5*(10^-4) 0.5166*(10^-4) 0.533*(10^-4) 0.55*(10^-4) 0.566*(10^-4) 0.583*(10^-4) ];
vds = 1;
for x=1:2
  for i= 1:6
    SIbp= (q*Nd(x)*((a1(i))^2))/(2*E);
    SIbi = SIbn -(0.0259*log(Nc/Nd(x)));
    Vto = SIbi - SIbp;
    Vt = Vto + (Lm*vds);
    b = (Lgs + (L1(i)/2))/Lds;
  end
end
\[ f = \pi/(2*a1(i)\sin((\pi*L1(i))/(2*a1(i)))); \]
\[ k = ((16*q*Nd(x)*(a1(i)^2))/((\pi^3)*E)); \]
\[ h = (4*(qss-qso))/\pi; \]
\[ p = \sin((\pi*b*L1(i))/(2*a1(i))); \]
\[ g = h+(vds/\pi); \]
\[ j = \sin((\pi*(1-b)*L1(i))/(2*a1(i))); \]
\[ Ey = f*((h*k)*p) + (g*k)*j; \]
\[ Vt1(x,i) = (Vt +a1(i)*Ey); \]

\end{end}

\begin{for} x=1:2 \end{for}

\begin{for} i=1:6 \end{for}

\[ SIbp1= (q*Nd(x)*(a2(i)^2))/(2*E); \]
\[ SIbi1 = SIbn - (0.0259*\log(Nc/Nd(x))); \]
\[ Vto1 = SIbi1 - SIbp1; \]
\[ Vt2 = Vto1 + (Lm*vds); \]
\[ b1= (Lgs + (L2(i)/2))/Lds; \]
\[ f1 = \pi/(2*a2(i)\sin((\pi*L2(i))/(2*a2(i)))); \]
\[ k1 = ((16*q*Nd(x)*(a2(i)^2))/((\pi^3)*E)); \]
\[ h1 = (4*(qss-qso))/\pi; \]
\[ p1 = \sin((\pi*b1*L2(i))/(2*a2(i))); \]
\[ g1 = h1+(vds/\pi); \]
\[ j1 = \sin((\pi*(1-b1)*L2(i))/(2*a2(i))); \]
\[ Ey1 = f1*((h1*k1)*p1) + (g1*k1)*j1); \]
Vt3(x,i) = (Vt2 +(a2(i)*Ey1));

end
end

Ey1
Vt3

hold on;

plot(L1,Vt1);

plot (L2,Vt3);

title('Channel Length Vs Threshold Voltage');

leh1 = legend( 'Nd=1*(10e17) L/a =2','Nd=2*(10e17),L/a=2','Nd=1*(10e17),L/a=3','Nd=2*(10e17),L/a=3');

xlabel('Length ,L (cm)');

ylabel('Threshold Voltage, Vt, (V)');

grid on;

hold off;


%*********** Results for ‘Dopic Concentration Vs Threshold Voltage’ ***********%

clc;

close all;

Nds= 10^19

Na= [1*(10^15) 5*(10^15) 10*(10^15)];

ni = 1.79*(10^6);
Nd = [1*(10^17) 2*(10^17) 3*(10^17) 4*(10^17)];

Nc = 4.7*10^17;
qso = 0.8;

E = 1.2*(10^-14);
q = 1.60218*(10^-19);
Lgs = 0.25*(10^-4);
Lds = 1.25*(10^-4);
vds = 1;
SIbn = 1.24;
Lm = 0.5;
L = 1.5*(10^-4);
a = 0.5*(10^-4);
vds = 1;
for x = 1:3
  for i = 1:4
    qss = 0.0259*(log((Na(x)*Nds)/(ni^2)));  
    SIbp = (q*Nd(i)*(a^2))/(2*E);
    SIbi = SIbn - (0.0259*log(Nc/Nd(i)));
    Vto = SIbi - SIbp;
    Vt = Vto + (Lm*vds);
  end
end
b = (Lgs + (L/2))/Lds;
f = pi/(2*a* sinh((pi*L)/(2*a)));
k = ((16*q*Nd(i)*(a^2))/((pi^3)*E));
h = (4*(qss-qso))/pi;
p = sinh((pi*b*L)/(2*a));
\[ g = h + \frac{v_ds}{\pi}; \]
\[ j = \sin\left(\pi(1-b)L/(2a)\right); \]
\[ Ey = f\left(\left(\frac{h}{k}\right)p + \left(\frac{g}{k}\right)j\right); \]
\[ Vt(x,\hat{i}) = (Vt + (a\times Ey)); \]
\[ \text{end} \]
\[ \text{end} \]

\[ Vt1 \]
\[ Ey \]

\[ \text{plot}(Nd, Vt1); \]
\[ \text{title('Doping Concentration Vs Threshold Voltage');} \]
\[ \text{hle1} = \text{legend( 'Na=1*(10e15)','Na=5*(10e15)','Na=10*(10e15)');} \]
\[ \text{xlabel('Doping Concentration,Nd, (Cm^-3)');} \]
\[ \text{ylabel('Threshold Voltage, Vt, (V)');} \]
\[ \text{grid on;} \]

\%**Results for 'Drain Source Voltage Vs Extent electric field induced by DIBL effect**
\%**

\[ \text{clear all;} \]
\[ \text{clc;} \]
\[ \text{close all;} \]
\[ \text{Nd} = 1 \times (10^{19}); \]
\[ \text{Na}= 3 \times (10^{15}); \]
\[ \text{ni} = 1.79 \times (10^{6}); \]
Nd = [1*(10^17) 2*(10^17) 3*(10^17) 4*(10^17)] ;
Nc = 4.7*(10^17);
qso=0.8;
E = 1.2*(10^-14);
q = 1.60218*(10^-19);
a = 0.5*(10^-4);
Lgs = 0.25*(10^-4);
Lds = 1.25*(10^-4);
vds = [1 2 3 4 5 6 7 8 9 10] ;
SIbn=1.24;
SIbi = SIbn -(0.0259*log(Nc/Nds))
Lm=0.5;
L=1.5*(10^-4) ;

for x= 1:4
for i= 1:10
 qss = 0.0259 *(log((Na*Nds)/(ni^2)))
 SIbp= (q*Nd(x)*(a^2))/(2*E)
 Vto = SIbi - SIbp;
 Vt = Vto + (Lm*vds(i));
 b = (Lgs + (L/2))/(Lds);
 f = pi/(2*a*sinh((pi*L)/(2*a)));

k = ((16*q*Nd(x)*(a^2))/((pi^3)*E));

h = (4*(qss-qso+vds(i)))/(pi);

p = sinh((pi*b*L)/(2*a));

g = h+(vds(i)/pi);

j = sinh((pi*(1-b)*L)/(2*a));

Ey(x,i) = f*(((h*k)*p) + ((g*k)*j));

Vt1(x,i) = (Vt + (a*Ey(x,i)));

end
end

Vt1

Ey
clf;
hold on;
grid on;
plot(vds,Ey);
hleh1 = legend('Nd=1*(10e17)', 'Nd=2*(10e17)', 'Nd=3*(10e17)', 'Nd=4*(10e17)');
title('Drain Source Voltage Vs DEymin');
xlabel('Drain Source Voltage, Vds, (V) ');
ylabel('DEymin, (V/Cm)');

%**Results for ‘Doping Concentation Vs Extent electric field induced by DIBL effect
*%:
clear all;
clc;
close all;
\[ Nds = 1 \times (10^{19}); \]
\[ Na = 3 \times (10^{15}); \]
\[ ni = 1.79 \times (10^6); \]
\[ Nd = [0.5 \times (10^{17}) \ 1 \times (10^{17}) \ 1.5 \times (10^{17}) \ 2 \times (10^{17}) \ 2.5 \times (10^{17}) \ 3 \times (10^{17}) \ 3.5 \times (10^{17})]; \]
\[ Nc = 4.7 \times (10^{17}); \]

\[ qso = 0.8; \]
\[ E = 1.2 \times (10^{-14}); \]
\[ q = 1.60218 \times (10^{-19}); \]
\[ a = 0.5 \times (10^{-4}); \]
\[ Lgs = 0.25 \times (10^{-4}); \]
\[ Lds = 1.25 \times (10^{-4}); \]

\[ vds = 1; \]
\[ SLbn = 1.24; \]
\[ SLbi = SLbn - (0.0259 \times \log(Nc/Nds)) \]

\[ Lm = 0.5; \]
\[ L = 1.5 \times (10^{-4}); \]

\[ \text{for } i = 1:7 \]
\[ \quad qss = 0.0259 \times \log((Na \times Nd(i))/(ni^2)) \]
\[ \quad SLbp = (q \times Nd(i) \times a^2)/(2 \times E) \]
\[ \quad Vto = SLbi - SLbp; \]
\[ \quad Vt = Vto + (Lm \times vds); \]
b = (Lgs + (L/2))/(Lds);
f = p/(2*a*sinh((pi*L)/(2*a)));
k = ((16*q*Nd(i)*(a^2))/((pi^3)*E));
h = (4*(qss-qso+vds))/(pi);
p = sinh((pi*b*L)/(2*a));
g = h+(vds/pi);
j = sinh((pi*(1-b)*L)/(2*a));
Ey(i) = f*(((h*k)*p) + ((g*k)*j));
Vt1(i) = (Vt + (a*Ey(i)));
end

Vt1
Ey
clf;
hold on;
grid on;
plot(Nd,Ey,'--rs');
title('Doping Concentration Vs DEys min');
xlabel('Doping Concentration, Nd ');
ylabel('DEys min, (V/Cm)');
text(2*10^17,8.009*10^7,'\leftarrow (Nd=2e17,DEys min=8.009e7)\', 'FONTSIZE',10);

%***********Results for 'Channel Length Vs Surface Electric Field *************%
clear all;
clc;
close all;
Nds = 1*(10^19);
Na= 3*(10^14);
i = 1.79*(10^6);
Nd = 4*(10^16);
Nc = 4.7*(10^17);

qso=0.8;
E = 1.2*(10^-14);
q = 1.60218*(10^(-19));
a = 0.5*(10^-4);
Lgs = 0.25*(10^-4);
Lds = 1.25*(10^-4);

vds = 1;
SIbn=1.24;

SIbi = SIbn - (0.0259*log(Nc/Nd))

Lm=0.5;

L=[ 1.50*(10^-4) 1.55*(10^-4) 1.6*(10^-4) 1.65*(10^-4) 1.7*(10^-4) 1.75*(10^-4) 1.8*(10^-4)];
for i= 1:7
    qss = 0.0259*(log((Na*Nds)/(ni^2)))
    SIbp= (q*Nd*(a^2))/(2*E);
    Vto = SIbi - SIbp;
    Vt = Vto + (Lm*vds);
\[ b = \frac{(L_{gs} + (L(i)/2))/Lds}{\pi} \]
\[ T = \frac{\pi \cdot L(i)}{2 \cdot a} \]
\[ f = \frac{\pi \cdot \sinh(T)}{2 \cdot a \cdot \sinh(T)} \]
\[ k = \frac{(16q^2Nd/a^2)/((\pi^2/E))}{(4*(qss-qso)/(\pi))} \]
\[ h = \frac{((16q^2Nd/a^2)/((\pi^2/E))}{(4*(qss-qso)/(\pi))} \]
\[ p = \frac{\sinh((\pi b L(i)/(2 \cdot a))}{\sinh((\pi b L(i)/(2 \cdot a))} \]
\[ g = h + (vds/\pi) \]
\[ j = \sinh((\pi^2/(1-b) L(i))/(2 \cdot a)) \]
\[ Ey(i) = f^2(((h^2k)^2+p)^2 + ((g^2k)^2 j))) \]
\[ Vt1(i) = (Vt + a \cdot Ey(i)) \]
\[ Eys(i) = ((q*Nds)/E) \cdot b \cdot L(i) + Ey(i) \]

**end**

Vt1

Eys
clf;
hold on;
grid on;
plot(L,Eys,'--rs');
title('Channel Length Vs Eymin');
xlabel('Channel Length, (L) (Cm)');
ylabel('Eymin, (v/Cm-3)');

```
text(1.7e-4, 1.9*(10^10), 'L=1.7e-4, Eymin=1.9e10');
```