A Physics based Analytical Model for GaN MISFET’s

A graduate project submitted in partial fulfillment of the requirements
For the degree of Master of Science in Electrical Engineering

By

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Abstract

A Physics based Analytical Model for GaN MISFET’s

By

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Master of Science in Electrical Engineering

A physics based one dimensional analytical model for modeling GaN MISFET has been developed. The developed model computes parameters such as transconductance, gate-source capacitance and drain-source current. The fundamental aim of the project is to analyze the frequency response of the GaN MISFIT by evaluating the parameters such as gate-source capacitance and transconductance. The study based on analytical model computes the transconductance and gate-source capacitance in the current-saturation region in order to evaluate the frequency response of the GaN MISFET. The vital necessity for computing the frequency response of the devices is to study the effect of physical dimensions such as gate length insulator thickness and the gate biasing on the frequency behavior of the MISFET device. The extracted device characteristics from the analytical model were found to be similar to the theoretical properties such as I-V characteristics and intrinsic parameters of MISFET devices.
Chapter 1 Introduction

1.1 Gallium Nitride Metal Insulation Semiconductor Field Effect Transistor

Silicon being one of the most abundant material in the world has been acquired to manufacture solid state devices since 19th century [1]. The advantages of the solid state industries moves towards silicon are because of its low cost and ease of use. Industrialists believed that solid state industry has reached the saturation since the advent of silicon [1] and if at all a change has to be brought a new compound which is better than silicon need to be developed. One such compound which brought about the change is Gallium Nitride (GaN). Yet another compound which was better than silicon is Silicon carbide. The characteristics of the three compounds are tabulated below.

<table>
<thead>
<tr>
<th>Properties</th>
<th>Description</th>
<th>GaN</th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eg (eV)</td>
<td>Bandgap Energy</td>
<td>3.4</td>
<td>1.12</td>
<td>3.2</td>
</tr>
<tr>
<td>$E_{BR}$ (MV/cm)</td>
<td>Crystal electric field for breakdown in crystal</td>
<td>3.3</td>
<td>0.3</td>
<td>3.5</td>
</tr>
<tr>
<td>$\mu$ (cm²/Vs)</td>
<td>Mobility of electrons</td>
<td>990-2000</td>
<td>1500</td>
<td>650</td>
</tr>
</tbody>
</table>

Table 1.1: Material Properties of Gallium Nitrate, Silicon and Silicon Carbide
From the Table 1.1 the parameters which define the performance measure of compounds used to construct Metal Insulation Semiconductor Field Effect Transistor (MISFET) are conduction efficiency, switching efficiency, breakdown voltage, cost and size. These characteristics are used to study the power density and the system frequency. From the above table it can be observed that the theoretical values of Gallium Nitride fair better than Silicon Carbide and Silicon. The breakdown voltage defines the limit of resistance the semiconductor device can provide when high electric field is applied [2]. Gallium Nitride offers very high breakdown voltage and also allows better mobility of elections [3]. Overall Gallium Nitride would be the best choice to develop a transistor. Due to the wide bandgap energy reduces the possibility of valence electrons in the valence band jumping into conduction band reduce, therefore the noise in the system decreases.

In today’s world Gallium Nitride has replaced silicon in variety of applications especially the electronic and optoelectronic devices which consume high power [1]. Gallium Nitride has found to be the best choice of transistors which work at high frequency and high power [1]. One of the added advantages of using Gallium Nitride is that it offers high electron drift velocity, therefore by default it has resistance to be operated at high temperatures [1]. Gallium Nitride also has wide bandgap energy approximately 3.4eV at room temperature, whereas silicon and silicon carbide offer 1.12eV and 1.42eV respectively [2]. Also the large bandgap in the semiconductor makes the device more sensitive and can be used as detectors in the ultra violet range [3]. Recently studies have been carried out on constructing alloys manufactured using gallium
Nitride and silica to get the merits of both the compounds [4]. AlGaN/GaN hector structure is one such alloy which has been developed and has been widely used in the fabrication of photo detectors and light emitting diodes. One of the main reason which contributes to the fall of Gallium Nitride is that it has large lattice structures[5] and thermal mismatch, hence gallium nitride film constructed over gallium nitride buffers contribute lesser ionization than the gallium nitride film grown with AIN buffer layers.

1.2 High RF Power in Gallium Nitride devices

The GaN devices address the high power requirements in microwave devices. Gallium Nitrate has a very high band gap of approximately 3.4 eV, a very optimal velocity of around 1.4cm/s and also possess a flat field of almost 1500cm\(^2\)/Vs. A device or material which is as flat as 1500 cm\(^2\)/Vs is suitable for high power applications. Recent advancements in this fields has made the GaN HEMTs with an adorable force yield of around 9.7 W/mm at 8.1 GHz has been proved. Using GaN as the substrate, Gallium Nitrate FETs have been elevated, as pin pointed by Daumiller [6]. It possesses an “electron velocity of 3 x 10\(^7\) cm/s” and has a dielectric with a very low capacitance value. The “GaN Materials” exhibits very high potential to be operated periodically [6, 7].

Gallium Nitride (GaN) is a good material to be used to fabricate the electronic and optical applications which need a good operating temperature, wide range of frequencies and can be operated at high power [8]. While under a few conditions, the microwave transistors are recognized by admittance (Y) and scattering (S) parameters. In the relatively recent past, S.S. Islam and A.F.M Anwar have shown non-linearity's in GaN MESFETs using material science based model which considers trans-conductance [8].
FETs constructed using the Gallium Nitrate structures can operate at a very high speed and have a high switching speed in comparison with Gallium Arsenide and Silicon. Theoretical FETs have an optical power density of around 20W/mm. The high power density will contribute in increasing the temperature of the channel and thermal stability of structures becomes of vital importance [12] GaN has a very high thermal sensitivity of around 750 degree Celsius.

The MISFET's are broadly been utilized for their energy enhancement capacities [13]. For microwave power intensification, InP MISET's are utilized monetarily because of the properties of InP material. The InP MISFET has a force yield of 1.8 W/mm gate width close by an addition of 2.8 dB and an included force effectiveness of 20% at its working frequency of 30GHz. The force enhancement of the InP MISFET can be mulled over utilizing two numerical models specifically two-dimensional recreation taking into account the Poisson's mathematical statement and the pseudo two-dimensional model [14]. These models give the most exact depiction of InP MISFET both in upgrade and consumption modes.

The GaN based power switching transistors have been replacing Si-based MOSFET’s and IGBT’s due to its ability to transfer high power alongside, high switching speed. The GaN based transistor is also found to have the highest breakdown voltage ever which is approximately 10400V and exhibits an ability to operate at a very high frequency of 203 GHz and has small signal gain of 22dB at 26 GHz with a 3dB bandwidth of 25-29 GHz.
Chapter 2 Properties Gallium Nitride Material

2.1 Selection of Gallium Nitride (GaN)

Gallium Nitride is better than Silicon in Silicon carbide in terms of not being vulnerable towards temperature, speed and can be operated in high power [12]. Gallium Nitride also showcases the essential features needed for innovations in terms of efficiency.

Gallium Nitride also displays unique electrical and electronic characteristics, such as high current density, high dielectric strength, and ability to be operated at high temperature, low cut-in resistance and high speed switching [13]. Gallium Nitride also offers exceptionally high carrier mobility electrical breakdown and three times the bandgap in comparison with silicon [13].
Figure 1: Advantages of Gallium Nitride

Few other advantages of Gallium Nitride over Gallium Arsenide are as shown in the Figure 2.1, low voltage drop for high output power, Gallium Nitride can be used in construction of unipolar devices unlike Gallium Arsenide, also Gallium Nitride provides high transient characteristics and improved switching speed. Gallium Nitride also has the ability to work at high temperature and produces less electrical noise.

2.2 Crystal Structures of Gallium Nitride

Gallium Nitride is available both in molecular and crystalline structures [14]. The crystalline structure can be explained using Wurtzite and Zincblende structures.
2.2.1 Wurtzite Structure versus Zincblende Structure

The Wurtzite Gallium Nitride structure and Zincblende Gallium Nitride structure are very closely related however they have several dissimilarities. The Zincblende structure has tetrahedral bonding with its neighboring molecules and Wurtzite structure has hexagonal bonding along the C-axis with the atoms of the same element to form the stacking pattern. The stacking pattern of the Zincblende lattice is given by

…GaANAGaBNBGaCNCGaANAGaBNBGaCNC…

The stacking pattern of the Wurtzite arrangement is given by

…GaANAGaBNBGaANAGaBNBGaANAGaBNB…

The atomic projection of the “Wurtzite structure” is given by the Figure 2.2 below. The figure shows the face group of the structure which is \(C_{6v}^4\). the Lattice structure constants ‘a’ and ‘b’ are equal for the structure. The Gallium atoms are spaced at the coordinates (0, 0, 0) and at (2/3, 1/3, 1/2). The Nitride atoms are spaced at the coordinates (0, 0, u) and (1.5, 0.33, 0.5+u). where ‘u’ is around “3/8”. At this value of ‘u’ the Wurtzite structure approximates to zinc plate structure. This is because the coordinate with u=3/8 changes the hexagonal structure to a tetrahedral.
Figure 2: Wurtzite structure of Gallium Nitride

The atomic projection of the Zincblende model is given by the Figure 2.3 below. From the Figure 2.3 the parameters of the gallium Nitride such as energy gap, ideal angle and distance between the two nearest neighbors can be computed. Zincblende structure is not chosen for GaN, only for some special cases Zincblende is considered. The values for the given Zincblende structure is given to be

- Energy gap between the bands = 3.2eV.
- The angle between the atoms at ideal state = 109.47°
- The Distance between the nearest neighbor = 19.5nm
2.2.2 Polar Material and Structures

Polar materials are been used in manufacturing of semiconductor devices since the advent of materials like indium, aluminum, gallium based alloys in the electronics and optoelectronics [15]. These materials are different from the conventional cubic semiconductors at the abstract level and the exhibit strong polarization in the C direction.

To understand the effect of polar materials it is important to have knowledge on the effects caused by polarization fields on the electrical properties of the material.

2.2.3 C-plane bulk GaN Substrates

The advantage of building a substrate using C-plane Gallium Nitride is that it can offer strong polarization along the C-direction [15]. In order to obtain Bulk Substrate semiconductor epitaxy is performed over the native Gallium Nitrate substrate which will minimize the interface effects and defect formation. The bulk gallium nitride substrate
have better lattice constant mismatch dislocation density and thermal conductivity in comparison with hetero-epitaxial gallium nitride on silicon carbide, sapphire or silicon.

2.2.4 Growth of Wurtzite GaN onto Sapphire

Gallium Nitride can be developed over gallium nitride and sapphire film in order to achieve high energy gap separation. Also, the energy separation A-valley, spinning orbital and crystal field. The energy gap structure of gallium nitride over gallium nitride and sapphire is shown in the Figure 2.4 below.

Figure 4: Growth of Wurtzite GaN on Sapphire Substrate

However, gallium nitride lattice over gallium nitride and sapphire is not performed commercially like bulk gallium nitride over gallium nitride because they offer large lattice mismatch and thermal mismatch [17].

The block diagram of developing gallium nitride over gallium nitride and sapphire substrate is shown below in Figure 2.5.
Figure 5: Schematic illustration of GaN growth onto GaN & Sapphire Substrate

2.3 Energy band Structure of GaN

The gallium nitride can be explained using Zincblende structure and the Wurtzite structure. The Figure 2.6 shows that the Zincblende structure has an energy gap of 3.2eV and the energy of the X-valley is 4.6eV and the energy of the L-valley is around 4.8eV and 5.1eV.
The Wurtzite structure has A-valleys and the M-L-Valleys and they have an energy of 4.7eV and 4.5 eV respectively. The energy gap in this case is around 3.39 eV and is a much more suitable choice for fabrication of a high power MISFET. These characteristics are depicted in the Figure 2.7.
2.4 Electrical Properties of GaN

Gallium nitride based semiconductor materials have raised up exponentially the past decade and has become one of the most import commercial semiconductor material [17]. This is because of the excellent electrical and optical properties of gallium nitride. Gallium nitride can provide high power, high speed in comparison to silicon.

The band gap of the gallium nitride varies between 3.4eV and 6.2eV which is very high in comparison to other semiconductor materials available [18]. This insures that the majority carriers in the valence band to not enter into the conduction band making it strong detector to operate in the ultra violet range. The electron mobility is very less and is approximately around 900 cm²/Vs in comparison to silicon which is 1400 cm²/Vs and germanium 3900 cm²/Vs. Making it a very stable device. Similar to electron
mobility the hole mobility in the gallium nitride material is also very less and it is around 10 cm$^2$/Vs. whereas germanous has 1900 cm$^2$/Vs and silicon has 450 cm$^2$/Vs.

Yet another electrical property which makes gallium nitride the best choice for high power applications, the thermal conductivity and gallium nitride has a conductivity of 110 W/mK, whereas germanium has a conductivity of 58 W/mK. The thermal expansion coefficients is found to be around 5.4 to 7.2.

Few of the most important parameters of gallium nitride are listed below.

- Bandgap = 3.44eV
- Lattice constant = 3.189 Armstrong
- Breakdown field = 3.3*10$^6$ V/cm
- Dielectric constant = 9.5 at static and 5.35 at high frequency

Band to band luminescence is detected at room temperature in a high quality gallium nitride. This property is called yellow luminescence and it is centered on 560nm and can be witnessed in undoped and silicon doped gallium nitride layers. These yellow emissions make gallium nitride a shallow donor to an acceptor making it and optically strong device.

Gallium nitride layer also contribute to ionized impurity scattering and acoustic phonon scattering making it an optically strong device. Few of the optical properties of gallium nitride are listed below.

- Optical phonon energy = 91.8meV
- Ionization energy = 12meV
2.4.1 Excitation Energy versus Temperature

To understand the excitation energy and its relationship with the temperature of operation, we will have to follow Wurtzite structure of gallium nitride. On doing practical analysis the relationship between the excitation energy and temperature is given from the Figure 2.8, and can be computed by

\[
E_g (T) - E_g (0) = \frac{-5.08 \times 10^{-4} \times T^2}{996 - T}
\]

Where ‘Eg’ is defined as excitation energy gap and the ‘T’ is the temperature in Kelvin.

Figure 8: Excitation Energy Vs Temperature
2.4.2 Bandgap Energy versus Temperature

Gallium Nitride has high band gap energy and can be operated at variety of temperatures [19]. The relationship between the bandgap and the temperature is shown in the Figure 2.9 below.

![Figure 9: Bandgap Energy Vs Temperature](image)

2.4.3 Intrinsic Carrier Concentration versus Temperature

The dopant and acceptor concentration in a semiconductor device built using gallium nitride for both Zincblende model and Wurtzite model is shown in the Figure 2.9 below.

From the Figure 2.10, it can be observed that the intrinsic carrier Concentration is inversely related to the temperature.
2.4.4 Drift Velocity versus Electric Field

From the Figure 2.11 shown below, it is clearly seen that the Drift Velocity of GaN is high for the considered electric field compared to SiC, Si and GaAs. So for higher drift velocity GaN is considered for the fabrication of MISFET.
2.5 Thermal Properties of GaN

Gallium Nitride is also known for its high peak electron velocity, high electron sheet density, and high breakdown voltage [20]. Therefore the transistors built using gallium nitride have demonstrated extremely remarkable DC and radio frequency characteristics. Some of the important thermal and mechanical properties are listed below. Drain current density equals 1.43A/mm.

- Breakdown voltage equals 340V between gate and drain
- Maximum frequency = 140GHz
- Output power density = 3.3W/mm
• Output power = 3.2 W

2.5.1 Thermal Considerations

In a semiconductor device, there exists a relation between the drain source current and transconductance because of the low electric field mobility and high electric field velocity. The relationship is facilitated by the temperature of operation. It is observed that the mobility and electron field velocity decrease with temperature and this effect can be reversed by increasing the values of sheet resistance and parasitic resistance.

The effects of temperature play a major role in semiconductor device constructed using gallium nitride because they operate at high power [21] and gallium nitride possess a quality of self-eating. The amount of self-eating is inversely proportional to the thermal conductivity. And the effects of the temperature have to be minimized in order for the semiconductor device to be operated at high power environment. The only way to reverse the effect of temperature is to incorporate a highly thermally conductive substrate such as AIN or diamond. The thermal properties of gallium nitride are listed below

• Thermal conductivity = 1.95W/cm C
• Thermal expansion = 5.59*10^{-6} °C
• Elastic constant  C_{13} = 103 , C_{33} = 405
• Piezoelectric constants e_{31} = -0.49 C/m^2 , e_{33} = 0.77 c/m^2
• “Hardness = 15.5 GPa”
2.6 Mechanical Properties

Few of the most important mechanical properties of gallium nitride cubic polytopes can be investigated using the molecular-beam epitaxy. The mechanical properties are studied using MEMS and NEMS. This covers a very wide range of applications such as cantilevers and bridge up membranes. In general the mechanical properties are semiconductor materials are defined by the elastic constants [21]. The elastic constants of gallium nitride is listed below

- \( C_{11} = 410.5 \pm 10 \)
- \( C_{12} = 148.5 \pm 10 \)
- \( C_{13} = 98.5 \pm 3.5 \)
- \( C_{33} = 388.5 \pm 10 \)
- \( C_{44} = 124.6 \pm 4.5 \)

2.7 Energy Band Diagram of the MISFET

The MISFETs constructed using the n and p type substrates are briefed in figure 12 & 13
Figure 12: Energy Band Diagram of MISFET n-Substrate

The procedure in constructing the MISFET using the n-substrate is discussed below:

- The positive potential is applied at intersection of the conduction bands and the Ec bend around the Fermi energy level Ef which is defined to be a constant in the semiconductor which ensures that no current flows in the circuit. The bending leads to an collection of the electrons which are the majority carriers at the interface of the two layers.

- The zero input voltage shows that the energy band remain flat and ensures the semiconductor n and p type carriers to be at an thermal equilibrium.

- When a very minimal negative voltage is applied, the electrons which are the majority carriers will be diffracted away from the interface, making the bands bend outwards which makes the intrinsic energy go closer to the Fermi energy.

- On increasing the negative voltage further, the bending of the waves further continues, which ensures the Ei to be Ef, the holes exceed the electrons which are the
majority carriers at the interface. This phenomenon is called as inversion, and at this stage the interface gets inverted.

Figure 13: Energy Band Diagram of MISFET p-Substrate

The figures 12 and 13 depicts the ideal MOS- capacitors under different bias conditions such as accumulation, flat-band, depletion and inversion. The charges in the n type and p type substrates are responsible for the bending of the bands upwards near the interface of the oxide/substrate. For the negative voltages \( V < 0 \), the substrate bends upwards and downwards for \( V > 0 \). The energy levels are computed at zero voltage or flat-band conditions where the \( \phi_{ms} \) denotes the Fermi level potential, the \( \chi_i \) and \( \chi \) represents the electron affinity for the oxide and the substrate, and \( E_g \) is the bandgap of the substrate.

p-semiconductor (nMOS) has \( \phi_{ns} = \phi_m - (\chi + E_g/q - \phi_p) = 0 \), and

n-semiconductor (pMOS) has \( \phi_{ns} = \phi_m - (\chi + \phi_n) = 0 \).

2.8 Defects in Gallium Nitrate

Gallium nitride, InN and AlN have a great significance because of their
applications in high power abilities. Among the three, the GaN have a few deformities when contrasted due with the cross section structures included. Because of these deformities it will influence the electrical and also optical properties of the essential material included [21]. The imperfections include the separated and the few purposeful deserts so they can influence the functionalities of the materials.

2.8.1 Native Point Defects

Deformities will constantly show in the materials as it will impacts the optical properties and electrical properties of the materials. These imperfections are lead to the toughening in the materials. The disengaged local imperfections take the type of opportunities, interstitials, and antisites. Complex imperfections shaped through collaboration of segregated local deformities. Figure 2.13 demonstrates the vitality development at the diverse levels of the arrangement vitality” (eV).

Figure 14: Formation of Energies in Fermi level for Naive defects
2.8.2 Interstitial and Antisites Defects

Accomplishment of blemishes is frequently observed in GaN as a result of the minor cross segment predictable of GaN and the broad size in-between of Ga and N atoms. Then again, under specific conditions a percentage of the defects may shape yet in greatly little core interests. The forcing size of the Ga particles facilitates improvement energies of the Ga interstitial (Gai) and colossal cross segment relaxations. Expansive convey ability of Gai even at room temperature imply that Gai is caught by some distinctive deformations and does not exist in GaN as a restricted negative perspective in balance [22].
Chapter 3 MISFET

3.1 Introduction

MISFET stands for Metal Insulator Semiconductor Field Effect Transistor. MISFETs and MOSFETs are closely related. Structure of MISFET is as shown in the Figure 3.1.

![Figure 15: Structure of GaN MISFET](image)

The illustration of the GaN MISFET is briefed in the Figure. The GaN MISFET is built over a GaN and Silicon substrate. A buffer layer is then developed which is of few micrometer thickness over the substrate region. The buffer layer facilitates the doping and fabrication of MISFET. The buffer layer is undoped. The doped GaN is then added over the undoped buffer layer to construct the active layer. The active layer contributes to the source and the drain region. They are well separated from each other using the oxide layer. The oxide layer acts as an insulator. The gate which is made using the Pd is then developed over the oxide layer.
3.2 MISFET Structure

MISFET’s are nowadays constructed using the new technology popularly known as etch-stop barrier structure. High electron mobility transistors using GaN are constructed using this technology.

The gate terminal is what that differentiates the MOSFET from the MISFET, therefore gate recess becomes a very important process in construction of a high mobility transistor (HEMTs). The gate recess is technically used to reduce the short-channel effects and improve the gain cutoff frequency. The GaN is a very inert to wet chemical etching, therefore chlorine based chemical etching is used. This dry plasma etching technique however has two major drawbacks which are is causes defects in the crystal lattice structure and degrades the channel mobility in the recessed region. Secondly it is impossible to have precise control on the amount of etching required; therefore it might contribute to change in transconductance and the threshold potential.

The Figure below shows the relationship between the depth of each region of the constructed MISFET and their corresponding energy band values given in eV. The Figure also shows the way on which the MISFET is constructed. It is fabricated by developing a 2.8 micrometer thickness buffer region over the silicon wafer. The buffer region is etched using plasma etching technology and then the GaN material is applied over it for a depth of 1.2 micrometer. The applied GaN has bandgap energy of about -3 eV. The source and drain terminals are developed over the GaN layer. The source and drain is well insulated by developing a layer of AlGaN and AlN each of thickness 3 nanometer and 1.5nanometer respectively. One more layer of GaN is incorporated to develop the gate.
The n type GaN to construct the gate is around 22 nanometer. The Gate terminal is developed over the n-GaN.

Figure 16: Developing of MISFET

MISFET is formed by highly doped n channel region on p-type substrate. The drain and the source of the MISFET is formed in two sides of n-channel. The low doped p region is formed between the n region acts as the insulation layer and hence serves the purpose of gate terminal. The two highly doped n regions becomes the source and drain.

A MISFET which uses gallium nitrite as the insulated gate material is commercially used because of its low cost, high output power and ability to operate in high temperature. It can also provide hot carrier endurance and punch-through endurance. In n and p type layers p and n type dopants are added respectively. The addition of additional impurity makes the gallium nitride structure which is in crystal plane
orientation. The addition of impurities also boosts impurity diffusion layer and breakdown voltage. The breakdown voltage is three times greater than MISFETs which has silicon as gate. Utilization of insulated materials such as Gallium Nitride provides high speed switching in the transistor in comparison to the bipolar or traditional transistors.

When the gallium nitride substrate is introduced to the gate terminal, the interface between the oxide layer and the gallium nitride has the channel mobility which is lower than those additional transistors. In archaic transistors care has to be taken to restrict the electrons flowing out of the source to the channel. However in MISFETs the channel region are well covered or separated by a higher energy gap and restricts the current flowing between the source and the drain. MISFETs have crystal plane orientation.

The MIIIFET is finally developed by diffusing several gasses which includes nitrogen, phosphorous and arsenic. The gate incorporates a silicide layer of refractory metal which consists of components such as tungsten, molybdenum or titanium.

3.3 Material Growth

3.3.1 Metal organic Chemical Vapor Deposition (MOCVD)

In the previous couple of years, metal organic chemical vapor statement (MOCVD) has developed into a main method for generation of III-V nitride semiconductor optoelectronic and electronic gadgets [23]. For business GaN gadget applications MOCVD has developed as the main hopeful in view of the accomplishment of super-splendid blue LEDs and the extensive scale-fabricating capability of the MOCVD procedure [23]. The dominant part of all GaN based p-n intersection light
discharging diodes (LEDs) commonly utilize polluting influence related move for blue and green outflow [24]. As of late, direct bandgap discharge in the blue-green ghastly district has been gotten utilizing high as a part of substance in single quantum well (SQW) LEDs and lasers utilizing the two-stream MOCVD system [28]. Full-shading LED showcases can now be made altogether with the MOCVD procedure when consolidating the blue and green GaN LEDs with the high brilliance yellow and orange discharging LEDs which were shown in the AlGaInP materials framework in the mid 1990's [28]. Understanding the development of AlInGaN/GaN based materials by metalorganic compound vapor affidavit (MOCVD) is along these lines of compelling significance in enhancing the properties of electronic components [29].

3.3.2 MOCVD Reaction Chemistry

The common MOCVD reaction defining the GaN deposition process can be explained by the following reaction[30]:

\[
\text{Ga} (\text{CH}_3)_3 (v) + \text{NH}_3 (v) \rightarrow \text{GaN} (s) + 3\text{CH}_4 (v)
\]

“Where (v) =vapor and (s) = solid”

This balanced explanation neglects that the specific reaction way and responsive species are expansively obscure. The parts of the reaction are not remarkable and the transitional reactions are thought to be perplexing. A more probable response pathway prompting development of the GaAs epitaxial layers includes the homogeneous disintegration of TMG as reported in a before study on GaAs epitaxy [31].

\[
\text{Ga(CH}_3)3(v) \rightarrow \text{Ga(CH}_3)2(v) + \text{CH}_3(v) \text{Ga(CH}_3)2(v) \rightarrow \text{GaCH}_3(v)
\]
$+ \text{CH}_3(\nu) \text{Ga(CH}_3(\nu) \rightarrow \text{Ga(\nu)} + \text{CH}_3(\nu)$

The Group-V hydride root is used to disintegrate heterogeneously on the GaN surface or the reactor dividers to produce nuclear nitrogen holding radical at Heightened development temperature. Reflection of the first hydrogen security is thought to be the rate confining step in the deterioration of ammonia.

“$\text{NH}_3(s/v) \rightarrow \text{NH(3-x)(s/v)} + x \ Hz(s/v)$”

“$\text{GaCH}_3(s/v) + \text{NH(s/v)} \rightarrow \text{GaN(s)} + \frac{1}{2} \text{H}_2$”

Then again, the level of appreciating of the advancement methodology is insufficient at the most. The most complex point, and decidedly the smallest propelled, is the zone of the vitality of the strategy and advancement components happening at the strong/vapor interface all through MOCVD improvement. Pyrolysis and dispersal of the get together III beginning through the utmost layer is the key pathway managing the improvement rate. Regardless, parasitic side reactions for instance enduring adduct organizing in the middle of TMAI and alkali unpredictable will decrease the advancement rate by confining the flux of get-together III roots to the creating interface.

Streamlining of MOCVD improvement is ordinarily done by observational examinations of outside parameters for instance advancement temperature, V/III degree, substrate tilt and mass stream rates. These studies have perceived a few zones of advancement: mass transport limited, desorption and surface effectively obliged administrations. Expected GaN MOCVD is ordinarily performed in the mass transport
limited administration that happens over a wide temperatures (600°C–1100°C). In this
temperature range improvement is bound by mass transport of the fragment III reactant to
the creating interface. Coming about because of the way that the spread procedure is a
subject to temperature, there exists a slight grow in the advancements.

A refined philosophy to a basically detachment boundless GaN substrate for
instruments may be used by two progressive LEO ventures with the front of the second
step situated over the opening depicted by the front of the first step, therefore closing the
defects that grew out of the first windows. This caught system offers the believability of
killing the weights of heteroepitaxy, and can be noteworthy until GaN substrates come to
be prepared.

![Cross-section TEM of typical MOCBD grown GaN using an AlN buffer layer on SiC (left) and typical LEO GaN (right).](image)

Figure 17: Cross-section TEM of typical MOCBD grown GaN using an AlN buffer layer on SiC (left) and typical LEO GaN (right).

Hall portability, an alternate goal for GaN used as a piece of contraption
demands is to obtain most astonishing Hall motilities possible. Figure3.3. thinks about
the deliberate electron versatility in n-sort GaN, in addition to the impacts got from
Monte Carlo comparison. As may be seen, the exploratory data is brutally a substantial
piece of the processed regard, likely on account of vital scattering from degradations and
deserts in the State-of-the-craftsmanship materials.
Figure 18: Electron Concentration vs Electron Mobility

The “III-V nitrides are needed to be made p-sort by substituting Column II segments for case Zn, Mg Be and Ca on for Ga” regions to structure “single acceptors”. On the other hand, the majority of the previously stated divalent parts shape significant acceptors; Magnesium (Mg) is the shallowest with ionization level of 0.17eV which is still incalculable kTs over the valence gathering edge of GaN. At this acceptor level, one should simply require <10% of the Mg atoms to be ionized at room temperature, which implies the Mg obsession ought to be more or less two-solicitations of size more great than the desired opening obsession. At the point that MOCVD is used as the improvement system, it has been requesting to get p-sort conductivity. It was later perceived that hydrogen has earnest impact in passivating the Mg acceptors, and makes a fair-minded complex Mg-H that maintains a strategic distance from the organizing of openings in GaN. It was initially shown by Amano et al. that p-
sort conductivity could be acknowledged by starting Mg-doped GaN using level-life electron light. Nakamura [35] showed in this way that the actuation of Mg can likewise be acknowledged by warm strengthening at ~7000 C. Note that MBE developed GaN doped with Mg may be p-sort without a warm initiation process, due to the nonappearance of hydrogen and H-N radicals amid development. Also, p-sort doping was likewise attained to by insert of Ca or Mg into GaN, took after by high temperature tempering (~11000 C). The most astounding opening fixation reported so far is ~, and the regular gap portability is low, regularly 10 cm2 /Vs or beneath, yet permitting the acknowledgment of p-n intersections. Attaining to low resistance Ohmic contacts to the GaN layers with poor p-sort doping fixations has turned out to be troublesome.[36] Recently, Brandt et al found that by repaying Be with O, a nonpartisan dipole is framed that does not diffuse the openings. Henceforth a record high gap portability of 150 cm2/Vs was acquired. This may be the perfect contact layer for GaN based gadgets obliging a p-sort ohmic contact [37].

GaN-based enhancers and switches are charming for uplifted force demands in antagonistic domains. Dependable edge end and passivation strategies are separating to altogether attempt the previously stated sorts of devices. There is very little work to date here. Additionally, as said something regarding past, thermally stable doping, separation, and metal contacts are every single key issue for these uncommon orders.
3.4 Defects in Gallium Nitride MISFET

In the Gallium Nitride semiconductor device the p-type gate region has n-type impurity region as well as the n-type concentration region which is buried under the channel region. The gate insulation layer between the “source and drain regions” must be insulated enough to distinguish the n-type semiconductor used for source and drain and the n-type impurity present in the gate terminal.

The gate electrode of the semiconductor device is manufactured using gallium nitride at its poly crystalline form with either boron or aluminum as the dopant. The doping concentration should fall within the range $1.01 \times 10^{16} \text{ cm}^{-3}$ to $1.01 \times 10^{21} \text{ cm}^{-3}$.

The channel regions are well insulated while diffusion of nitrogen, phosphorous or arsenic. The concentration of these species should be kept between $5 \times 10^{15} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$. The source and the drain have p-type dopant which has been diffused right below the insulated gate. The amount of this p-type dopant should lie between $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$.

The crystalline gallium nitride has a surface which is either hexagonal or tetrahedral. And is given by the Wurtzite model and Zincblende model is used to construct the insulator gate terminal. The fabrication should not alter the crystalline structure of the material. The MISFET should have the lateral RESURF or lateral DMOS.
Chapter 4 Numerical Analysis

4.1 I-V Characteristics Discussion

The construction of the channel of a semiconductor device such as MISFET is a random process and can be described by two-dimension Poisson equation [40]

\[
\frac{\partial^2 \Phi(x,y)}{\partial x^2} + \frac{\partial^2 \Phi(x,y)}{\partial y^2} = -\frac{q N_d^+}{\varepsilon}
\] (4.1.1)

The above expression for \( \Phi(x,y) \) is labeled as electrostatic potential in the link, \( N_d^+ \) is the doping concentration due to the ionization in the channel, electronic charge in the channel is given by \( q \) and the permittivity is given by \( \varepsilon \).

The “boundary conditions” of semiconductor channel are [41]

\[
\Phi(0,y) = \Phi_{ss} = \Phi_{n^+} + I \quad (4.1.2)
\]

\[
\Phi(0,y) = \Phi_{ss} + V_{DS} \quad (4.1.3)
\]

\[
\Phi(0,y) = U(0) = \Phi_{s0} \quad (4.1.4)
\]

Where \( \Phi_{ss} \) = surface state potential at the interface of insulator and GaN

The Electric Field Boundary condition

\[
\frac{\partial \Phi(x,a)}{\partial y} + \frac{\partial U(y)}{\partial y} = 0 \quad (4.1.5)
\]

where

\( \Phi_{n^+} = \) the built-in voltage across the gate/drain-to-substrate

\( U(y) = 1\text{-D solution for the Poisson equation} \)

\( V_{DS} = \) Voltage between drain and source
Φ_{s0} = potential at gate-channel surface

L = channel length.

a = depth of device channel

The voltage Φ(x,y) in equation above is stated as a conjunction of two functions, U(x,y) and Ψ(x,y)

Φ(x,y) = U(x,y) = Ψ(x,y)  \hspace{1cm} (4.1.6)

Where Φ(x,y) and Ψ(x,y) satisfies

\[ \frac{\partial^2 \Psi(x,y)}{\partial x^2} + \frac{\partial^2 \Psi(x,y)}{\partial y^2} = 0 \]  \hspace{1cm} (4.1.7)

\[ \frac{\partial^2 U(x,y)}{\partial x^2} + \frac{\partial^2 U(x,y)}{\partial y^2} = -(q N_d^+ / \varepsilon) \]  \hspace{1cm} (4.1.8)

Drain current is evaluated using the depth of the depletion region and the carrier velocity of the channel designated by the above Poisson equations. Let ‘h1’ and ‘h2’ give the values of the depletion depth and let the carrier transportation area be defined as ‘A’

\[ s = \frac{h1}{A} = \frac{-\sqrt{Vi} + \sqrt{Vi - \beta (Ko + Vgs)}}{\beta \sqrt{Vp}} \]  \hspace{1cm} (4.1.9)

\[ p = \frac{h2}{A} = \frac{-\sqrt{Vi} + \sqrt{Vi - \beta (Ko + Vgs - Vds)}}{\beta \sqrt{Vp}} \]  \hspace{1cm} (4.1.10)
The 2-d Poisson equation is integrated from s to p on y-axis and from zero to length of the channel to evaluate the drain current.

\[
I_{ds} = \frac{IA}{\beta \sqrt{Vp}} \left( (\beta \sqrt{Vp}) + \sqrt{Vi} \right) Vds \frac{2}{3 \beta} (Vi - 3\beta \sqrt{Vp}) Vps \frac{2}{3} VAB \frac{Lg + \frac{Vds}{Ec}}{Lg + \frac{Vds}{Ec}}
\]

(4.1.11)

Where \( Vi, \beta \) and \( Ko \) defines the surface voltage parameters and \( \beta \) is relational to surface state density (Nss) and it is inversely proportional to the permittivity of the insulator (\( \epsilon_d \)). \( Vi \) is a function of Donor concentration, permittivity and it is inversely proportional to insulator permittivity. And \( Ko \) relies upon \( \beta \) and \( Vi \) and are given by

\[
\beta = 1 + \left( \frac{q \ast t \ast Nss}{\epsilon_d} \right)
\]

(4.1.12)

\[
Vi = \left( \frac{q \ast \epsilon \ast Nd \ast t \ast t}{2 \ast \epsilon \ast d} \right)
\]

(4.1.13)

\[
Ko = (\beta \ast \psi_{so}) - (2 \ast \sqrt{Vi \ast \psi_{so}})
\]

(4.1.14)

The current in the carrier-transport area is given by ‘IA’ and it is proportional to the area of the carrier-transport region, carrier velocity, carrier concentration, electron
charge and the saturation voltage. ‘VA’ is the voltage in the active layer. And it depends on ‘Vgs’ and ‘Vds’.

\[ I_A = q \times N_d \times Z \times A \times \left\{ \mu + \left( \frac{V_{sat}}{E_C} \right) \right\} \]  

(4.1.15)

\[ V_{ps} = \sqrt{V_i - (\beta \times VA)} - \sqrt{V_i - (\beta \times VB)} \]  

(4.1.16)

\[ V_{AB} = VA\sqrt{V_i - (\beta \times VA)} - VB\sqrt{V_i - (\beta \times VB)} \]  

(4.1.17)

\[ VA = K_0 + V_{gs} - V_{ds} \]  

(4.1.18)

\[ VB = K_0 + V_{gs} \]  

(4.1.19)

The Alteration in the energy in the conduction band and the Fermi level energy is a function of Boltzmann’s constant and electron charge. The dissimilarity amid the energy of conduction band and the intermediate energy dangles on the energy gap between levels. The Fermi potential ‘\( \psi_{fp} \)’ is given by

\[ \psi_{fp} = \left( \frac{E_g}{2} \right) - \left( \frac{kT}{q} \right) \times \log\left( \frac{N_c}{N_d} \right) \]  

(4.1.20)

The surface potential \( \psi_{so} \) is twice of the Fermi potential \( \psi_{fp} \) under strong inversion. The surface potential \( \psi_{so} \) can be expressed as
\[ \psi_{so} = 2 \times \psi_{fp} \quad (4.1.21) \]

The Transconductance is the negative slope of “Drain source” current and “Gate source Voltage” evaluated for a given \( V_{ds} \). On simplification transconductance become a function of source current and pinch off voltage. And is given by

\[ g_m = \left( \frac{I_s}{V_p} \right) \times f_{g} \quad (4.1.22) \]

Where the influence of the insulator is given by ‘\( f_{g} \)’

\[ f_{g} = \frac{A \times \varepsilon d}{2 \left[ \left( \varepsilon + (q \times N_{ss} \times p \times A) \right) \times t \right] + (p \times A \times \varepsilon d)} \quad (4.1.23) \]

The total gate terminal capacitance is proportional to gate source capacitance, insulator capacitance and the surface capacitance.

\[ C_{gs}' = \frac{(C_{gs} + C_{ss}) \times C_{ox}}{C_{gs} + C_{ss} + C_{ox}} \quad (4.1.24) \]

The gate source capacitance that is strongly related to the surface permittivity, length of the channel and the gate width and so the modified gate source capacitance can be expressed by

\[ C_{gs} = \frac{2 \times \varepsilon \times Z \times L_g \times f_{g}}{A} + C_f \quad (4.1.25) \]

The \( C_{gs} \) also depends upon fringe effect capacitance (\( C_f \)) is evaluated by

\[ C_f = \frac{\varepsilon \times Z \times L_g}{g} \quad (4.1.26) \]
The consequence of surface states can be represented by an comparable capacitance ‘C_{ss}’ and is given by the equation

\[ C_{ss} = q \times N_{ss} \times Z \times L_g \]  

(4.1.27)

The oxide in the MISFET performances like a capacitor and the capacitance provided can be mathematically written as

\[ C_{ox} = \frac{\varepsilon d \times L_g \times Z}{t} \]  

(4.1.28)

The cut off frequency is a function of amplifier current gain, sensitivity of the insulator and gate terminal capacitance. and is given by

\[ f_t = \frac{g_m}{(2 \pi C_{gs}')} \]  

(4.1.29)

The intrinsic carrier concentration (n_i) is exponentially dependent with the electron charge, energy gap and Boltzmann’s constant and is proportional to N_c and N_v and given by

\[ n_i = \sqrt{N_c \times N_v} \times \exp \left( \frac{-E_g \times q}{2 \times K \times T} \right) \]  

(4.1.30)

The ‘N_c’ and ‘N_v’ can be computed using

\[ N_c = 3.25 \times 10^{15} \times \sqrt{T \times T \times T} \]  

(4.1.31)

\[ N_v = 4.8 \times 10^{15} \times \sqrt{T \times T \times T} \]  

(4.1.32)
The pinch off voltage is computed mathematically using the equation below and is a function of the permittivity, the electron charge and the donor concentration

\[ Vp = \left( \frac{qNd*A*A}{2*\varepsilon} \right) \]  \hspace{1cm} (4.1.33)

The Built-in potential depends on the Boltzmann’s constant and it is logarithmically proportional to the donor concentration, acceptor concentration and intrinsic carrier concentration

\[ Vbi = \left( \frac{K*T}{q} \right) * \log \left( \frac{Na*Nd}{Ni*Ni} \right) \]  \hspace{1cm} (4.1.34)

The threshold voltage is given by the difference between built-in potential and the pinch off potential

\[ Vt = Vbi - Vp \]  \hspace{1cm} (4.1.35)

Saturation voltage is the minimum potential required to drive the MISFET to saturation and it depends on the electric field where the voltage is maximum

\[ Vsat = U * Ec \]  \hspace{1cm} (4.1.36)

Fully open channel saturation current is considered when the MISFET is at saturation region with saturation voltage ‘Vsat’. The saturation voltage also depends on the donor concentration, and can written as

\[ Is = q * Nd * Z * A * Vsat \]  \hspace{1cm} (4.1.37)
Chapter 5 Results and Discussions

An analytical model of GaN MISFET has been developed to study the DC parameters. The I-V characteristics, transconductance and gate capacitance have calculated to find the frequency response. This analytical model has been computed by using MatLab and the results have been displayed categorically.

5.1 Simulation 1: Drain Current Vs Drain Voltage Characteristics

![Drain Current Vs Drain Voltage Characteristics](image)

Figure 19: Drain Source Current versus Drain source Voltage Characteristics
The Figure 19 shows a “plot of drain-source current (Ids)” versus “drain-source voltage (Vds)” for different “gate-source voltages (Vgs) of 0V, -6V, -12V and -18V” with “channel doping (Nd) of 1x10^{17} cm^{-3}, acceptor doping (Na) of 1x10^{15} cm^{-3}, surface state density (Nss) of 5x10^{11}, channel length (Lg) of 4x10^{-4} cm, gate width (Z) of 260x10^{-4} cm, active layer (A) of 0.8x10^{-4}cm. The simulated I-V characteristics show clearly linear region, non linear regions and saturation regions. The drain-source current shows good resemblance of usual MISFET device. The nature of drain-source current and gate-source voltage Vgs authorizes that device acting as depletion device. This plot has been generated by using the equation (4.1.11).
5.2 Simulation 2: Transconductance Vs Gate to Source Voltage

![Figure 20: Transconductance versus Gate to Source Voltage](image)

The Figure 20 presents a plot of transconductance (gm) versus gate-source voltage (Vgs) for different drain-source voltage Vds at 40V, 60V, and 90V with persistent mobility (U) of 700 cm²/V⋅sec, thickness of oxide (tox) of 40x10⁻⁸ cm, gate width (Z) of 500x10⁻⁴ cm, gate length (Lg) of 4x10⁻⁴ cm, active layer (A) of 0.8x10⁻⁴ cm, acceptor doping concentration (Na) of 1x10¹⁵ cm⁻³, donor concentration (Nd) 1x10¹⁷ cm⁻³, surface...
state density (Nss) of \(1\times10^{10}\). The Transconductance (gm) plot has been estimated in saturation region to know the behavior of transconductance in non-linear region to evaluate the maximum frequency response. The transconductance exponentially increases for gate-source voltage (Vgs) transition range of -20 to +20V and also confirm the device behaving as depletion mode. This graph is been computed using the equation (4.1.22)
5.3 Simulation 3: Gate Source Capacitance Vs Insulator Thickness

Figure 21: Gate Source Capacitance versus Insulator Thickness

The Figure 21 displays a plot of gate-source capacitance versus insulator thickness for the different surface state density (Nss) of $5 \times 10^{12}$, $1 \times 10^{12}$ with mobility (U) of 700 cm$^2$/V.sec, gate width (Z) of $500 \times 10^{-4}$cm, gate length (Lg) of $4 \times 10^{-4}$ cm, active layer thickness (A) of $0.8 \times 10^{-0}$ cm, acceptor doping concentration (Na) of $1 \times 10^{15}$ cm$^{-3}$ and donor concentration (Nd) $1 \times 10^{17}$ cm$^{-3}$. The gate-source capacitance $C_{gs}$
exponentially decreases with insulator thickness because of gate-insulator change. In order to increase the cut-off frequency, the insulator thickness plays an important role by affecting the gate capacitance. This plot has been drawn by the equation (4.1.24)

5.4 Simulation 4: Cut Off Frequency Vs Channel Length – Vgs Differs

![Figure 22: Cut Off Frequency Vs Channel Length – Vgs Differs](image)

The Figure 22 presents a group of cut-off frequency versus channel length for different gate source voltage Vgs = 0V, -6V and -12V with constant Vds = 30V, mobility...
(U) of 700 cm²/V·sec, thickness of oxide (tox) of 40x10⁻⁸ cm, gate width (Z) of 260x10⁻⁴ cm, gate length (Lg) of 4x10⁻⁴ cm, active layer thickness (A) of 0.8x10⁻⁴ cm, acceptor doping concentration (Na) of 1x10¹⁵ cm⁻³, donor concentration (Nd) 1x10¹⁷ cm⁻³, surface state density (Nss) of 5x10¹¹. The cut off frequency in the range of 9Ghz is acquired for a small channel MISFET. The cut-off frequency exponentially reduces as the channel length drops. In order to acquire any range of high cut-off frequency, the physical gate length plays a vital role. The plot has been framed by using the equation (4.1.29)
5.5 Simulation 5: Cut Off Frequency Vs Channel Length - tox Differs

![Figure 23: Cut Off Frequency Vs Channel Length - tox Differs](image)

The Figure 23 shows a plot of cut off frequency $f_t$ versus gate length $L_g$ for difficult insulator thickness of $40 \times 10^{-7}$ cm, $60 \times 10^{-7}$ cm and $80 \times 10^{-7}$ cm with mobility ($U$) of $700 \text{ cm}^2 / \text{V.sec}$, thickness of oxide ($tox$) of $40 \times 10^{-8}$ cm, gate width ($Z$) of $260 \times 10^{-4}$ cm, gate length ($L_g$) of $4 \times 10^{-4}$ cm, active layer thickness ($A$) of $0.8 \times 10^{-4}$ cm, acceptor doping concentration ($Na$) of $1 \times 10^{15}$ cm$^{-3}$, donor concentration ($Nd$) $1 \times 10^{17}$ cm$^{-3}$, surface
state density (Nss) of 5x10^{11}\text{cm}^{-3}. The maximum cut-off frequency of 16Ghz for insulator thickness of 80x10^{-7}\text{cm} is obtained for the gate oxide thickness 80x10^{-7}\text{cm}. The cut-off frequency for this plot has been computed by using equation (4.1.29)

5.6 Simulation 6: Cut Off Frequency Vs Insulator Thickness

![Figure 1: Cut Off Frequency versus Insulator Thickness](image)

Figure 24: Cut Off Frequency versus Insulator Thickness
The Figure 24 demonstrates the cut-off frequency $f_{t}$ versus insulator thickness for various surface state change density $N_{ss}$ of $5 \times 10^{11} \text{cm}^{-3}$ and $1 \times 10^{12} \text{cm}^{-3}$ with constant drain source voltage $100 \text{V}$ and $V_{gs}=0$, mobility $(\mu)$ of $700 \text{cm}^{2}/\text{Vsec}$, thickness of oxide $(t_{ox})$ of $40 \times 10^{-8} \text{cm}$, gate width $(Z)$ of $260 \times 10^{-4} \text{cm}$, gate length $(L_g)$ of $4 \times 10^{-4} \text{cm}$, active layer thickness $(A)$ of $0.8 \times 10^{-4} \text{cm}$, acceptor doping concentration $(N_a)$ of $1 \times 10^{15} \text{cm}^{-3}$ and donor concentration $(N_d)$ $1 \times 10^{17} \text{cm}^{-3}$. The surface state charge density affects and results in significant change in transconductance and gate capacitance. Hence the effects of surface state density on intrinsic parameter are having direct influence over cut off frequency, hence it is vibrant from the plot that the cut off frequency $f_{t}$ shows large value for low $N_{ss}$ and linearly increase with insulator thickness. This plot has been generated by using the equation (4.1.29).
Chapter 6 Conclusion

The “Physics based one-dimensional analytical model for GaN MISFET” has been established to compute the “transconductance, drain-source current and gate-source capacitance”. The fundamental reason for evaluating the transconductance and gate-source capacitance is to compute the frequency response of the device. The I-V characteristics of the MISFITs were calculated for both linear and non-linear regions. The non-linear region of the I-V characteristics gave an insight of the early effect to expect high breakdown voltage. The transconductance and gate-source capacitance has been calculated in the saturation current region to accurately study the frequency response of the MISFET. Another reason to compute the frequency response is that it helps to determine and study the effect of physical dimensions such as the gate length and insulator thickness. It is also used to evaluate the gate biasing for the frequency response. The cut-off frequency response of the evaluated MISFETs were found to be dependent over the gate length and the maximum cut-off frequency response was found to be around 16GHz for gate length which in terms of nanometers. The evaluated device characteristics using the developed analytical model which comprises of the frequency response and other electrical parameters such as I-V characteristics and intrinsic parameter was found to be similar to all parameters computed on the other MISFET devices. The GaN MISFET finds wide range of applications in analog and digital domains due to its ability to work at high speed and ability to operate at high frequency and has emerged as a competitor for the silicon based CMOS.
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APENDIX A

Notations and Symbols Used:

\( U \) = Low field Drift Mobility

\( q \) = Electron Charge

\( Z \) = Gate Width

\( L_{g} \) = Gate Length

\( A \) = Active Layer

\( K \) = Boltzmann’s Constant

\( T \) = Thermal Equilibrium

\( N_{a} \) = Acceptor Concentration

\( N_{d} \) = Donor Concentration

\( E_{o} \) = Permittivity of Semiconductor

\( E_{c} \) = Electric Field Peak at Carrier Peak

\( V_{\text{sat}} \) = Saturation Current Voltage

\( P_{\text{Si0}} \) = Surface Potential at Zero Bias

\( P_{\text{Si}} \) = Surface Potential

\( t \) = Insulator Thickness

\( N_{ss} \) = Surface State Density
Ed = Permittivity of Insulator

B,Vi,K0 = Simplifying Parameters for the Surface Potential

Vgs = Gate to Source Voltage

Vds = Drain to Source Voltage

Vp = Pinchoff Voltage

Vt = Threshold Voltage

gm = Transconductance

Cgs = Gate to Source Capacitance

ft = Cut Off Frequency

Cgs’ = Terminal Capacitance

Cox = Insulating layer Capacitance

Css = Surface State Capacitance

IA = simplifying parameters for Ids

Is = open channel saturation current

Ids = channel or drain current

Rs = Parasitic Resistance at source

Rd = Parasitic Resistance at drain

psi = Channel Conductivity
APENDIX B
MATLAB CODE

Code 1: Drain Current Vs Drain Voltage Characteristics

clc;
clear all;
close all;
array= 100;
Vdslen=120;
q = 1.6*(10^-19);
U =700;
Z= 260*(10^-4); % Gate Width
Lg = 4*(10^-4); % Gate Length
A = 0.8*(10^-4); % Active Layer
K=1.3807e-23;
T=300;
Na = 1*(10^15);
Nd = 1*(10^17); % Donor Concentration
Eo= 8.9; %permittivity of semiconductor
E= Eo*8.854e-14;
Eg= 3.2;
Ec=5000; %electric field peak at carrier peak velocity
Vsat=U*Ec; %saturation carrier voltage
Nc = 3.25e15*sqrt(T*T*T);
PSIfp=(Eg/2)-(((K*T)/q)*log10(Nc/Nd));
PSIs0=2*PSIfp; %surface potential at 0 bias
\text{t}=40\times10^{-8}; \quad \%\text{insulator thickness nm}

\text{Nss}=1\times10^{12}; \quad \%\text{surface state density}

\text{Ed}=3.9\times8.5\times10^{-14}; \quad \%\text{permittivity of insulator}

\text{B}=1+\left(\frac{q\times t \times Nss}{Ed}\right);

\%\text{simplifying parameter for the surface potential}

\text{Vi}=\frac{(q\times E \times N_e \times t \times t)}{(2 \times Ed \times Ed)};

\%\text{simplifying parameter for the surface potential}

\text{K0}=(B \times \text{PSIs0})-(2 \times \sqrt{\text{Vi} \times \text{PSIs0}});

\%\text{simplifying parameter for the surface potential}

\text{Vp} = \frac{(q \times N_d \times A \times A)}{(2 \times E)}

\%\text{******************************}

\text{Vgs} = 0;

\text{Vds} = [0:0.5:Vdslen];

\text{for} \ i=1:\text{length} (\text{Vds})

\quad \text{for} \ k = 1:array

\quad \text{Va}=K0+Vgs-Vds(i);

\quad \text{Vb}=K0+Vgs;

\quad \text{Ia}=(q \times N_d \times Z \times A) \times \left(\frac{U+(V_{sat}/E_{c})}{E}\right);

\quad \text{Vps}=\sqrt{\text{Vi}-(B \times \text{Va})}-\sqrt{\text{Vi}-(B \times \text{Vb})};

\quad \text{Vab}=(\text{Va} \times \sqrt{\text{Vi}-(B \times \text{Va})})-(\text{Vb} \times \sqrt{\text{Vi}-(B \times \text{Vb})});

\quad \text{Id1}=((B \times \sqrt{\text{Vp}})+\sqrt{\text{Vi}}) \times \text{Vds}(i);

\quad \text{Id2}=(2/(3 \times B)) \times (\text{Vi}-(3 \times B \times \sqrt{\text{Vi} \times \text{Vp}})) \times \text{Vps};

\quad \text{Id3}=(2/3) \times \text{Vab};

\quad \text{Id4}=Lg+(\text{Vds}(i)/E_{c});

\quad \text{Id5}=(\text{Id1}-\text{Id2}-\text{Id3})/\text{Id4};

\quad \text{Ids}(k) = \left(\frac{\text{Ia}}{(B \times \sqrt{\text{Vp}})}\right) \times \text{Id5};

\text{end}

\text{ilinear}(i) = \text{Ids}(k);

\text{ilinear}(i)=\text{real}(\text{ilinear}(i));

\text{61}
end
plot(Vds,ilinear,'b')
ylabel( 'Drain-Current, Ids (mA)' )
xlabel( 'Drain-Bias voltage, Vds (V)' )
title( 'Id-Vd characteristics ' )
hold on;
%*****************************************************************************
Vgs = -6;
Vds = [0:0.5:Vdslen];
for i=1:length(Vds)
    for k = 1:length(Va)
        Va=K0+Vgs-Vds(i);
        Vb=K0+Vgs;
        Ia=(q*Nd*Z*A)*(U+(Vsat/Ec));
        Vps=sqrt(Vi-(B*Va))-sqrt(Vi-(B*Vb));
        Vab=(Va*sqrt(Vi-(B*Va)))-(Vb*sqrt(Vi-(B*Vb)));
        Id1=((B*sqrt(Vp))+sqrt(Vi))*Vds(i);
        Id2=(2/(3*B))*(Vi-(3*B*sqrt(Vi*Vp)))*Vps;
        Id3=(2/3)*Vab;
        Id4=Lg+(Vds(i)/Ec);
        Id5=(Id1-Id2-Id3)/Id4;
        Ids(k) = (Ia/(B*sqrt(Vp)))*Id5;
    end
    ilinear(i) = Ids(k);
    ilinear(i)=real(ilinear(i));
end
plot(Vds,ilinear,'g')
ylabel( 'Drain-Current, Ids (mA)' )
xlabel( 'Drain-Bias voltage, Vds (V)' )
title( 'Id-Vd characteristics ' )
hold on;
%
Vgs = -12;
Vds = [0:0.5:Vdslen];
for i=1:length(Vds)
    for k = 1:array
        Va=K0+Vgs-Vds(i);
        Vb=K0+Vgs;
        Ia=(q*Nd*Z*A)*(U+(Vsat/Ec));
        Vps=sqrt(Vi-(B*Va))-
        sqrt(Vi-(B*Vb));
        Vab=(Va*sqrt(Vi-(B*Va)))-(Vb*sqrt(Vi-(B*Vb)));
        Id1=((B*sqrt(Vp))+sqrt(Vi))*Vds(i);
        Id2=(2/(3*B))*((Vi-(3*B*sqrt(Vi*Vp)))*Vps;
        Id3=(2/3)*Vab;
        Id4=Log(Vds(i)/Ec);
        Ids(k) = (Ia/(B*sqrt(Vp)))*Id5;
        end
        iinear(i) = Ids(k);
        iinear(i)=real(iinear(i));
        end
        plot(Vds,iinear,'r')
        ylabel('Drain-Current, Ids (mA)')
        xlabel('Drain-Bias voltage, Vds (V)')
        title('Id-Vd characteristics ')
        hold on;
%
Vgs = -18;
Vds = [0:0.5:Vdslen];
for i=1:length(Vds)
for k = 1:array
Va=K0+Vgs-Vds(i);
Vb=K0+Vgs;
Ia=(q*Nd*Z*A)*(U+(Vsat/Ec));
Vps=sqrt(Vi-(B*Va))-sqrt(Vi-(B*Vb));
Vab=(Va*sqrt(Vi-(B*Va)))-(Vb*sqrt(Vi-(B*Vb)));
Id1=((B*sqrt(Vp))+sqrt(Vi))*Vds(i);
Id2=(2/(3*B))*(Vi-(3*B*sqrt(Vi*Vp)))*Vps;
Id3=(2/3)*Vab;
Id4=Lg+(Vds(i)/Ec);
Id5=(Id1-Id2-Id3)/Id4;
Ids(k) = (Ia/(B*sqrt(Vp)))*Id5;
end
ilinear(i) = Ids(k);
ilinear(i)=real(ilinear(i));
end
plot(Vds,ilinear,'k')
ylabel('Drain-Current, Ids (mA)')
xlabel('Drain-Bias voltage, Vds (V)')
title('Id-Vd characteristics ')
hold on;
text(87.5,0.350,'tox = 40e-08')
text(87.5,0.330,'Vgs = 0')
text(87.5,0.310,'Z = 260e-04')
text(87.5,0.290,'Lg = 4e-04')
text(87.5,0.270,'A = 0.8e-04')
text(87.5,0.250,'Na = 1e15')
text(87.5,0.230,'Nd = 1e17')
text(87.5,0.210,'Nss = 5e11')
legend('Vgs = 0','Vgs = -6','Vgs = -12','Vgs = -18')
Code 2: Transconductance Vs Gate to Source Voltage

clc;
clear all;
close all;
q = 1.6e-19; % e- Charge
U = 700; % Low field Drift Mobility
Z = 500e-04; % Gate Width
Lg = 4e-04; % Gate Length
A = 0.8e-04; % Active Layer
K = 1.3807e-23;
T = 300;
Na = 1e15;
Nd = 0.1e17; % Donor Concentration
E0 = 8.9; %permittivity of semiconductor
E = E0*8.854e-14;
Ec = 5000; %electric field peak at carrier peak velocity
Vsat = U*Ec; %sauraion carrier voltage
Eg = 3.23;
Nc = 3.25e15*sqrt(T*T*T);
Nv = 4.8e15*sqrt(T*T*T);
PSIs0 = -0.67; %surface potential at 0 bias
t = 40e-08; %insulator thickness nm
Ni = sqrt(Nc*Nv)*exp(-(Eg*q)/(2*K*T))
phif = ((K*T)/q)*log10(Na/Ni);
Ed=3.9*8.5e-14; %permittivity of insulator

Vp = (q*Nd*A*A)/(2*E)
Vbi=((K*T)/q) * log((Na*Nd)/(Ni*Ni))
Vt=Vbi-Vp;
Nss=1e10;

Vds = [40,60,90];
for Vgs=-20:0.1:20;
  B=1+((q*t*Nss)/Ed);
  Vi=(q*E*Nd*t*t)/(2*Ed);
  K0=(B*PSIs0)-(2*sqrt(Vi*abs(PSIs0)));
  p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
  Is=q*Nd*Z*A*Vs
  fg1=(A*Ed)/1;
  f2=(q*Nss*p*A);
  fg3=E+fg2;
  fg4=fg3*t;
  fg5=p*A*Ed;
  fg6=fg4+fg5;
  fg=fg1./fg6;
  gm=(Is/Vp)*fg;
  plot(Vgs,gm)
end

ylabel(' Transconductance, gm (ms)')
xlabel('Gate to Source Voaltage, Vgs (V) ')
title('Transconductance Vs Gate to Source Voaltage ')
text(-18.0,1.9e-03,'U = 700')
Code 3: Gate Source Capacitance Vs Insulator Thickness

clc;
clear all;
close all;
q = 1.6e-19; % e- Charge
U = 700; % Low field Drift Mobility
Z = 260e-04; % Gate Width
Lg = 4e-04; % Gate Length
A = 0.8e-04; % Active Layer
K = 1.3807e-23;
T = 300;
Na = 1e15;
Nd = 1e17; % Donor Concentration
E0 = 8.9; %permittivity of semiconductor
E = E0 * 8.854e-14;
Ec = 5000; %electric field peak at carrier peak velocity
Eg = 3.23;
Nc = 3.25e15 * sqrt(T*T*T);
\[ N_v = 4.8 \times 10^{15} \sqrt{T \times T \times T}; \]
\[ \text{PSI fp} = \frac{E_g}{2} - \frac{((K \times T) / q) \times \log(N_c / N_d)}{2}; \]
\[ \text{PSI s0} = 2 \times \text{PSI fp}; \quad \text{%surface potential at 0 bias} \]
\[ t = 40 \times 10^{-7}; \quad \text{%insulator thickness nm} \]
\[ N_i = \sqrt{N_c \times N_v} \times \exp\left(-\frac{E_g \times q}{2 \times K \times T}\right); \]
\[ \phi_i = \frac{(K \times T) / q}{} \times \log\left(\frac{N_a}{N_i}\right); \]
\[ E_d = 3.9 \times 8.5 \times 10^{-14}; \quad \text{%permittivity of insulator} \]
\[ V_p = \frac{q \times N_d \times A \times A}{2 \times E}; \]
\[ V_{gs} = 0; \]
\[ V_{ds} = 100; \quad \text{%Vds} = V_{dss} \]
\[ V_{bi} = \frac{(K \times T) / q}{} \times \log\left(\frac{N_a \times N_d}{N_i \times N_i}\right); \]
\[ V_t = V_{bi} - V_p; \]
\[ G = 350 \times 10^{-4}; \]
\[ \text{%********************************************************************} \]
\[ N_{ss} = 5 \times 10^{12}; \]
\[ \text{for} \ t = 0:0.1 \times 10^{-7}:100 \times 10^{-7} \]
\[ B = 1 + \frac{(q \times t \times N_{ss})}{E_d}; \]
\[ V_i = \frac{q \times E \times N_d \times t \times t}{2 \times E_d}; \]
\[ K_0 = (B \times \text{PSI s0}) - (2 \times \sqrt{V_i \times \text{PSI s0}}); \]
\[ V_p = \frac{q \times N_d \times A \times A}{2 \times E}; \]
\[ p = (2 \times \sqrt{V_i} + \sqrt{V_i - (B \times (K_0 - V_{gs} - V_{ds}))}) / (B \times \sqrt{V_p}); \]
\[ f_g = \frac{(A \times E_d / 2) \times ((E + q \times N_{ss} \times \text{real}(p) \times A) \times t) + (\text{real}(p) \times E_d)}{A \times \text{real}(p) \times A}; \]
\[ C_f = \frac{E_d \times L_g}{G}; \]
\[ C_{ss} = q \times N_{ss} \times L_g; \]
\[ C_{ox} = \frac{E_d \times L_g \times Z}{t}; \]
\[ C_{gs} = \frac{(2 \times E \times Z \times \text{Lg} \times f_g) / A + C_f}{(Cgs + C_{ss}) \times \text{Cox}} / (Cgs + C_{ss} + C_{ox}); \]
plot(t,totalCgs)
hold on;
end

Nss=1e12 ;
for t= 0:0.1e-07:100e-07 ;
B=1+((q*t*Nss)/Ed);
Vi=(q*E*Nd*t*t)/(2*Ed);
K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
Vp = (q*Nd*A*A)/(2*E) ;
p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
fg = (A*Ed/2)./(((E+q*Nss*real(p)*A)*t)+(real(p)*Ed));
Cf=(E*Z*Lg)/G;
Css=q*Nss*Z*Lg;
Cox=(Ed*Lg*Z)/t;
Cgs=((2*E*Z*Lg*fg)/A)+Cf;
totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
plot(t,totalCgs,'r')
hold on;
end

ylabel('Normalized Gate Source Capacitance, Cgs (F)')
xlabel('Insulator Thickness ,tox (cm) ')
title('Gate Source Capacitance Vs Insulator Thickness')

xlim([0.1e-07 100e-07])
text(7.5e-06,7e-12,'Vds = 100V')
text(7.5e-06,6.3e-12,'Vgs = 0')
text(7.5e-06,5.6e-12,'Z = 260e-04')
text(7.5e-06,4.9e-12,'Lg = 4e-04')
Code 4: Cut Off Frequency Vs Channel Length – Vgs Differs

clc;
clear all;
close all;
q = 1.6e-19; % e- Charge
U = 700; % Low field Drift Mobility
Z = 260e-04; % Gate Width
Lg = 4e-04; % Gate Length
A = 0.8e-04; % Active Layer
K = 1.3807e-23;
T = 300;
Na = 1e15;
Nd = 1e17; % Donor Concentration
E0 = 8.9; %permittivity of semiconductor
E = E0*8.854e-14;
Ec = 5000; %electric field peak at carrier peak velocity
Eg = 3.23;
Nc = 3.25e15*sqrt(T*T*T);
Nv = 4.8e15*sqrt(T*T*T);
PSIfp = (Eg/2) - (((K*T)/q)*log(Nc/Nd))
\[ PSI_{0} = 2 \times PSI_{fp} \] % surface potential at 0 bias
\[ t = 40 \times 10^{-8}; \] % insulator thickness nm
\[ N_i = \sqrt{N_c \times N_v} \times \exp(-\frac{(E_g \times q)}{(2 \times K \times T)}) \]
\[ \phi_{fi} = \left( \frac{(K \times T)}{q} \right) \log_{10}(Na/Ni); \]
\[ Ed = 3.9 \times 8.5 \times 10^{-14}; \] % permittivity of insulator
\[ V_p = \left( \frac{q \times N_d \times A \times A}{2 \times E} \right) \]
\[ V_{ds} = 30; \] % \( V_{ds} \geq V_{dss} \)
\[ V_{bi} = \left( \frac{(K \times T)}{q} \right) \log_{10}\left( \frac{(Na \times N_d)}{(Ni \times Ni)} \right) \]
\[ V_t = V_{bi} - V_p \]
\[ G = 350 \times 10^{-4}; \]
\[ t = 40 \times 10^{-8}; \]
\[ V_{sat} = U \times E_c; \] % sauraion carrier voltage
\[ \%*************************************** \]
\[ V_{gs} = 0; \]
\[ N_{ss} = 5 \times 10^{11}; \]
\[ \text{for } L_g = 0.1 \times 10^{-4}:0.001 \times 10^{-4}:1 \times 10^{-4}; \]
\[ B = 1 + \left( \frac{q \times t \times N_{ss}}{Ed} \right); \]
\[ V_i = \left( \frac{q \times E \times N_d \times t \times t}{2 \times E_d} \right); \]
\[ K_0 = (B \times PSI_{0}) - (2 \times \sqrt{Vi \times PSI_{0}}); \]
\[ V_p = \left( \frac{q \times N_d \times A \times A}{2 \times E} \right); \]
\[ p = \left( -\sqrt{Vi} + \sqrt{Vi - (B \times (K_0 + V_{gs} - V_{ds}))} \right)/(B \times \sqrt{V_p}); \]
\[ f_g = \left( \frac{A \times E_d}{2} \right)/(((E + q \times N_{ss} \times \text{real}(p) \times A) \times t) + (\text{real}(p) \times E_d)); \]
\[ C_f = (E \times Z \times L_g)/G; \]
\[ C_{ss} = q \times N_{ss} \times Z \times L_g; \]
\[ C_{ox} = (E_d \times L_g \times Z)/t; \]
\[ C_{gs} = \left( \frac{2 \times E \times Z \times L_g \times f_g}{A} \right) + C_f; \]
\[ \text{totalCgs} = (C_{gs} + C_{ss}) \times C_{ox}/(C_{gs} + C_{ss} + C_{ox}); \]
Is=q*Nd*Z*A*Vsat;
fg=((A*Ed)/2)/(((E+(q*Nss*p*A))*t)+(p*A*Ed));
gm=(Is/Vp)*fg;
ft=gm/(2*pi*totalCgs);
   plot(Lg,ft)
   hold on;
end
plot(Lg,ft)
hold on;

Vgs=-6;
Nss=5e11;
for Lg= 0.1e-04:0.001e-04:1e-04;
  B=1+((q*t*Nss)/Ed);
  Vi=(q*E*Nd*t*t)/(2*Ed);
  K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
  Vp = (q*Nd*A*A)/(2*E) ;
  p = (-sqrt(Vi)+sqrt(Vi-(B*(K0-Vgs-
                   Vds)))/(B*sqrt(Vp));
  fg = (A*Ed/2)/(((E+q*Nss*real(p)*A)*t)+(real(p)*Ed));
  Cf=(E*Z*Lg)/G;
  Css=q*Nss*Z*Lg;
  Cox=(Ed*Lg*Z)/t;
  Cgs=((2*E*Z*Lg*fg)/A)+Cf;
  totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
  Is=q*Nd*Z*A*Vsat;
  fg=((A*Ed)/2)/(((E+(q*Nss*p*A))*t)+(p*A*Ed));
  gm=(Is/Vp)*fg;
  ft=gm/(2*pi*totalCgs);
     plot(Lg,ft,'r')

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hold on;
end
%******************************************************************************
Vgs=-12;
Nss=5e11
for Lg= 0.1e-04:0.001e-04:1e-04 ;
B=1+((q*t*Nss)/Ed);
Vi=(q*E*Nd*t*t)/(2*Ed);
K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
Vp = (q*Nd*A*A)/(2*E) ;
p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
fg = (A*Ed/2)./(((E+(q*Nss*real(p)*A)*t)+(real(p)*Ed));
Cf=(E*Z*Lg)/G;
Css=q*Nss*Z*Lg;
Cox=(Ed*Lg*Z)/t;
Cgs=((2*E*Z*Lg*fg)/A)+Cf;
totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
Is=q*Nd*Z*A*Vsat;
fg=((A*Ed)/2)/(((E+(q*Nss*p*A)) *t)+(p*A*Ed));
gm=(Is/Vp)*fg;
ft=gm/(2*pi*totalCgs);
    plot(Lg,ft,'g')
    hold on;
end
ylabel('Cut Off Frequency, ft (hz)')
xlabel('Channel Length, Lg (cm) ')
title('Cut Off Frequency Vs Channel Length')
xlim([0.1e-04 10e-05])
text(8e-05,9.0e09,'Vds = 30V')
Code 5: Cut Off Frequency Vs Channel Length - tox Differs

clc;
clear all;
close all;
q = 1.6e-19; % e- Charge
U = 700; % Low field Drift Mobility
Z = 260e-04; % Gate Width
Lg = 4e-04; % Gate Length
A = 0.8e-04; % Active Layer
K = 1.3807e-23;
T = 300;
Na = 1e15;
Nd = 1e17; % Donor Concentration
E0 = 8.9; % permittivity of semiconductor
E = E0*8.854e-14;
Ec = 5000; %electric field peak at carrier peak velocity
Eg = 3.23;
Nc = 3.25e15*sqrt(T*T*T);
Nv = 4.8e15*sqrt(T*T*T);
PSIfp=(Eg/2)-(((K*T)/q)*log(Nc/Nd))
PSIs0=2*PSIfp %surface potential at 0 bias

t=40e-08; %insulator thickness nm
Ni = sqrt(Nc*Nv)*exp(-(Eg*q)/(2*K*T))
phif=((K*T)/q)*log10(Na/Ni);
Ed=3.9*8.5e-14; %permittivity of insulator

Vp = (q*Nd*A*A)/(2*E)
Vgs=0;
Vds =30; %Vds>=Vdss
Vbi=((K*T)/q)*log((Na*Nd)/(Ni*Ni))
Vt=Vbi-Vp
G=350e-04;
Vsat=U*Ec; %sauraion carrier voltage

%********************************************************************

for Lg= 0.1e-04:0.001e-04:1e-04 ;
B=1+((q*t*Nss)/Ed);
Vi=(q*E*Nd*t*t)/(2*Ed);
K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
Vp = (q*Nd*A*A)/(2*E) ;
p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
fg = (A*Ed/2).(((E+q*Nss*real(p)*A)*t)+(real(p)*Ed));
Cf=(E*Z*Lg)/G;
Css=q*Nss*Z*Lg;
Cox=(Ed*Lg*Z)/t;
Cgs=((2*E*Z*Lg*fg)/A)+Cf;
totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
Is=q*Nd*Z*A*Vsat;
fg=((A*Ed)/2)/(((E+(q*Nss*p*A)) *t)+(p*A*Ed));
gm=(Is/Vp)*fg;
ft=gm/(2*pi*totalCgs);
plot(Lg,ft)
hold on;
end

%*****************************************************************************************% 

 t=60e-07;
 Nss=5e11;
 for Lg= 0.1e-04:0.001e-04:1e-04 ;
 B=1+((q*t*Nss)/Ed);
 Vi=(q*E*Nd*t*t)/(2*Ed);
 K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
 Vp = (q*Nd*A*A)/(2*E) ;
 p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
 fg = (A*Ed/2) ./(((E+q*Nss*real(p)*A) *t)+(real(p)*Ed));
 Cf=(E*Z*Lg)/G;
 Css=q*Nss*Z*Lg;
 Cox=(Ed*Lg*Z)/t;
 Cgs=((2*E*Z*Lg*fg)/A)+Cf;
totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
Is=q*Nd*Z*A*Vsat;
fg=((A*Ed)/2)/(((E+(q*Nss*p*A)) *t)+(p*A*Ed));
gm=(Is/Vp)*fg;
ft=gm/(2*pi*totalCgs);
plot(Lg,ft,'r')
hold on;
end

%***********************************************************************
t=80e-07;
Nss=5e11;
for Lg= 0.1e-04:0.001e-04:1e-04;
    B=1+((q*t*Nss)/Ed);
    Vi=(q*E*Nd*t*t)/(2*Ed);
    K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
    Vp = (q*Nd*A*A)/(2*E);
    p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
    fg = (A*Ed/2)./(((E+q*Nss*real(p)*A)*t)+(real(p)*Ed));
    Cf=(E*Z*Lg)/G;
    Css=q*Nss*Z*Lg;
    Cox=(Ed*Lg*Z)/t;
    Cgs=((2*E*Z*Lg*fg)/A)+Cf;
    totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
    Is=q*Nd*Z*A*Vsat;
    fg=((A*Ed)/2)/(((E+(q*Nss*p*A))*t)+(p*A*Ed));
    gm=(Is/Vp)*fg;
    ft=gm/(2*pi*totalCgs);
    plot(Lg,ft,'g')
    hold on;
end
ylabel('Cut Off Frequency, ft (hz)'
xlabel('Channel Length, Lg (cm)'
title('Cut Off Frequency Vs Channel Length')
xlim([0.1e-04 1e-04])
text(8e-05,14e09,'Vds = 30V')
text(8e-05,13.3e09,'Vgs = 0')
text(8e-05,12.6e09,'Z = 260e-04')
text(8e-05,11.9e09,'Lg = 4e-04')
text(8e-05,11.2e09,'A = 0.8e-04')
text(8e-05,10.5e09,'Na = 1e15')
text(8e-05,9.8e09,'Nd = 1e17')
text(8e-05,9.1e09,'Nss = 5e11')
legend('tox = 40e-07','tox = 60e-07','tox = 80e-07')

**Code 6: Cut Off Frequency Vs Insulator Thickness**

clc;
clear all;
close all;
q = 1.6e-19; % e- Charge
U =700; % Low field Drift Mobility
Z= 260e-04; % Gate Width
Lg = 4e-04; % Gate Length
A = 0.8e-04; % Active Layer
K=1.3807e-23;
T=300;
Na = 1e15;
Nd = 1e17; % Donor Concentration
E0= 8.9; %permittivity of semiconductor
E= E0*8.854e-14;
Ec=5000; %electric field peak at carrier peak velocity
Eg= 3.23;
Nc = 3.25e15*sqrt(T*T*T);
Nv = 4.8e15*sqrt(T*T*T);
PSIfp=(Eg/2)-(((K*T)/q)*log(Nc/Nd))
PSIs0=2*PSIfp %surface potential at 0 bias
t=40e-08; %insulator thickness nm
Ni = sqrt(Nc*Nv)*exp(-(Eg*q)/(2*K*T))
phif=((K*T)/q)*log10(Na/Ni);
Ed=3.9*8.5e-14; %permittivity of insulator
Vp = (q*Nd*A*A)/(2*E)
Vgs=0;
Vds =100; %Vds>=Vdss
Vbi=((K*T)/q)*log((Na*Nd)/(Ni*Ni))
Vt=Vbi-Vp
G=350e-04;
Vsat=U*Ec; %sauraion carrier voltage
Nss=5e11 ;
for t= 0:0.1e-07:100e-07 ;
B=1+((q*t*Nss)/Ed);
Vi=(q*E*Nd*t*t)/(2*Ed);
K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
Vp = (q*Nd*A*A)/(2*E) ;
p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vd))))/(B*sqrt(Vp));
fg = (A*Ed/2)./(((E+q*Nss*real(p)*A)*t)+(real(p)*Ed));
Cf=(E*Z*Lg)/G;
Css=q*Nss*Z*Lg;
Cox=(Ed*Lg*Z)/t;
Cgs=((2*E*Z*Lg*fg)/A)+Cf;
totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
Is=q*Nd*Z*A*Vsat;
fg=((A*Ed)/1)/(((E+(q*Nss*p*A))*t)+(p*A*Ed));
gm=(Is/Vp)*fg;
ft=gm/(2*pi*totalCgs);
    plot(t,ft)
    hold on;
end

%**********************************************************************
Nss=1e12 ;
for t= 0:0.1e-07:100e-07 ;
    B=1+((q*t*Nss)/Ed);
    Vi=(q*E*Nd*t*t)/(2*Ed); 
    K0=(B*PSIs0)-(2*sqrt(Vi*PSIs0));
    Vp = (q*Nd*A*A)/(2*E) ;
    p = (-sqrt(Vi)+sqrt(Vi-(B*(K0+Vgs-Vds))))/(B*sqrt(Vp));
    fg = (A*Ed/2)./(((E+q*Nss*real(p)*A)*t)+(real(p)*Ed));
    Cf=(E*Z*Lg)/G;
   Css=q*Nss*Z*Lg;
    Cox=(Ed*Lg*Z)/t;
    Cgs=((2*E*Z*Lg*fg)/A)+Cf;
totalCgs=((Cgs+Css)*Cox)/(Cgs+Css+Cox);
Is=q*Nd*Z*A*Vsat;
fg=((A*Ed)/2)/(((E+(q*Nss*p*A))*t)+(p*A*Ed));
gm=(Is/Vp)*fg;
ft=gm/(2*pi*totalCgs);
    plot(t,ft,'r')
    hold on;
end

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ylabel('Cut Off Frequency, ft (hz)')
xlabel('Insulator Thickness, tox (cm)')
title('Cut Off Frequency Vs Insulator Thickness')
xlim([0.1e-07 100e-07])
text(7.80e-06,4.20e08,'Vds = 100V')
text(7.80e-06,4.0e08,'Vgs = 0')
text(7.80e-06,3.80e08,'Z = 260e-04')
text(7.80e-06,3.60e08,'Lg = 4e-04')
text(7.80e-06,3.40e08,'A = 0.8e-04')
text(7.80e-06,3.20e08,'Na = 1e15')
text(7.80e-06,3.0e08,'Nd = 1e17')
text(7.80e-06,2.80e08,'Nss = 1e12')
legend('Nss = 5e11','Nss = 1e12')