THE FABRICATION AND CHARACTERIZATION OF A 4H-SILICON CARBIDE METAL-SEMICONDUCTOR FIELD EFFECT TRANSISTOR

A graduate project submitted in partial fulfillment of the requirements
For the degree of Master of Science in Electrical Engineering

By

Ira Ardoin

May 2015
The graduate project of Ira Ardoin is approved:

_____________________________     ____________________________
Dr. Matthew M. Radmanesh         Date

_____________________________     ____________________________
Dr. Barton J. Gordon              Date

_____________________________     ____________________________
Dr. Somnath Chattopadhyay, Chair  Date

California State University, Northridge
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THE FABRICATION AND CHARACTERIZATION OF A 4H-SILICON CARBIDE METAL-SEMICONDUCTOR FIELD EFFECT TRANSISTOR

By

Ira Ardoin

Master of Science in Electrical Engineering

The fabrication of the 4H-silicon carbide metal semiconductor field effect transistor (MESFET) is occurring in the Microelectronics Engineering Laboratory (MEL). There are various experiments occurring that characterize different aspects of the device, in order to achieve its optimum performance. The silicon dioxide (SiO$_2$) layer achieves widespread use in the microelectronics industry. This may be used for the dielectric field effect in MOS (metal oxide semiconductor) devices, as a field oxide for isolation between source, gate, and drain contacts, or for device isolation on a very crowded integrated circuit (IC). In this project, the SiO$_2$ is used for isolation between source, gate, drain, and devices. It is imperative to minimize the defect density in the SiO$_2$ layer to increase the reliability and performance of these devices. The quality of the SiO$_2$ is thus characterized by the fabrication of SiC MOS capacitors.

Thermal oxidation has been utilized in the fabrication of the SiO$_2$ in the 4H-SiC MOS capacitors adopting the nickel-SiO$_2$-4H-SiC (Ni/SiO$_2$/4H-SiC) structure. The SiO$_2$ layers have been grown onto Si-face and C-face 4H-SiC substrates employing the techniques of sputtering and wet thermal oxidation. The recipes for deposition by these
techniques are optimized by trial and error method. Atomic force microscopy (AFM) analysis is employed in the investigation of growth effects of SiO$_2$ on the Si- and C-face of these SiC substrates. MOS capacitors are made utilizing sputtering and wet oxidation methods on the Si-face of 4H-SiC wafers, which are studied utilizing C-V (capacitance versus voltage) techniques.
CHAPTER 1: INTRODUCTION

1.1 Silicon Carbide MOS Devices

SiC is an attractive semiconductor for optoelectronic devices including the optical 
MESFET owing to sufficient radiative recombination of electrons across the p-n junction.
SiC based devices exhibit qualities of survivability across highly irradiated and heated 
conditions. SiC will eventually replace the mature Si technology due to better 
performance. Lower defect-density Si-face 4H-SiC substrates are required rather than C-
face for the body of quality MOS devices [1].

In microelectronics, SiO$_2$ is widely used for such applications as electrical 
insulation, sacrificial barriers for ion-implantation, passivation, fiber-optic cables, and 
solid-state memory devices. The reliability of MOS devices in ICs relies on decreased 
thickness of the SiO$_2$ layer. Additionally, the breakdown electric field magnitude is 
determined by such parameters as leakage current, flat band voltage, band bending of 
surface or semiconductor potential, or thickness of insulator (SiO$_2$). A decrease in SiO$_2$
thickness contributes to the breakdown voltage [2]. There are certain applications where 
thickness can be traded-off.

MOS devices are a subset of MIS (metal-insulator semiconductor) devices, in 
which the insulator is the oxide layer. In an ideal MIS capacitor, the charge stored in the 
dielectric (Q) is commensurate to the voltage (V) between the plates:

\[ Q = CV \]

When a positive voltage is applied to one terminal, a negative charge exists on the 
opposite terminal, and this creates an electric field between the two plates. Due to the 
coulomb force, the atoms within the dielectric become polarized. If a dielectric is
composed of weakly bonded molecules, those molecules become polarized and reorient themselves so that their symmetry axes align to the field, creating an internal electric field that reduces the overall field within the dielectric. This "dielectric polarization" allows a capacitor to store energy between its plates.

The most common conduction mechanism by electrons through insulators under high electric fields is tunneling. Tunnel emission describes the process whereby a potential barrier is penetrated by the electron wave function as the result of quantum mechanics. Tunnel emission can be subdivided into direct tunneling and FN tunneling. Fowler-Nordheim tunneling occurs when carriers tunnel through a partial width of the potential barrier. The current density as a function of electric field has the equation:

\[ J = C_4 E_1^2 \exp \left( \frac{-E_0}{E_1} \right) \]

where \( C_4 = \frac{q^2}{16\pi^2 h \varphi_{ox}} \), \( E_0 = \frac{-4\sqrt{2m^*}(q\varphi_{ox})^{3/2}}{3hq} \), and \( E_1 \) is the applied electric field [14].

Consider the band diagram of an n-type Ni/SiO\(_2\)/4H-SiC MOS capacitor as shown in Figure 1, where the band gap of SiO\(_2\) is taken as 9.0 eV. The barrier height from the Fermi level of n-type 4H SiC to the edge of the conduction band of SiO\(_2\) is considered as 2.70 eV, whereas it is reported to be 3.05 eV to the edge of the valence band for p-type 4H SiC MOS devices [9,10]. This barrier height is likely smaller than that in the Ni/SiO\(_2\) interface. This leads to the difference in electron affinities of 4H-SiC semiconductor and SiO\(_2\). The electron affinity of 4H-SiC can be considered to be the difference between the work function of Ni metal and the barrier height of the Ni/4H-SiC interface [11]. The electron affinity of 4H-SiC, which measures from the Fermi level of semiconductor to the
vacuum level resides above the conduction band of 4H-SiC. The electron affinity of SiO2 is around 6.75 eV, whereas this value is around 4.05 eV for SiC.

In the p-type 4H-SiC MOS device, the electrons tunnel from the peak of the valence band to the conduction band of the SiO2 layer during forward-bias. In the n-type device, the electrons tunnel from the lowest point on the conduction band of the semiconductor to the conduction band of the oxide layer. At higher electric fields, the electron tunneling is elastic, where nuclear stopping occurs and energy from the tunneling atom is transferred to the stationary atom. At lower electric fields, the tunneling collisions are inelastic and affect the electronic stopping mechanism by ionization with the lattice atoms. The effect of the lower field on the current is minimal.

Figure 1: Electronic band structure of an n-type SiO2/4H-SiC MOS device [43].

1.2 Silicon Carbide MESFET

As stated earlier, the 4H-SiC is a wide bandgap material, having a bandgap of 3.26 eV at room temperature. Additionally, its exemplary electrical properties such as
increased saturation velocity, thermal conductivity, and high breakdown field magnitude make it an excellent candidate for high-temperature, high-power MESFETs.

Figure 2: The cross section of a silicon carbide MESFET, illustrating the basic device dimensions such as gate length ($L_g$), distance from gate to source ($L_{gs}$), distance from gate to drain ($L_{gd}$), and source and drain widths ($L_s$ and $L_d$, respectively).

The idea behind the MESFET is the use of the potential energy barrier for electrons formed at the interface of a metal and a semiconductor. The "Schottky barrier", as it is known, uses the height of the potential energy barrier of the metal gate to modulate current in the buried channel [14]. Consider a typical structure in Figure 2. The device is based on a semi-insulating substrate on which an n-type region is fabricated epitaxially to form an “electrically-active” conducting channel of height 'a'.

In terms of their dimensions, a typical MESFET can have a gate length ($L_g$ of 0.5) µm, and a gate width ($W_g$) of 500 µm. This device would be referred to as a $0.5 \times 500$ µm device. A typical microwave device has a gate length on the order of 0.1 ~ 1.0 µm, with an active layer height of one-fifth to one-third of the gate length. The cross-sectional area of the gate determines the deliverable current-capacity of the device, since the area depends on the gate width [14]:

$$I_{D_{Sat}} = \frac{W_g q \mu N_d a}{L} \left[ \frac{\phi_{po}}{3} - (\phi_{bi} - V_G) \left( 1 - \frac{2}{3} \sqrt{\frac{\phi_{bi} - V_G}{\phi_{po}}} \right) \right]$$
where \( L = \) gate width, \( W_z = \) channel width (into page), and \( a = \) channel depth.

Consider the case where the active channel is partially depleted, in Figure 3, where the energy band diagram of the MESFET is shown for negative-gate voltage, so that the channel is completely depleted [15]. A negative gate-bias changes the width of the depletion region in the metal-semiconductor junction, allowing modulation of the device conductance.

![Energy Band Profile](image.png)

Figure 3: The energy band profile of a MESFET with a negative gate bias which depletes the channel [15].

We can divide the MESFET's current-voltage (I-V) characteristics into three regions as follows:

i. Linear region: Consider the device with a small source drain bias (\( V_{DS} \)) with zero gate bias. \( I_D \) is proportional to \( V_D \).

ii. Nonlinear region: The gate bias is consistent as the drain bias is increased. The gate-semiconductor junction is reverse biased.

iii. Saturation: As the gate bias is increased and the gate semiconductor junction is negative biased, the current decreases until the channel is devoid of free-carriers. As "pinch-off" occurs, the current cannot increase even if the drain voltage is increased.
The reverse gate-bias required for "pinch-off" is approximated by the depletion width of the channel [14]:

\[ W_D = \left[ \frac{2\varepsilon_s (\phi_{bi} - V_{GS})}{q N_d} \right]^{1/2} \]

where \( \varepsilon_s \) is the permittivity of the semiconductor. For 4H-SiC, \( \varepsilon_s = 9.7(8.854 \times 10^{-14} \) F/cm) = 8.588 \times 10^{13} \) F/cm. \( N_d \) is the doping concentration in the channel. In a p-channel device, a positive gate-bias is needed for pinch-off. The pinch-off potential \( \phi_{po} \) is defined by [14]:

\[ \phi_{po} = \frac{q N_d a^2}{2\varepsilon_s} \]

and the gate voltage required for pinch-off in an n-channel device is

\[ V' = V_{bi} - V_{Th} \]

with \( V_{Th} \) signifying the threshold voltage. The "enhancement-mode" device consists of a conducting channel with "free-charge" during forward gate-bias. The device channel is completely depleted when the pinch-off voltage is less than the built-in voltage (\( V_{bi} > V_p \)). On the other hand, in a "depletion mode device" (\( V_p > V_{bi} \)), the channel is only partially depleted and carries free charge at zero gate bias (\( V_G = 0 \)). A reverse gate-bias will turn off the device during channel depletion.

The fabrication of ion-implanted SiC MESFET's are typically achieved by starting with a bulk SiC substrate, such as those manufactured by Cree Research. The devices are then fabricated on the top (Si-face) of the substrate. Epitaxial layers are grown on the substrate. To fabricate an n-type MESFET, a p-type epitaxial-layer ("epi-layer") is grown on an insulative n-type substrate, and an n-type epi-layer is grown above to serve as the conducting channel. \( N^+ \) regions are doped via ion implantation in the n-
type epi-layer. Metal ohmic contacts are deposited above the n$^+$ regions for source and drain contacts, and a metal contact is formed above the channel to serve as the Schottky gate.

4H-SiC MESFET's implanted with nitrogen ions were fabricated and characterized by Shou Guo Wang at Northwest University in Xi'an, China in 2011. 4H-SiC with p-type epi-layers were grown at Cree. The following process was used to achieve the structure shown in Figure 4:

i. N-wells ion implantation: The N-wells were formed by multiple-fold ion implantation of nitrogen on the silicon-face at a temperature of 300°.

ii. Annealing: The N$^+$ regions for source and drain ohmic contacts were formed at 300° after re-patterning. The sample was then annealed for 1800 seconds in argon at an ambient temperature of 1650° celsius.

iii. Source and drain Ohmic metal deposition, lift-off, and annealing: Ohmic contact windows are formed on SiO$_2$, and the nickel-chromium source and drain ohmic contacts and gold gate contacts are evaporated and alloyed at 900° C for 30 minutes in a vacuum furnace.

iv. Schottky gate metal deposition and lift-off: Schottky contacts are formed through evaporation of a titanium-platinum-gold alloy after the silicon dioxide is deposited.

v. Pad metallization. Au is used for ease of probe testing.
Figure 4: a) The ion-implanted 4H-SiC MESFET fabricated by Wang, showing the implanted $N^+$ regions. b) Layout for the experiment showing the MESFET's and Schottky Barrier Diodes (SBD's). Test structures were also fabricated on the wafer including transmission line methods (TLM's) and Van Der Pauw structures [28].

Wang differentiates between the use of ion-implantation for doping of MESFET's and the conventional method of plasma-etching for fabrication of gate and metal contacts and device isolation on the SiC multi-epi-layers. Plasma-etching lowers device performance, such as augmenting gate leakage current, hindering N-well carrier mobility, and lowering the Schottky contact's resistivity. In order to achieve uniformity of implanted channel, it is often beneficial to use multiple fold implantations to fabricate the active regions. The implantation energies and doses for the two samples mentioned in this experiment to form the channels are for Sample A: 55, 100, and 160 keV with a sample dose of $10^{13}$; and for Sample B: 55, 100, 160, and 240 keV at the same sample dose. An additional implantation is done with an energy of 30 keV and dose of $3.54 \times 10^{14}$ cm$^{-2}$ to form the active regions.

As stated previously, a SiO$_2$ sacrificial barrier was used for the ion implantation and this was calculated using the equation:
\[ R = R_{pl} + 3\sigma_i \]

where \( R_{pl} \) is the mean depth (projected range) and \( \sigma_i \) is the longitudinal straggle for the highest energy from Transport of Ions in Matter (TRIM) calculation. This mask layer can stop 99% of the ions from entering the semiconductor.

The ion-implantation parameters such as implantation times, ion energies, and doses will determine the device's physical characteristics such as source and drain N+ -doping concentration and channel depth [28].

J.B. Tucker, et. al., at George Mason University in Virginia, reported the successful fabrication and characterization of ion implanted MESFETs in semi-insulating 4H-silicon carbide. Semi-insulating is the quality of certain semiconductors which have low carrier concentration and hence, wide energy band gap, which are undoped and allow better electrical isolation between adjacent devices. For example, it was shown by N.T. Son, et. al., in "Defects and carrier compensation in semi-insulating 4H-SiC substrates", where semi-insulating 4H-SiC was grown, having donor concentrations of \( 1 \times 10^{15} \text{ cm}^{-3} \) - \( 1 \times 10^{16} \text{ cm}^{-3} \) [20].

J.B. Tucker's experimental procedure consisted of the fabrication of n-type MESFETs on 8° off-axis Si-face bulk, semi-insulating 4H-silicon carbide utilizing ion implantation. The energies and dosages are shown in the table below:
Table 1: Values used for ion implant energies (keV) and ion dosages (cm\(^{-2}\)) for doping of channel and source/drain regions used by J.B. Tucker [21].

<table>
<thead>
<tr>
<th>Implant</th>
<th>Energy (keV)</th>
<th>Dose (cm(^{-2}))</th>
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<tbody>
<tr>
<td>Nitrogen (channel)</td>
<td>20</td>
<td>1.7(\times)10(^{12})</td>
</tr>
<tr>
<td></td>
<td>45</td>
<td>3.0(\times)10(^{12})</td>
</tr>
<tr>
<td></td>
<td>80</td>
<td>4.0(\times)10(^{12})</td>
</tr>
<tr>
<td></td>
<td>130</td>
<td>5.0(\times)10(^{12})</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>8.0(\times)10(^{12})</td>
</tr>
<tr>
<td>Nitrogen (source/drain)</td>
<td>20</td>
<td>5.7(\times)10(^{13})</td>
</tr>
<tr>
<td></td>
<td>45</td>
<td>1.0(\times)10(^{14})</td>
</tr>
<tr>
<td></td>
<td>80</td>
<td>1.33(\times)10(^{14})</td>
</tr>
<tr>
<td></td>
<td>130</td>
<td>1.67(\times)10(^{14})</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>2.67(\times)10(^{14})</td>
</tr>
</tbody>
</table>

A patterned photoresist layer of 1.5 µm was used as an implant mask prior to each implantation. The wafer was subsequently annealed in argon ambient for 900 seconds in an induction furnace at 1450° celsius. Source and drain ohmic contacts were created using a lift-off process and electron beam physical vapor deposition, followed by a 1200° C anneal for 180 seconds in vacuum. Channel thickness was achieved for a specified pinch-off voltage by dry etching (RIE) in sulfur hexafluoride utilizing the ohmic regions as an etchant mask. A 100 nm Al gate was patterned using e-beam evaporation and lift-off. The MESFETs I-V characteristic along with its physical structure are shown in the following figure:
Figure 5: a) Forward I-V characteristic and diagram showing peak ion concentrations. b) Negative-bias current-voltage characteristics of the Al Schottky contact [31].

Characterization of the device was performed using the on-wafer transmission line model (TLM) patterns. The resistivity of the as-grown wafer was given as greater than $1 \times 10^5 \, \Omega \, \text{cm}$. 450 µm isolation between devices was measured to have greater than $1 \times 10^{10} \, \Omega \, \text{cm}$, which is sufficient for interdevice isolation. C-V measurements of the recessed channel indicated that the implanted dopant concentration was $3 \times 10^{17} \, \text{cm}^{-3}$, a 50% activation of implanted nitrogen species. Van der Pauw Hall measurements were used to measure carrier concentration and mobility. Current-voltage measurements were linear in a semi-log plot over six decades of current. There was no significant leakage.
current in the reverse direction up to a reverse-bias $V_{gs} = -18$V. The built-in voltage was extracted as 1.1 V for the Al gate using the $1/C^2-V$ curve.

Additional devices implanted with phosphorus were fabricated by Tucker for comparison with the N-implanted devices. These processes were identical except for the fact that the channel was implanted with phosphorus, while source and drain regions were still doped with nitrogen. Implant schedules for channel and source/drain doping are shown below:

<table>
<thead>
<tr>
<th>Implant</th>
<th>Energy (keV)</th>
<th>Dose (cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phosphorus (channel)</td>
<td>30</td>
<td>$1.10 \times 10^{12}$</td>
</tr>
<tr>
<td></td>
<td>65</td>
<td>$1.62 \times 10^{12}$</td>
</tr>
<tr>
<td></td>
<td>110</td>
<td>$2.29 \times 10^{12}$</td>
</tr>
<tr>
<td></td>
<td>170</td>
<td>$3.32 \times 10^{12}$</td>
</tr>
<tr>
<td></td>
<td>275</td>
<td>$6.80 \times 10^{12}$</td>
</tr>
</tbody>
</table>

Table 2: Values used for phosphorous ion implant energies (keV) and ion dosages (cm$^{-2}$) for doping of channel used by J.B. Tucker [32].

A cross-sectional view of the device as well as the forward-bias I-V characteristic is shown below:
As with the nitrogen-doped sample, Van der Pauw Hall measurements were demonstrated in the phosphorous-doped channel. Doping concentration on the Al Schottky gate was $3 \times 10^{17}$ cm$^{-3}$, which was consistent with nitrogen. This suggests that for low-doping concentrations, phosphorous implantation fails to create higher carrier mobility. The forward I-V characteristics for phosphorous was linear over the pA to nA range. The built-in potential extracted from the I-V curve was 2.0 V. The reverse-biased I-V characteristics exhibited low-leakage current of $\sim 1.0$ nA at -20 V. The Transmission Line Model (TLM) test patterns were used to measure the Ni source/drain ohmic contact resistance ($\rho_c$), which was found as $\sim 10^{-2}$ $\Omega$ cm$^2$, which was consistent for nitrogen. Mutual transconductance ($g_m$) was found to be 2.33 mS at $V_{gs} = -5$ V and $V_{ds} = 25$ V. The resulting channel carrier mobility was $\sim 32$ cm$^2$/Vs. This effective channel carrier mobility value is 4-5 times smaller in both the nitrogen and phosphorous-doped devices than the value calculated from the bulk Hall mobility. The high source/drain ohmic
contact resistance is thought to create the poor transconductance in these devices. This contact resistance needs to be reduced in order to realize the optimum characteristics of these fully-implanted 4H-SiC MESFETs [32].

A similar experiment was done by J.H. Yim, et. al., at Seoul National University. In Yim's experiment, the 4H-SiC substrates acquired from Cree, Inc., consisted of high-purity semi-insulating (HPSI) 4H-silicon carbide with a sequential p-type buffer layer. The channel epi-layer was reduced to 0.22 µm by using a dry-etching process. The cross-sectional schematic is shown in Figure 9.

MESFETs of varying gate lengths were fabricated: (Lg) of 0.3, 0.5, 1.0, 2.0, and 3.0 µm. Current-voltage characteristics with varying ion-implantation depths were simulated using ATLAS 2D simulator from Silvaco. The experimental DC characteristics were extracted and plotted against the simulated results. The experimentally determined I-V curves, below, are showing weak saturation characteristics.

In the experiment, both thin and thick-channel MESFETs were processed using different ratios of ion-implantation-depth to channel-depth due to similar ion-implantation depths of 0.2 µm. Implanted regions in the thick-channel MESFETs formed shallow regions, whereas the thin-channel MESFETs formed deep regions (the entire depth of channel).
Highly-doped regions created by deep implantation show a reduction in source and drain resistances and magnification of drain current, which leads to an increase in the field potential along the channel and density of electrons. The depletion region between the channel and buffer layer maintains a high drain bias, creating a parasitic bipolar transistor, also known as the source-to-drain punch-through effect. This has the effect of limiting the maximum operating voltage and output power.

Analysis of these MESFETs showed that particularly shallow implantation depth of under 0.14 μm brings on a current crowding effect in the ohmic regions and increases source and drain resistances. Yim further concluded that shallow implantation is necessary for decreasing the short-channel effect. Simultaneously, shallow depths under 0.14 μm must be avoided as they degrade device performance [33].

1.3 Silicon Carbide Schottky Diodes

RF high-power MESFETs are currently being offered commercially, and there is an emerging market for Schottky diodes made from SiC. We are still at the beginning of the SiC revolution, however, and the material’s full potential has yet to be realized.
1.4 Silicon Carbide Optoelectronic Applications

The industrial application of SiC began with the blue light emitting diode (LED), which was very weak due to the indirect bandgap of SiC but was the only commercial blue electroluminescent light source at the time (the late 1980s). The SiC blue LED was soon surpassed in intensity by the gallium nitride (GaN)-based LED due to the direct bandgap of the III-nitrides. However, due to the lack of a native substrate for GaN, sapphire or SiC substrates were and are still used. The biggest use of semiconductor-grade SiC is still for LEDs, but now it serves the role as the substrate for the active GaN layer rather than both the substrate and the active layer.

1.5 SiC as Substrates for GaN High Electron Mobility Transistors

Like SiC, Gallium Nitride (GaN) has emerged as a major semiconductor in high-power, high-frequency devices for wireless, switching power control, and optoelectronic applications. This is due to its wide band gap energy (3.39 eV). High-electron mobility transistors (HEMTs) until the 1990s were fabricated primarily using AlGaAs/GaAs and now are being replaced by AlGaN/GaN. GaN-based semiconductors are materials of high-hardness and these materials are grown epitaxially on sapphire or insulating 4H-SiC, due to low mismatch in their lattice constants. AlGaN/GaN HEMTs are being utilized in both high-power and low noise amplification, where sizable gains are achieved, as well as noise figures slightly higher than GaAs. Output power is significantly higher than GaAs.

The basic operation of the HEMT consists of channel formation from carriers accumulated along a substantially asymmetric heterojunction between a heavily doped
high bandgap and a lightly doped low bandgap region. In HEMTs based on GaN substrates, this carrier accumulation is mainly due to polarization charges developed along the heterojunction in the high bandgap AlGaN side. The accumulated carriers might have high mobility due to their separation from their heavily doped source region, and their location in the low-doped region where impurity scattering is absent.

The heterojunction layers are fabricated using MOCVD (metalorganic chemical vapor deposition) or MBE (molecular beam epitaxy). Short ~ 0.1 µm T-shaped gates are fabricated using electron beam lithography (EBL). Small-signal HEMTs are used in low-noise receiver front-end applications as opposed to large-signal power devices, resulting in smaller area since the power devices require larger currents which increase the device area.

Typical AlGaN/GaN HFETs are fabricated with the source-to-drain spacing from 2 µm to 7 µm, the gate length from 0.25 µm to 5 µm, and the total gate width from 50 µm to 150 µm (2 x 25 µm to 2 x 75 µm). T-shaped gate contacts are employed, providing short channel lengths, while the wide "cap" reduces the gate resistance of the ohmic contact. The gate contact is the Schottky type, made using Ni/Au, Pt/Au, or Pd/Au.
CHAPTER 2: SILICON CARBIDE

2.1 Introduction

SiC, GaN, and ZnSe belong to the family of materials known as the "wide-bandgap semiconductors," that is, their bandgap energies (difference in valence and conduction band energies) are highest of the semiconductors, with 3.2 eV, 3.45 eV, and 3.6 eV, respectively [2]. All three of the aforementioned materials are suitable for optoelectronic devices, but only SiC and GaN are utilized in high-power, high-thermal, and microwave-frequency applications [3].

The leading contender for high-temperature and high-power applications in modern technology is SiC. These facts are qualified by the very high operating temperature of SiC (1600°C), and high saturation velocity (2 x 10^{-7} cm/s). The high saturated drift velocity is necessary in obtaining higher channel currents in microwave devices such as MESFET's, which invariably makes SiC suitable for high-gain solid-state devices [4].

SiC can be produced on earth and also found in outer space. For example, presolar SiC grains have been found in meteorites. Their morphology has been extensively studied by electron microscopy and the elemental and isotopic compositions analysis by SIMS (secondary ion mass spectrometry).

Including silicon carbide, five types of presolar matters have been identified in chondrites, namely diamond (about 2.6 nm), graphite (0.8–7 l m), silicon carbide (0.05–20 l m), silicon nitride, and aluminum oxide. The anomalous isotopic compositions of Si, C, O, and N demonstrate that the grains have a presolar origin. Studies on presolar diamond, graphite, and silicon carbide in chondrites show that
the abundance of these elements is attributed to the chemical structures of the meteorites [5]. SiC’s use dates back to 1906 when it was used as the first semiconductor crystal radio detector. In 1907 it was used to make the first light emitting diode (LED) [3].

2.2 Crystal Growth

SiC wafers used to fabricate high-performance semiconductor devices require exceptional electrical properties. As such, it is required that the wafers be relatively defect-free and of single-crystal nature, meaning they have long-range order over many atomic or molecular dimensions. Their crystal lattice structure should have a high degree of geometric order or periodicity.

The methods used to grow such crystals require high control over physical growth parameters, which might include temperature, RF heating, heat generation within a graphite susceptor by eddy currents, heat transfer by conduction and radiation, species transport, growth kinetics, or material stress. These methods for crystal growth should also be economically viable for today's market. The two main growth techniques employed today in SiC crystal growth are (1) seeded sublimation growth, used in SiC boule growth, and (2) CVD, used in epitaxial growth on SiC substrates.

2.2.1 Growth From Seeded Sublimation

Seeded sublimation growth is used almost exclusively for growing bulk SiC crystal boules. The technique, also known as the "Modified Lely Method," was
developed in 1978 by Tairov and Tsvetkov [16]. A schematic of the modified Lely method is shown below:

Figure 8: Two variations of the Modified Lely Method, (a) seed sublimation from bottom, and (b) seed sublimation from top; (1) seed, (2) crystal boule, (3) SiC source material, (4) graphite crucible, (5) graphite powder, (6) porous graphite cylinder [2].

The Modified Lely Method has evolved into the seeded sublimation growth method in use today, which has become the industry standard for growth of bulk SiC, and is the only method in use by industry today for bulk growth of SiC ingots. These ingots are sliced into wafers, which are then used to fabricate the devices.

In seeded sublimation growth, a SiC boule, or ingot is created by dipping a seed crystal into pure SiC powder at high temperature and slowly extracted. The process occurs within an allotropic carbon (graphite) crucible, which is partially filled with SiC powder. The second configuration is the most common used today, with the source material held at the bottom of the crucible and the seed plate fixed to the crucible lid [2]. The system is enclosed and heated up to temperatures from 1800° - 2600° C, the point at which SiC begins to sublime, or vaporize.

The primary phases of growth are: (1) molecular disengagement of silicon carbide source material, (2) diffusive transport, and (3) seed crystallization. At high temperature,
Silicon carbide precursor material dissociates into compounds of various ratios of silicon and carbon ($\text{Si}_x\text{C}_y$), for example, $\text{Si}_3\text{C}$, or $\text{SiC}_3$. The dissociation of silicon carbide into these various compounds can be described as [17]:

$$\text{SiC}(\text{solid}) \rightleftharpoons \text{Si}(\text{gas}) + \text{C}(\text{solid})$$

$$2\text{SiC}(\text{solid}) \rightleftharpoons \text{SiC}_2(\text{gas}) + \text{Si}(\text{gas})$$

$$\text{SiC}(\text{solid}) + \text{Si}(\text{gas}) \rightleftharpoons \text{Si}_2\text{C}(\text{gas})$$

where, a double arrow ($\rightleftharpoons$) indicates that the reaction occurs in both directions. The phase is indicated by: solid (s), gas (g), or vapor (v). The reactions of charge dissociation in the SiC powder can also be represented as:

$$\text{SiC}(\text{solid}) \rightarrow \frac{1}{2}\text{Si}_2\text{C}(\text{vapor}) + \frac{1}{2}\text{C}(\text{vapor})$$

$$\text{SiC}(\text{solid}) \rightarrow \frac{1}{2}\text{SiC}_2(\text{vapor}) + \frac{1}{2}\text{Si}(\text{vapor})$$

The surface interactions occurring in the crucible proceed as:

$$\text{C}(\text{solid}) + 2\text{Si}(\text{vapor}) \rightarrow \text{Si}_2\text{C}(\text{vapor})$$

$$2\text{C}(\text{solid}) + \text{Si}(\text{vapor}) \rightarrow \text{SiC}_2(\text{vapor})$$

The graphite (C) in the crucible wall creates a catalytic reaction with the evaporated $\text{Si}_x\text{C}_y$, forming $\text{Si}_2\text{C}$ and $\text{SiC}_2$. A temperature differential is applied such that the SiC powder is slightly hotter than the seed, thus facilitating transport from source to seed where supersaturation (condensation) occurs, resulting in highly controllable crystal growth [2,3]. A more detailed schematic of seeded sublimation growth is shown below:
Seeded sublimation growth uses an induction furnace, usually operating at an optimum frequency of \(~10\ kHz\) [3]. Within the main chamber, the "hot zone" consists of rigid graphite insulation enclosing a high-density graphite crucible and susceptor [2]. The physical mechanism by which the "hot zone" and the SiC source material is brought to elevated temperatures within the induction furnace can be described by Faraday's Law of electromagnetic induction, that a time varying electric current through the "RF coil" induces a magnetic field within the SiC charge, which, in turn induces eddy currents that generate heat on the susceptor.

### 2.2.2 Epitaxy

The MESFET structure utilizes the Schottky barrier formed by the junction of a metal gate structure with a N-type semiconductor layer, as opposed to the MOSFET structure, which is based on the metal-oxide-semiconductor capacitor. A moderately doped buffer layer serves to isolate the conductive channel layer from the bulk substrate. This type of structure is achieved by the use of epi-layers, which are multiple layers of
SiC of varying doping densities, which are homoepitaxially deposited. One example of the epi-layered MESFET structure has been fabricated by Yim, et. al. at Seoul National University, in the figure below:

![Cross-sectional schematic of the MESFET fabricated at Seoul National University](image)

**Figure 10:** Cross-sectional schematic of the MESFET fabricated at Seoul National University [23].

Chemical vapor deposition (CVD) is the only commercial application of SiC epitaxial growth currently [3]. Additional epitaxial processes include metallorganic CVD (MOCVD) and molecular beam epitaxy (MBE) which are currently used to fabricate SiC MEMS microstructures. CVD commonly employs the hot-wall reactor, in place of the cold-wall reactor. In CVD, the gases pass over a heated graphite susceptor, which is coated by SiC or tantalum carbide (TAC), as in the illustration below:

![Schematic of the Chemical Vapor Deposition reactor for SiC](image)

**Figure 11:** Schematic of the Chemical Vapor Deposition reactor for SiC [18].
The vapors pass over the heated susceptor at high-velocity streamline flow. The gases include silane (SiH₄) and hydrocarbon precursors, and a hydrogen carrier gas (H₂) [3]. The hydrocarbon is normally propane (C₃H₈). As the SiH₄ and C₃H₈ pass over the susceptor, the heated gases diffuse through the boundary layer to allow growth on the substrate and on the reactor walls [3].

The CVD system is thermodynamically complex, consisting of the following procedure: (1) mass transfer of the precursors from the reactor inlet to the wafer proximity, (2) reaction of precursors to form a range of gaseous species, (3) transfer of these species to the surface of the wafer, (4) release of SiC through surface reactions, (5) desorption of the vapor by-products, (6) transfer of the by-products away from the wafer surface, and (7) release of by-products from outlet of reactor [19]. Mass transport and chemical equilibrium of gaseous species within the reactor is governed by the law of mass action. Consider the dissociation of silane into daughter molecules:

$$\text{SiH}_4(g) \rightleftharpoons \text{SiH}_2(g) + \text{H}(g)$$

According to the law of mass action:

$$K_p(T) = \frac{p_{\text{SiH}_2}p_H}{p_{\text{SiH}_4}}$$

where p is the partial pressure of the gaseous species and $K_p(T)$ is the reaction equilibrium constant. The total pressure of the reactor $P$ is the sum of the partial pressures:

$$P = p_{\text{SiH}_4} + p_{\text{SiH}_2} + p_H + p_{H_2}$$

A more complete scenario of the reactions occurring in the reactor would be:

$$\text{SiH}_4(g) \rightleftharpoons \text{SiH}_2(g) + \text{H}(g)$$

$$\text{SiH}_4(g) + \text{SiH}_2(g) \rightleftharpoons \text{Si}_2\text{H}_6(g)$$
\[ Si_2H_6(g) \rightleftharpoons HSiH_3(g) + H_2(g) \]

In order to find the equilibrium partial pressures of this system, we must find the equilibrium constant for each reaction [19].

In certain applications of SiC, such as deposition of SiC on Si substrates for MEMS applications, the high growth temperatures in excess of 1000° C utilized in CVD are impractical. These high temperatures tend to introduce defects such as high tensile stress and lattice defects in the SiC films due to the variations in thermal expansion coefficients and lattice constants between two dissimilar semiconductors such as SiC and Si. One alternative to CVD, which is useful at lower temperatures (700° - 1000° C), is metallorganic chemical vapor deposition (MOCVD) [20].

MOCVD is a variation of thermal chemical vapor deposition, or vapor-phase epitaxy (VPE), which uses heat to provide the required energy to sustain the chemical reactions [19]. MOCVD systems may be similar to the one pictured below, taken from Matsunami's treatment of SiC epitaxial growth in step-controlled epitaxial growth of SiC: high-quality homoepitaxy [21].

![Figure 12: Reactor for Chemical Vapor Deposition of SiC, similar to that used in MOCVD [21].](image-url)
This technique uses metallorganic compounds such as methyl- and ethyl- compounds. For example, GaAs crystal growth uses TMG, trimethylgallium [Ga(CH₃)₃] as the Gallium source and arsine (AsH₃) as the group V hydride source.

D.C. Lim at Sungkyunkwan University, South Korea, has reported the preparation of high-quality SiC thin films using diethyl methylsilane (C₅H₁₄Si) as the antecedent gas [20]. Reasonably structured 3C-SiC layers were grown by increasing the deposition temperature to 900° C and 10⁻⁵ Torr for MEMS microstructures. These conditions yielded rectangular crystal formations of 3C-SiC film on the substrate with average sizes of 100 nm and RMS surface roughness of 32 nm [20].

2.3 Crystallographic Structure

The SiC unit cell consists of a tetragonal structure with a Si atom within four C atoms. In this way, the crystal structures of silicon carbide are comprised of equivalent masses of Si and C atoms. Two carbon atoms are separated by 3.08 Å, and a C and Si atoms is separated by roughly 1.89 Å, as shown in Figure 1.

![Figure 1: The silicon carbide unit cell, showing the distance between nearest neighbor atoms [3].](image)

The stacking order of the SiC crystal bilayer plane determines whether the Si-C bonding is cubic (zincblende) or hexagonal (wurtzite) in structure. Wurtzite bonds are
reflected images with respect to adjacent atoms, and cubic bonds are rotated 60°. The hexagonal wurzite crystal plane is comprised by a C atom, amidst vertices formed by Si atoms. This plane can be considered as "A", and the orientation of the upper plane can be configured differently as in Figure 2.

For example, if the stacking is ABCABC..., the 3C-SiC (or β-SiC), or purely cubic structure is constructed as in Figure 2a. The SiC polytypes contain varying degrees of these basic cubic or hexagonal structures. 4H- and 6H-SiC have more complex stacking sequences (Figures 2b and 2c). 6H-SiC is two-thirds zincblende while 4H- contains equivalent ratios of zincblende and wurzite. The 4H- and 6H-SiC are the most researched for MESFET devices [3].

![Figure 14: The molecular structures of β-SiC (a), 4H- (b), and 6H- (c) [3].](image)

2.4 Electrical and Material Properties

SiC has over 260 variations or "polytypes". A polytype, such as 3C-, 4H-, or 6H- signifies the order of Si-C sheets contained in a unit cell, along with its distinct crystallographic structure, with C denoting "cubic", and H denoting "hexagonal". The
aforementioned polytypes are the most relevant in microelectronics, with 4H-SiC being the main subject of this paper [6]. 4H-SiC is the most common available on the market, and is particularly well suited to device applications due to its high breakdown electric field strength (20 x 10^5 V/cm), low dielectric constant (9.7), and high thermal conductivity (5 W/cm*K) [7]. Table 1 presents a comparison of pertinent electrical parameters between Si, GaAs, and the SiC polytypes [1].

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>3C-SiC</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Band Gap (eV)</td>
<td>1.12</td>
<td>1.43</td>
<td>2.2</td>
<td>3.26</td>
<td>3.03</td>
</tr>
<tr>
<td>Max. Operating Temp. (K)</td>
<td>600</td>
<td>760</td>
<td>1200</td>
<td>1600</td>
<td>1580</td>
</tr>
<tr>
<td>Melting Point (K)</td>
<td>1690</td>
<td>1510</td>
<td>&gt;2100</td>
<td>&gt;2100</td>
<td>&gt;2100</td>
</tr>
<tr>
<td>Electron Mobility, $\mu_n$ (cm^2/Vs)</td>
<td>1350</td>
<td>8500</td>
<td>900</td>
<td>720</td>
<td>370</td>
</tr>
<tr>
<td>Breakdown Voltage, $V_b$ (x 10^6 V/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>3</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Thermal Conductivity $\sigma_T$ (W/cm)</td>
<td>1.5</td>
<td>0.46</td>
<td>4.9</td>
<td>4.9</td>
<td>4.9</td>
</tr>
<tr>
<td>Saturation Drift Velocity, $V_{sat}$ (x 10^7 cm/s)</td>
<td>1</td>
<td>1</td>
<td>2.5</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Dielectric Constant, $\epsilon_r$</td>
<td>11.8</td>
<td>12.8</td>
<td>9.66</td>
<td>9.7</td>
<td>9.7</td>
</tr>
</tbody>
</table>

Table 3: Important electrical properties between Si, GaAs, and the main SiC polytypes [1].

From Table 1, it is evident that 4H-SiC has the widest bandgap of 3.26 eV as compared to 1.12 eV for Si. This is important when we consider the formation of an
ohmic contact. As will be seen later, the larger energy bandgap leads to a larger Schottky barrier with higher contact resistance in electrical contacts. This contributes to one of the potential problems in fabrication of SiC MOS devices. 4H-SiC also has a very high operating temperature and melting point, which is important when considering device survivability in high-temperature conditions such as space. 4H-SiC also has a high electron mobility (720 cm$^2$/Vs), high breakdown voltage ($3 \times 10^6$ V/cm), and high thermal conductivity (4.9 W/cm).

These material properties are determined by the electronic band structure of the atoms within the crystal. In the next section, the crystallographic properties of SiC are described in detail, in order to form a basis for understanding the material defects of SiC.

2.5 Energy Band Structure

When fabricating devices such as MESFETs in SiC, it is pertinent to know the material properties of SiC, such as those mentioned in Table 2.1. These material properties are determined by the electronic band structure of the atoms within the crystal. In a semiconductor crystal, where there is long-range order of atoms, their preliminary quantized energy levels will split into a band of discrete energy levels. The possible states that the electron can occupy are determined by the time-independent Schrodinger Equation [8]:

$$-\frac{\hbar^2}{2m} \frac{d^2\psi(x)}{dx^2} + V(x)\psi(x) = E\psi(x)$$

In Fundamentals of Solid State Engineering, by Manijeh Razeghi, this author outlines a method to plot the energy band structure of semiconductors algebraically, in which the following two equations are derived as solutions to the time-independent
The left-hand sides of these equations are functions of \( \gamma \) only, and the right-hand sides are functions of the energy \( E \), with the variable \( \xi \) being related to the energy \( E \) by:

\[
\begin{align*}
\alpha & = \left\{ 
\begin{array}{l}
j\alpha_- = j \frac{\sqrt{2m(U_0 - E)}}{\hbar^2} = j\alpha_0\sqrt{1 - \xi}, \quad 0 < E < U_0 \\
\alpha_+ = \frac{\sqrt{2m(E - U_0)}}{\hbar^2} = \alpha_0\sqrt{\xi - 1}, \quad U_0 < E \\
\beta = \frac{2mE}{\hbar^2} = \alpha_0\sqrt{\xi}
\end{array}
\right.
\end{align*}
\]

A solution in \( \xi \) of the above set of equations allows the determination of the energy values. Because of the cosine on the LHS, at the equilibrium interatomic distance, real (allowed) values for \( \gamma \), are achieved only with values of \( f(\xi) \) for which \(-1 < f(\xi) < 1\), with each value of \( f(\xi) \) corresponding to two opposite values of \( \gamma \). Allowable energy bands are continuous in \( \xi \) (or \( E \)), for real values of \( \gamma \). \( f(\xi) \) fails to produce energy states for \( \xi < -1 \) or \( \xi > +1 \). These "energy band gaps" are not allowed, and thus the energy is discretized [9].

Depending on the face of the unit cell within the lattice structure (\( \Gamma, M, K, L \)), the wave-vector (\( k \)) will determine these forbidden energy levels. A band gap energy of 3.263 eV was obtained by Choyke for the indirect \( \Gamma \) to M band of 4H-silicon carbide.
Research done by Ng, Vasilaska, and Schroder at University of Arizona, 2011 have determined the band structure of hexagonal 4H-SiC, shown in Figure 3 below [10]:

![Band Structure of 4H-SiC](image)

Figure 15: The electronic band structure of 4H-SiC, showing the energy level (eV) versus wavevector (k) (as determined by Ng, Vasilaska, and Schroder at University of Arizona, 2011) [10].

By developing cognizance of the physics of electrons in solids, the defects of SiC materials can be better understood.

2.6 Defects

Defects in SiC can hinder device performance by degrading such properties as bandgap energy, breakdown voltage, and yield. It is crucial to determine the causes of these defects in order to identify which methods of fabrication will minimize them. This section exposes some of the major defects of SiC. For example, the ion implantation doping process may establish a large concentration of vacancies or interstitial bonds. Post-implant annealing may cause precipitates to be formed due to the decrease in solubility [11].
These can be subdivided into point defects, two-dimensional defects (dislocations), and 3-dimensional defects. Examples of point defects include vacancies (e.g. the deficiency of an atom at its structural site), or interstitial bonds (e.g. the occurrence of an atom in a site that should be unoccupied). Antisites also occur in diatomic compounds, like SiC, when atoms of different type exchange places. Impurity atoms can also be observed in substitutional or interstitial positions in the crystal when atoms of different species are present.

Linear defects include possible dislocations in the lattice structure around which some of the atoms are misaligned. The may include “edge” dislocations, “screw” dislocations, or both [12].

![Figure 16](image)

Figure 16: For a dislocated edge, the Burgers vector is perpendicular to the dislocation line [12].

Edge or screw dislocations result in deformations of planes of atoms. Crystal structures are bent around edges and can result in helical paths being formed around dislocation lines, in the case of the screw defect.

Degenerate formations such as stacking faults are common among planar defects. Stacking faults are the main cause of atomic layers that have been shifted out of sequence, and these have been responsible for a loss of power in silicon carbide-based
diodes. The faults act as recombination centers for charge carriers, resulting in a decrease in carrier lifetime [13].

Perhaps the most significant defect exclusive to SiC are microtubes (pinhole defects). Micropipes may occur as a hollow core in the center of several screw dislocations bunched together to form a collective screw dislocation. Micropipes are essentially a hollow void penetrating vertically through the wafer’s entire thickness, inevitably causing failure to any device placed on top of it. Particularly disturbing for high-power devices due to their large-area, the added area increases the probability of placing your device on a micropipe.

As discussed, defects such as point defects, line defects, planar defects, or complex microtubes can cause degradation of device performance or even failure. In the design and fabrication of SiC MOS and MESFET technology, it is crucial to find ways to minimize these defects. This can be achieved during the crystal growth from a melt or even during epitaxial growth. Since at this point, zero defect SiC is both rare and expensive, SiC MESFET devices can utilize fabrication techniques which maximize performance. In this paper, some of these techniques will be outlined.
CHAPTER 3: SILICON CARBIDE MESFET DEVICE FABRICATION THEORY

The processes utilized in the fabrication of the SiC MESFET are similar to those of Si FET's, with minor differences. SiC is much harder to work with than veteran semiconductor materials such as Si, GaAs, and InP, and there is not a wealth of knowledge of SiC processing techniques in industry and academia. Current SiC processes are not mature. It is an area of research and development which requires much more work before SiC power and RF devices can compete economically with Si.

The general processes involved in the fabrication of the SiC MESFET include crystal growth, chemical vapor deposition (CVD), etching & cleaning, oxidation, photolithography, doping, annealing, and characterization. Simulation of certain processes such as doping must be performed to determine optimum conditions such as ion dose, ion energy, and annealing time.

The theoretical aspect of SiC MESFET fabrication will be discussed in addition to the practical fabrication procedures.

3.1 Fabrication Processes

It is necessary to describe the underlying theory behind the fabrication processes in order to understand the physics involved. Though not all of the processes described here will be used in this particular experiment, it is important to portray a broad scenario. This will allow the readers to more fully understand the fabrication of this device and compare the trade-offs between different processes.
3.1.1 Thin Film Deposition

Deposition of silicon dioxide (SiO$_2$) is used to form a sacrificial barrier above the source and drain regions in the MESFET prior to ion implantation. SiO$_2$ is also used for isolation between the source, gate, and drain structures. SiO$_2$ is commonly grown using thermal oxidation or deposited using plasma vapor deposition (sputtering). Often times, metal layers are needed to form the source, gate, and drain ohmic contacts. As such, sputtering is usually used to deposit metal alloy thin films such as nickel (Ni) or indium-tin oxide (ITO).

3.1.1.1 Thermal Oxidation

Thermal oxidation of SiC grows the SiO$_2$ on the SiC, whereas the sputtering method deposits the SiO$_2$ from a silica glass target. The mechanism of thermal oxidation of SiC is approximately equal to that of Si, this is because the density of Si atoms in SiC is roughly the same as in Si (46%) [22,23]. For example, to grow 1000 Å of SiO$_2$ on SiC, 460 Å of SiC are consumed. The oxidation of SiC can be described as a three-step process. First, the SiC is oxidized by the reaction of an oxygen atom bonding with a SiC molecule. A Si-O-C species is created by the O$_2$ insertion, which subsequently splits into a CO molecule and a Si atom with a dangling bond. Second, diffusion of the CO occurs through the oxide and reacts with O$_2$ to produce CO$_2$. Third, SiO$_2$ is produced by Si atoms interacting with O$_2$ atoms at the SiC surface during initial oxidation or by diffusing through the oxide to the SiC/oxide interface. These three processes can be described by the following chemical reactions [22]:

$$SiC + O \rightarrow CO + Si$$
\[ CO + O \rightarrow CO_2 \]
\[ Si + 2O \rightarrow SiO_2 \]

3.1.1.2 Sputtering

Physical Vapor Deposition (PVD), also known as "sputtering" is where accelerated gas ions sputter particles from a sputter target in a low-pressure plasma chamber. A radio-frequency (RF) magnetron accelerates the plasma toward the source material. Atoms within the source material will be knocked loose, or "sputtered", if the plasma energy is sufficiently strong, usually approximately 5 eV, or four times the molecular bond potential of the target.

Argon is the most common gas utilized in sputtering due to its highly unreactive nature. Its eight valence electrons create stability and resistance to bonding with the other elements. This species creates an ideal plasma for sputtering since it fails to chemically react with the majority of substrates. Other gaseous species can be mixed or "bled" into the chamber if a chemical reaction is desired with the substrate. For example, oxygen can be bled into the chamber at a ratio of 99% argon to 1% oxygen. This assists in completing the malformed bonds in SiO\(_2\) sputtering on silicon carbide to reduce the interface charge density at the SiO\(_2\)/SiC interface. The deposition rate for SiO\(_2\) is approximately 1000 Å/hr.

3.1.2 Ion Implantation

As was stated previously, the dopants of the active regions of MESFET's are introduced via ion implantation. N-type devices consist of n-type substrates with P-type...
insulative layers below conductive N-type epitaxial layers grown on them, with the top N-type layer to serve as the conducting channel. In SiC, the N-type channel layer is implanted with n-type dopants such as nitrogen or phosphorous. P-type dopants include boron and aluminum [24]. Metals such as nickel are deposited above the N$^+$ regions for source and drain ohmic contacts. Metals such as indium tin oxide (ITO) are used above the channel to serve as the Schottky gate.

Because of the extreme stability of SiC, it is not feasible to dope the crystal by thermal diffusion as is commonly done in Si processing. Instead, dopants are usually introduced via ion implantation, which offers many advantages over thermal diffusion, such as good controllability and high selectivity [25].

When the ions are implanted into the crystal, the atoms are slowed down by nuclear and electronic stopping mechanisms due to the host lattice atoms. The nuclear stopping is responsible for elastic collisions and electronic stopping is responsible for inelastic collisions [26]. The dopants enter into the crystal and settle down creating an impurity concentration that is Gaussian in nature, with the peak concentration ($N_p$) occurring at the center of the curve where $x = R_p$ (range). The standard deviation ($\sigma_p$) denotes the straggle. In the figure below, a physical cross-section of a SiC MESFET is shown with typical doping concentrations after ion implantation.
Figure 17: Concentration contours in on-axis 6H-SiC for 90 keV Al\(^+\) implanted at 7° from the wafer normal within a plane halfway from the (10-10) and (11-20) family of planes [3].

![Concentration contours](image)

Figure 18: Schematic cross section of an ion implantation device. The implanter can be subdivided into three parts: the Source, where the impurity gas is ionized by means of an anode and cathode; the Beamline Area, where the ions are extracted and accelerated into a mass separator; and Endstation, which contains the target chamber where the ion beam hits the wafer surface [27].

![Schematic cross section](image)

The implantation is performed by an implanter tool, shown in Figure 17. Using the ion implanter tool, the surface of the wafer is scanned electrostatically to provide superior uniformity of doping. At the microscopic level, the ionic dopants are bombarded into the crystal, and the atoms cease to move at some mean infiltration depth, denoted as the "projected range" (R\(_p\)). This range may vary from about 300 Å to 1.0 µm.

An implanted impurity profile N(x) with ionic dose (Q) per square centimeter is fundamentally characterized using a Gaussian distribution as in the equation below [17].

\[
N(x) = \frac{Q}{\sqrt{2\pi} \Delta R_p} \exp \left[ -\frac{1}{2} \left( \frac{x - R_p}{\Delta R_p} \right)^2 \right]
\]
where:

\[ Q = \text{implant dose (ions/cm}^2\text{)} \]

\[ R_p = \text{projected range (mean penetration depth)} \]

\[ \Delta R_p = \text{straggle (standard deviation of the distribution at } e^{-1/2} \times \text{peak concentration)} \]

\[ x = \text{penetration depth (cm)} \]

As mentioned previously, ion-implantation is the preferred method of introducing dopants into the active regions of devices fabricated in SiC polytypes. This is due to such factors as the high stability of SiC and controllability of ion-implantation. Ion-implantation also displays superiority over such techniques as plasma-etching for mesa isolation, which degrades device performance by increasing gate leakage current, decreasing mobility, and lowering contact resistance of the ohmic features [28].

Ion-implantation is used to introduce acceptor dopants into SiC such as Al and B, and donors such as nitrogen and phosphorous [29]. S.J. Wang at NW University in China describes the design of nitrogen implant layers on 4H-SiC p-channels by multiple ion-implantation doping. Multiple implants are used to get a uniform "box profile", which alludes to the symmetrical Gaussian profile. Wang describes the implant distribution for multiple fold ion-implantation as:

\[
\rho(x) = \sum_{i=1}^{I} \frac{\beta Q_i}{\sqrt{2\pi}\sigma_i} \exp \left[ -\frac{(x - R_{p_i})^2}{2\sigma_i^2} \right] - N_A
\]

with \( \rho(x) \) being the effective carrier concentration at a depth \( x \) from the surface of the 4H-SiC, \( \beta \) is the activation rate for nitrogen ions implanted, \( Q_i(Q_i) \) represents the ion dose for the "i-th" implant, \( \sigma_i(\sigma_i) \) is the i-th longitudinal straggle parameter, \( R_{p_i}(R_{pi}) \) is the projected range of the i-th implant, and \( N_A \) is the doping density of the p-type epilayer [18]. The
channel depth should be based upon the final implantation (corresponding to the highest energy). Figure 14 gives the energy band diagram after the 4H-SiC has received multiple ion-implants.

![Energy Band Diagram](image)

**Figure 19:** Energy band diagram of P type epilayer in 4H-SiC implanted by nitrogen [29].

For the implanted layer, the channel depth is: $a = x_a - x_{ns}$, where $x_a$ signifies the position at which $\rho(x) = N_A$.

### 3.1.3 Annealing

Silicon carbide wafers can be annealed, enabling dopant atoms to diffuse substitutionally into points within the semiconductor lattice, affecting the electrical properties of the target wafer. This is commonly done to mend the disrepair suffered due to implantation in the crystal lattice, or alter the quality of grown films. The annealing process for the small quartz tube furnace in the Microelectronic Engineering Laboratory (MEL) is as follows:

1. Set the proportional-integral-derivative (PID) controller to 200° C to allow the annealing furnace to warm up.
ii. Raise temperature to 650° C as suitable temperature to load furnace. Turn Nitrogen gas on to a flow rate of 6.1 ft³/hr.

iii. Clean the quartz rod and boat, place the wafer in the quartz boat, and remove the end-cap from the furnace. Beginning pushing quartz boat into furnace very slowly to prevent thermal shock of wafer. Pushing in boat drags air into pure N, creating turbulence. Stop wafer in center of furnace.

iv. Raise temp to 1025° C. Upon reaching desired temp, anneal wafer for 60-90 min.

v. Lower temp to 650° C.

vi. Remove wafer slowly from furnace to avoid thermal shock. Replace end-cap.

vii. Reduce temp of furnace.

3.1.4 Photolithography

Single device and integrated circuit fabrication demands submicron patterning of various appropriately doped structures on a semiconductor substrate, together with a series of metallizations. A photolithographic process is required for the entire fabrication procedure to allow for each of these regions. In the case of integrated circuits, this is followed by one or more levels of interconnection patterns between them. The procedure for photolithographic patterning of SiC wafers for MESFETs is summarized below:

1. Coat with Photoresist (PR)
   i. Hard bake (150° C): Wafer is heated to 150° C to de-humidify surface and make bone-dry.
(Yellow room is kept at 60° F, 45% humidity – optimum for photolithography).

ii. Spin-Coating:

- Apply Photoresist.
- Soft bake: 120° C for 2 min.

2. Exposure to UV Light

i. Mask Align

ii. Exposure

3. Developer (CD-26):

- During ultraviolet exposure, the photoresist absorbs radiation in the exposed areas, allowing it to become soluble in the CD-26 developer solution. During development when the wafer is placed in the CD-26, the exposed areas are dissolved.

- If CD-26 is not developing PR: Try re-exposing the wafer at a longer exposure time, or increasing the intensity of the exposure.

4. Hard Bake (Polymerizes (solidifies) photoresist).

5. Coat Back Side of Wafer with PR (repeat above process without exposing to UV light or CD-26).
3.1.5 Etching and Cleaning

Etching is a process utilized to remove materials from a wafer; it can be used for either cleaning the surfaces prior to undergoing a process or for removing several hundred to thousands of angstroms with low precision. The two primary types of etching are wet etching and dry etching. In the wet etching process, a mixture of hydrogen flouride solution (HF), nitric acid (HNO₃), and C₂H₄O₂ (acetic acid) is the most common etchant solvent for semiconductors. The concentration of each solvent determines the etch rate.

By contrast, dry etching utilizes kinetic energy to remove target atoms. Plasma etching uses sputtering to remove substrate atoms with argon, knocking the target atoms loose and evaporating them after leaving the substrate. A summary of the two main etching processes are shown below:

1. Wet Chemical Etching
   i. HNA: Hydroflouric Acid + Nitric Acid + Acetic Acid. Produces isotropic etch using a redox reaction followed by a decomposition of the SiO₂ by a hydroflouric acid complexing agent.

   \[ 3Si + 4HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 8H_2O + 4NO + 3h^+ + 3e^- \]

   • Etch rate is 1 – 3 um per minute.

   ii. Silicon Dioxide: The addition of NH₄F to HF in BOE maintains a consistent etch rate by refilling the depleted flouride ions and controlling the pH value.
• Etch using Ultra-Etch Buffered HF Solution.

• Concentrated HF etches SiO₂ too rapidly for accurate process control. Buffered oxide etch (BOE) is applied for more higher-precision etching.

• 6:1 BOE will etch thermally grown oxide at approx. 2 nm/s at 25° C. Temperature can be increased to raise the etching rate.

• Clean with Acetone.

• Spin-Rinse-Dryer (SRD).

• 7:1 BHF gives about 1000 Å/min etch rate.

\[ Si + 6HF \rightarrow H_2SiF_6 + 2H_2O \]

• To avoid over-etching into substrate, try starting with lower etch rate (diluted BOE).

2. Dry Physical Etching
   i. Plasma Etching
4.1 Stopping and Range of Ions in Matter

SRIM (The Stopping and Range of Ions in Matter) is a suite of open-source software, originally developed by J.P. Biersack and J.F. Zeigler in 1983 which simulates the quantum mechanics of particle reactions. Assuming all moving atoms as "ions", and all target atoms as "atoms", SRIM utilizes statistical algorithms to efficiently calculate the gaps between collisions [34].

TRIM (the Transport of Ions in Matter) is the most involved program included with SRIM. TRIM will accept intricate compound targets and calculate both the final two-dimensional and three-dimensional distributions of the ions as well as all associated ionic energy loss, including atomic deterioration and phonon propagation. These programs are user-friendly and produce data as well as graphical plots [34].

4.1.1 Stopping and Range Tables

To produce a Gaussian impurity profile, the range and straggle parameters are required. These can be extracted from SRIM, and the version being used is SRIM-2008.04. The process can be summarized as follows:

1. Start SRIM and choose: Stopping and Range Tables. Select the ion using the periodic table of elements. Click "PT" and a periodic table is displayed. The ion can be selected from here. We are using Nitrogen for this simulation.
Figure 20: The periodic table of the elements [34].

2. To choose the target material, select "Compound Dictionary". Silicon carbide can be selected from the alphabetic list of materials as shown. Click "Add to Target".

Figure 21: The compound dictionary [34].

Both the atomic density and stoichiometry of the compound are programmed in TRIM. The density can be adjusted to be more accurate for 4H-SiC, which is 3.21 g/cm³.
3. Calculate Table. Adjust the implantation energy from 10 keV to 160 keV to give a sufficient range of energies for the simulation. Change the density of the target compound. Verify that the stopping power units are in MeV / (mg/cm²). The screen should now appear as shown. Select "Calculate Table."

![Image of ion stopping and range tables]

Figure 22: The ion stopping and range tables [34].

4. View and save range table. The following text file will be output, and can be saved. All pertinent information is output by TRIM including the ion energy, electronic and nuclear stopping energies, range, and straggle parameters. The ion stopping and range table can be seen in Appendix A.

4.1.2 Ion Distribution and Quick Calculation of Damage

TRIM can be used to calculate the damage to the target and plot the ion distribution. This process uses the following procedure:
1. From the main menu, choose "Trim Calculation." On the TRIM setup window, choose "Ion Distribution and Quick Calculation of Damage" under the "Damage" drop down menu. Also choose "Ion Distribution with Recoils Projected on Y-Plane" under the "Basic Plots" drop down menu. For "Ion Data" choose Nitrogen, similarly to how the ion is selected for the Stopping and Range Tables. The TRIM calculation is performed using 60 keV implant energy.

2. Input Target Data (Layer 1). Up to eight layers of dissimilar target materials can be input in the "Target Data" section. Again, choose Compound Dictionary, select SiO$_2$, and click Add to Current Layer. The window should appear as shown:

![Figure 23: The compound dictionary [34].](image)

SiO$_2$ is used as the sacrificial barrier through which the Nitrogen ions are implanted to reduce damage to the SiC target. In this simulation, the density of SiO$_2$ is left as 2.32 g/cm$^3$. The width of the layer is input as 500 Å.
3. Input Target Data (Layer 2). Select Add New Layer. The new layer appears as Layer 2. Again, choose Compound Dictionary, and select silicon carbide, then Add to Current Layer. Again, changing the density of SiC to 3.21 g/cm$^3$, and the width of layer 2 to 2550 Å, the screen should now appear as shown. The plotting window depth is automatically calculated by summing the total width of all layers. The total number of ions is set as 1000. This amount would not consume too much time, and the author has stated there is less than 10% error in the calculation for 1000 ions.

![TRIM Setup Window](image)

Figure 24: The TRIM setup window showing two layer target [34].

4. Save Input and Run TRIM. Select Save Input and Run TRIM. The following window appears. In the XY Longitudinal window, the damage to the lattice has been calculated and graphically represented in a plot of depth versus y-axis. Also,
the SiO$_2$ / SiC interface can be seen, with most of the damage occurring in the SiC. Also, a close-up of the XY Longitudinal window is shown.

![TRIM output window](image)

Figure 25: The TRIM output window [34].

5. Open and Save the Ion / Recoil Distribution Data File. The data file is shown below. This includes data for the depth and concentration of the ions in the target. These values can be plotted in any spread sheet software. Also, TRIM can output the graphical plots. The ion / recoil distribution data file can be seen in Appendix B.

6. Generate the Ion Distribution Plot. In the TRIM Plots window, there are two sections: Collision Plots and Distributions. Under Distributions, check the box under Plot. The following plot is displayed:
The above plot displays the ion concentration versus depth (Å). The units of the concentration are in \((\text{atoms/cm}^3) / (\text{atoms/cm}^2)\). Therefore, to obtain the ion concentration in units of ions/cm\(^3\), the y-axis data must be multiplied by the dose (ions/cm\(^2\)). The above plot is rough and doesn't provide very much detail. In order to better visualize the distribution, the TRIM data must be input using spread-sheet software. Matlab is chosen for this simulation for more controllability over mathematics and graphical display.

**4.2 Simulation Using Matlab**

**4.2.1 Statement of the Problem**

The purpose of this simulation is to determine the optimum ion-implantation parameters such as implant energy (keV), ion dose (ions/cm\(^2\)), annealing temperature (°C), and annealing time (seconds). This is achieved by plotting the impurity profile of
nitrogen into 4H-SiC for varying implant energies, given a desired junction depth. As an example, a plot of the impurity profile of nitrogen in 4H-SiC in units of ion concentration (ions/cm$^3$) versus depth (microns) is illustrated below, as published by Wang, et. al [29]. The profile of a multiple-fold ion-implantation can be achieved, as labeled by: "Effective Doping."

Figure 27: Simulation of nitrogen concentration of four-fold ion implantation in 4H-SiC [29].

4.2.2 Analytical Calculations

The Gaussian model is used to plot the impurity concentration after ion implantation. The process parameters are taken from experimental data. The Gaussian equation for pre-annealing is taken from Ghandi [26], and the equation for post-annealing is taken from Chattopadhyay [24]. The ion concentration as a function of depth ($x_j$) is shown below:

$$N(x) = \frac{Q}{\sqrt{2\pi}\sigma_p} \exp \left[ -\frac{(x_j - R_p)^2}{2\sigma_p^2} \right] \quad (1)$$

$$N(x, t) = \frac{Q}{\sqrt{2\pi}\sqrt{(\sigma^2 + 2Dt)}} \exp \left[ -\frac{(x_j - R_p')^2}{2\sigma_p'^2 + 4Dt} \right] \quad (2)$$
where the process parameters are indicated as:

- \( Q \) = implant dose per unit area (cm\(^2\))
- \( R_p \) = projected range (cm)
- \( \sigma_p \) = lateral straggle (cm)
- \( D \) = diffusivity (cm\(^2\)s\(^{-1}\))
- \( t \) = diffusion time (annealing) (s)
- \( R'_p = R_p + k\Delta x_j, \Delta x_j = \) change in junction depth due to post-annealing [24].

The diffusivity is a value that is specific to the dopant species in SiC, and this is calculated as:

\[
D = D_0 \exp \left( -\frac{E_A}{kT} \right)
\]

where

- \( D_0 \) = diffusion coefficient (cm\(^2\)s\(^{-1}\))
- \( E_A \) = activation energy (eV)
- \( k \) = Boltzmann constant \((8.6173 \times 10^{-5} \text{ eVK}^{-1})\)
- \( T \) = temperature (K)

Initially, the diffusivity of nitrogen in 4H-SiC is calculated using the empirically-determined diffusion coefficient value. For nitrogen, this value is found to be \( 5.0 \times 10^{-12} \) cm\(^2\)s\(^{-1}\), for temperatures between 1800\(^\circ\) C - 2450\(^\circ\) C [35]. For nitrogen donors, the activation energy \((E_A)\) has been determined to be 54.5 meV \( \pm \) 0.3 meV [24]. Substituting into the diffusivity equation,
\[
D = (5.0 \times 10^{-12} \text{cm}^{-2} \text{s}^{-1}) \exp \left( -\frac{0.0545 \text{eV}}{(8.6173 \times 10^{-5} \text{eV} \text{K}^{-1})(1600 \text{°C})} \right)
\]

\[
D = 7.42 \times 10^{-12} \text{cm}^2 \text{s}^{-1}
\]

However, this value conflicts with the experimentally determined value as published by J.G. Phelps, et al., where it is given as: \(7.2 \times 10^{-15} \text{ cm}^{-2} \text{s}^{-1}\) [36]. This value is used for more accuracy.

Process parameters from several case studies are used to simulate the ion implantation impurity profile, such as the Phelps, Wang, Tucker, and Moscatelli processes. Each case study provides a different combination of the ion implantation process parameters, including implant energy (keV), ion dose (Q) (cm\(^{-2}\)), annealing time (t) (seconds), annealing temperature (T) (celsius), and diffusivity (D) (cm\(^{-2}\)s\(^{-1}\)).

Prior to plotting the impurity concentrations, it is necessary to determine the thickness of the N-type epi-layer to be used as the channel layer where the source and drain will be implanted. In this way, the junction depth can be determined, where enough space will be left between the implants and the P-type epi-layer. A thin "sacrificial barrier" layer of SiO\(_2\) of approximately 500 Å will be deposited on the N-type epi-layer to help protect the host lattice from some of the damage occurring during implantation. In this way, the simulation allows the doping to be controlled. The specific parameters of implant energy, ion dose, and annealing time will be determined to create the optimum junction depth and peak concentration.

The thermal oxide growth at this point was determined to be 350 Å (the amount of SiC consumed by SiO\(_2\) was \(0.46(350 \text{ Å}) = 161 \text{ Å SiC}\)). Thus, the remaining epi was \(3224 - 161 \approx 3063 \text{ Å} \approx 3050 \text{ Å}\). The desired junction depth after annealing should be well
within 3000 Å. Approximately 2250 Å should be sufficient. The impurity concentrations are plotted in Matlab, showing the boundary of the SiO₂/SiC interface at 500 Å.

4.2.3 Output / Discussion

The impurity distribution is plotted at 20 keV, 30 keV, 40 keV, and 60 keV using the process parameters as stated by J.G. Phelps in "Field enhanced diffusion of nitrogen and boron in 4H-silicon carbide." In each plot, the process parameters are stated, the SiO₂ / SiC interface is plotted on the x-axis, and the background concentration in the n-type epi-layer is plotted on the y-axis. The calculation occurs in matlab as illustrated in the following figure:

![Impurity profile simulation flow chart](image)

Figure 28) Impurity profile simulation flow chart.
Figure 29: Simulation of the impurity concentration of nitrogen ions (cm$^{-3}$) in 4H-SiC versus depth (cm $\times$ 10$^{-5}$) for 20 keV. The plots show the impurity concentration prior to annealing (blue), and after annealing (magenta).
Figure 30: Simulation of the impurity concentration of nitrogen ions (cm\(^{-3}\)) in 4H-SiC versus depth (cm \(\times 10^{-5}\)) for 30 keV. The plots show the impurity concentration prior to annealing (blue), and after annealing (magenta).
Figure 31: Simulation of the impurity concentration of nitrogen ions (cm$^{-3}$) in 4H-SiC versus depth (cm $\times 10^{-5}$) for 40 keV. The plots show the impurity concentration prior to annealing (blue), and after annealing (magenta).
Figure 32: Simulation of the impurity concentration of nitrogen ions (cm$^{-3}$) in 4H-SiC versus depth (cm $\times 10^{-5}$) for 70 keV. The plots show the impurity concentration prior to annealing (blue), and after annealing (magenta).

Table 4: Summary of ion implantation parameters used in the simulation of the Phelps Model, including implantation energy (keV), ion dose (cm$^{-2}$), annealing temperature (°C), annealing time (minutes), peak concentration in SiC wafer (cm$^{-3}$), depth of implant ($x_j$ (Å)), thickness of SiO$_2$ layer (Å), and total depth of implant after annealing ($\Sigma x_j$ (Å)).
The plot with the highest peak concentration (\(N_p \approx 2.0 \times 10^{20} \text{ cm}^{-3}\)), as well as the desired junction depth of \(x_j \approx 2250 \text{ Å}\) is the simulation based on the Phelps process parameters with 70 keV implant energy, \(2.0 \times 10^{15} \text{ cm}^{-2}\) ion dose, and 10 minutes annealing time at 1600° celsius. In this plot, the peak concentration (\(N_p\)) occurs slightly to the right of the boundary of the \(\text{SiO}_2 / \text{SiC}\) interface, and this is also desired, since the metal (Ni) ohmic contact will make intimate contact at this boundary, where close to the maximum number of charge carriers will be available during biasing.

The Gaussian plots generated in Matlab represent idealized symmetrical impurity profile curves showing the ion concentration versus depth. It is later determined that Gaussian distributions are inaccurate. Impurity profiles based on experimental data are asymmetrical, skewed, and exhibit tails. A more accurate approach is to use the Pearson type-IV distribution function. These functions account for such crystalline properties as channeling, profile skewness, and kurtosis (flatness). Skewness describes the asymmetry of the implanted profile, and kurtosis describes the flatness at the peak of the profile. The basic parameters used in the Pearson type-IV distribution are known as moments. These moments include the (i) average projected range \(R_p\), (ii) straggle (standard deviation) \(\Delta R_p\), (iii), skewness \(\gamma\), and (iv) kurtosis \(\beta\) [37]. These parameters are used in the Pearson type-IV distribution functions as shown below:

\[
f(x) = K \left[ 1 + \left( \frac{x - R_p}{A} - \frac{n}{r} \right)^2 \right]^{-m} \exp \left[ -n \tan^{-1} \left( \frac{x - R_p}{A} - \frac{n}{r} \right)^2 \right]
\]

The parameters \(n, r, A,\) and \(m\) are correlated by:

\[
r = -(2 + 1/b_2)
\]

\[
n = - \frac{rb_1}{\sqrt{4b_0b_2 - b_1^2}}
\]
\[ m = -\frac{1}{2b_2} \]
\[ A = \frac{mrb_1}{n} \]

where

\[ b_1 = -\gamma \Delta R_p (\beta + 3)C \]
\[ b_0 = -\gamma \Delta R_p^2 (4\beta - 3\gamma^2)C \]
\[ b_2 = -(2\beta - 3\gamma^2 - 6)C \]
\[ C = \frac{1}{2(5\beta - 6\gamma^2 - 9)} \]

For nitrogen implanted in 4H-silicon carbide, the following parameters have been experimentally determined [25]:

\[ R_p = 4.00E^{0.819} \]
\[ \Delta R_p = 2.91E^{0.570} + 0.206 \times \frac{10^{4.6}}{E^2} \]
\[ \gamma = 2.40 - 0.85 \ln E \]
\[ \beta = 1.70\beta_0 \]

where

\[ \beta_0 = \frac{[39\gamma^2 + 48 + 6(\gamma^2 + 4)^{1.5}]}{(32 - \gamma^2)} \]

To plot the dopant impurity profile of nitrogen in 4H-silicon carbide using the Pearson type-IV distribution function, the data for ion concentration (atoms / cm\(^3\))/(atoms / cm\(^2\)) versus depth (angstroms) is taken from the "ion distribution and quick calculation of damage" using TRIM, as discussed earlier in section 5.1, "Stopping and Range of Ions."
in Matter." Impurity profiles using implant energies of 60 keV, 70 keV, 80 keV, 90 keV, and 100 keV are plotted using the same Phelps process parameters. It is also determined that diffusion of impurities in SiC is very slow for temperatures up to 2300° C, and even negligible below 1800° C, therefore furnace annealing at 1600° C cannot be reliable when predicting the post-annealing profile [37]. Additionally, the TRIM calculation cannot simulate the profile for post-annealing. Considering these observations, the furnace annealing must be replaced by the rapid thermal annealing (RTA) process at 1700° C for a short time (30 seconds). Annealing for 30 seconds will ensure that the impurities do not diffuse into the SiC too drastically, and using this high temperature will ensure that the dangling bonds and damage to the crystal is repaired sufficiently to improve biasing.

In order to generate the plots below, the TRIM data was plotted using Matlab, and fitness curves of even-order were used to connect the data points in order to predict the junction depths.
Figure 33: Simulation of the impurity concentration of nitrogen ions (cm\(^{-3}\)) in 4H-SiC versus depth (cm \(\times 10^{-5}\)) for 80 keV using the Pearson type-IV distribution. The plot uses an eighth-order fitness curve to connect the data points and predict the junction depth.
Figure 34: Simulation of the impurity concentration of nitrogen ions (cm$^{-3}$) in 4H-SiC versus depth (cm $\times 10^{-5}$) for 90 keV using the Pearson type-IV distribution. The plot uses an eighth-order fitness curve to connect the data points and predict the junction depth.
Figure 35: Simulation of the impurity concentration of nitrogen ions (cm\(^{-3}\)) in 4H-SiC versus depth (cm \(\times 10^{-5}\)) for 100 keV using the Pearson type-IV distribution. The plot uses an eighth-order fitness curve to connect the data points and predict the junction depth.

<table>
<thead>
<tr>
<th>Energy (keV)</th>
<th>Dose (cm(^{-2}))</th>
<th>Temp (°C)</th>
<th>Time (sec)</th>
<th>(N_P) (cm(^{-3}))</th>
<th>(x_j) (Å)</th>
<th>(SiO_2) (Å)</th>
<th>(\Sigma x_j) (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>2.0(\times 10^{15})</td>
<td>1700</td>
<td>30</td>
<td>2.6(\times 10^{20})</td>
<td>2200</td>
<td>500</td>
<td>1700</td>
</tr>
<tr>
<td>80</td>
<td>2.0(\times 10^{15})</td>
<td>1700</td>
<td>30</td>
<td>2.4(\times 10^{20})</td>
<td>2350</td>
<td>500</td>
<td>1850</td>
</tr>
<tr>
<td>90</td>
<td>2.0(\times 10^{15})</td>
<td>1700</td>
<td>30</td>
<td>2.3(\times 10^{20})</td>
<td>2600</td>
<td>500</td>
<td>2100</td>
</tr>
<tr>
<td>100</td>
<td>2.0(\times 10^{15})</td>
<td>1700</td>
<td>30</td>
<td>2.2(\times 10^{20})</td>
<td>2700</td>
<td>500</td>
<td>2200</td>
</tr>
</tbody>
</table>

Table 5: Summary of process parameters used in the Pearson Type-IV Distribution, including implantation energy (keV), ion dose (cm\(^{-2}\)), annealing temperature (°C), annealing time (minutes), peak concentration in SiC wafer (cm\(^{-3}\)), depth of implant \(x_j\) (Å), thickness of SiO\(_2\) layer (Å), and total depth of implant after annealing \(\Sigma x_j\) (Å).
Figure 36: Simulation of the impurity concentration of nitrogen ions (cm$^{-3}$) in high-purity semi-insulating 4H-SiC versus depth (cm $\times 10^{-5}$) for 80 keV using the Pearson type-IV distribution. The plot uses a tenth-order fitness curve to connect the data points and predict the junction depth.
CHAPTER 5: FABRICATION PROCESS

5.1 Schematic Steps

Prior to the fabrication of the SiC MESFET, a process is outlined. This helps to expose possible problems during the procedure and determine their solutions. The entire procedure is outlined graphically in a set of "Schematic Steps," as shown below:

Figure 37: The process begins by growing 4000 Å of SiO$_2$ on the Si-face.

Figure 38: Photoresist is applied.
Figure 39: The pattern is made in the photoresist using Mask #2: source and drain doping oxide etch.

Figure 40: Windows are etched in the oxide for the source and drain doping.

Figure 41: The photoresist is cleaned off and the wafer is rinsed.
Figure 42: 500 Å of SiO$_2$ are deposited.

Figure 43: The source and drain are doped n-type using ion implantation.

Figure 44: AlN is deposited and wafer is heated using rapid thermal annealing.
Figure 45: Photoresist is applied.

Figure 46: The pattern is made in the photoresist using Mask #0: mesa RIE oxide etch.

Figure 47: Oxide is etched prior to isolation implant.
Figure 48: The device isolation walls are implanted using p-type ions.

Figure 49: The photoresist is cleaned off and the wafer is rinsed.

Figure 50: The AlN and SiO$_2$ are etched, leaving 4000Å of oxide.
Figure 51: SiO₂ is deposited to increase the thickness of the oxide.

Figure 52: Photoresist is applied.

Figure 53: A pattern is made in the photoresist using Mask #4: Source and Drain Contact Oxide Etch.
Figure 54: The oxide is etched prior to the source and drain contact deposition.

Figure 55: The photoresist is cleaned off and the wafer is rinsed.

Figure 56: A nickel layer is deposited.
Figure 57: Photoresist is applied.

Figure 58: A pattern is made in the photoresist using Mask #5: Source, Drain, and Pads Metallization Etch.

Figure 59: The nickel is etched off, leaving the source and drain contact pads.
Figure 60: The photoresist is cleaned off and the wafer is rinsed.

Figure 61: Photoresist is applied.

Figure 62: A pattern is made in the photoresist using Mask #5: Gate Contact Etch.
Figure 63: The oxide is etched prior to deposition of gate contact.

Figure 64: The photoresist is cleaned off and the wafer is rinsed.

Figure 65: A layer of PMGI is applied prior to a lift-off process.
Figure 66: A layer of photoresist is applied.

Figure 67: A pattern is made in the photoresist using Mask #7: Gate Contact ITO Lift-Off.

Figure 68: A layer of indium tin oxide (ITO) is deposited.
The ITO is removed using the lift-off process, leaving the gate contact.

The wafer is complete after the deposition of the gate contact pad and lift-off. Characterization would occur both during and after the fabrication process. The fabrication of 4H-SiC MOS capacitors are used to characterize the silicon dioxide layer. The actual recipes used during the fabrication process of the 4H-SiC MOS capacitors are contained in the following two sections.

5.2 Fabrication of 4H-SiC MOS Capacitors

The MOS devices are made onto Si-face 4H SiC wafers that the SiO₂ is first grown onto Si-face 4H-SiC substrate by wet thermal oxide process, followed by annealing at 1175° C for two hours under N₂ atmosphere. The ohmic contacts are made by sputter deposition of Ni metal onto backside (C-face) of the 4H-SiC/SiO₂ sample [7,8]. In order to carry out photolithography, the polydimethylglutarimide (PMGI) is coated onto 4H SiC/SiO₂ by spin coating, followed by prebaking at 170° C. The photoresist (S1813) is then spun onto PMGI as a bilayer (PR), followed by soft-baking at 115° C. The SiC/SiO₂/PMGI/photoresist sample is irradiated by UV light using the mask aligner (Karl-SussMA65) for eleven seconds, followed by immediate dipping into
developer (CD-26) and left for fifty five seconds. After cleaning the sample with deionized water, the optical microscope confirms clear cut mesa structure patterns on the wafer. An each structure has an area of \(6.25 \text{ Å}^2 \approx 10^{-2} \text{ cm}^2\) on 3 inch wafer. After baking, the sample is shortly cleaned with RF plasma using Ar as a sputter gas. The Ni dots are deposited by sputtering using our well-established growth recipe. The CD-26 developer and acetone are employed to remove PR on the SiO\(_2\) to have Ni(back contact)/SiC Si-face/SiO\(_2\)/Ni MOS capacitor structure. Finally, the samples are post-oxidized that eliminates surface charge and reduces density of surface states of the samples to some extent. The current-voltage measurements on several MOS devices are carried out by using the HP4140E pico-ammeter at room temperature.
CHAPTER 6: ELECTRICAL CHARACTERIZATIONS

6.1 Electrical Characterizations: Theory

6.1.1 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a form of scanning probe microscopy capable of resolutions on the order of fractions of a nanometer. The particular AFM used in this experiment is the Dimension FastScan from Bruker Nano Surfaces. The AFM consists of a cantilever with a narrow tip (probe) at its end, usually made of silicon (Si) or silicon nitride (Si₃N₄) with a tip radius of curvature on the order of nanometers. When in proximity of a specimen surface, forces between the tip and the specimen lead to a deflection of the cantilever obeying Hooke's law. The vibration is measured using a laser spot reflected from the top surface of the cantilever into an array of photodiodes. A scanning electron micrograph of an AFM probe is shown below [39]:

![Scanning electron micrograph of AFM probe tip.](image)

6.1.2 Semiconductor Parametric Analysis

6.1.2.1 Current-Voltage (I-V) Measurement

Under certain conditions, the properties of insulators can be changed by introducing a sudden large current. Such a condition creates a weakened path through the
material that results in permanent molecular or physical changes in the insulator which causes conduction through the dielectric. The maximum voltage difference that can be applied across the material is called the “breakdown voltage” of the device. The breakdown voltage highly depends on physical properties of the device such as geometry of the conductive parts, including sharp edges or points in the device structure. When this occurs, the dielectric quickly breaks down causing a short circuit, which results in dissipated energy [41].

6.1.2.2 Capacitance-Voltage (C-V) Measurement

Likewise, Capacitance-Voltage profiling (C-V profiling) specifies valuable information about the semiconductors, their interface, and their depletion region. Not only they are used to determine the oxide thickness, oxide charges, contamination from mobile ions, and interface trap density in wafer processes, they also play important roles after the fabrication process is performed. Therefore, after fully fabricating the desired device, C-V measurements are performed to characterize the threshold voltages, analyze the doping profiles of the semiconductor device, and model the device performance. Although, the C-V testing method is one of the best methods for characterizing the semiconductor parameters in MOSFET or MOS capacitor, such methods can also be used to test and characterize other types of semiconductor devices including bipolar junction transistors, JFETs, III-V compound devices, photodiodes, and carbon nanotubes. A C-V measurement technique is performed by varying the applied voltage at a metal-semiconductor junction, a MOSFET, or a p-n junction and plotting the corresponding capacitance as a function of voltage.
Depending on the charge distribution, different operation regions can be classified. When a negative voltage \((V < 0)\) is applied to the top metal plate, the valence-band edge \(E_V\) bends upward near the surface towards the Fermi Level. Ideally, no current flows in the capacitor, and the Fermi Level stays flat. Since the majority carrier density depends exponentially on the difference in energy \((E_F - E_V)\), this causes an accumulation of majority carrier holes near the surface of the semiconductor. This is known as the “accumulation case.” When the applied voltage becomes greater than the flat-band voltage \((V_A > V_{FB})\), an “insulator-like” layer is created which is empty of conducting electrons and holes, but contains ionized donors or traps. This layer is called the “depletion layer.” When the applied voltage is increased still \((V_A >> V_{FB})\), the bands bend further down so that the intrinsic level \((E_i)\) crosses the Fermi Level \((E_F)\), increasing the minority carrier (electron) density at the surface greater than the holes, therefore inverting the p-type semiconductor to n-type. This is the “inversion case.” [14]. When the voltage is varied at the junction, the width of this region varies as well. The relation between the applied voltage and the width of the depletion region describes the doping profile and other internal characteristics of the device [42].

### 6.2 Electrical Characterizations

AFM is utilized to characterize the field-oxide SiO\(_2\) layer prior to oxidation of SiC MESFET product wafers. This is in order to determine the best process method for high-breakdown voltage oxide, which is determined by the interface trap density charges \(D_{it}\). Figure 71 portrays an image of the starting wafer, prior to processing, to show the differences between the Si- and C-face of the wafers. The surface of the C-face shows
higher surface roughness with various trenches, while the Si-face is smoother. RMS (root mean square) surface roughness values of 1.63 and 0.08 nm for C-face and Si-face samples, respectively. Since no trenches appear on the Si-face, we can infer that the C-face is more mechanically delicate than the Si-face of 4H-SiC.

Figure 72 displays the AFM scan of SiO$_2$ grown by wet thermal oxidation on the C-face where nano-structured features with uniform surface roughness of 0.3 nm. This could be due to C agglomeration, where the growth of SiO$_2$ emerges as bonding between C and Si in the SiC breaks down at high temperature by impact of H. The nanorod-like structures may be due to C clusters formed by the agglomeration of C on the C-face of 4H-SiC.

After totally etching the SiO$_2$ layer on the SiC substrate, dips, voids, and protrusions are found to be inhomogeneously propagated on the surface of the C-face 4H-SiC substrate. It could be due to C clusters such as SiO$_x$C$_y$ or a $\alpha$-CH at the interface of SiC and SiO$_2$. The RMS surface roughness of the substrate is in the range of 8.76 nm caused by pyramid-like structures, after etching SiO$_2$ layer.
Figure 71: (a) AFM image of 4H-SiC raw C-face substrate. (b) AFM image of 4H-SiC raw Si-face substrate [38].
Figure 72: SiO$_2$ grown on C-face 4H SiC by wet thermal oxidation [38].

Figure 73: AFM image of 4H-SiC C-face substrate after etching wet thermally grown SiO$_2$ [38].
Figure 74 portrays an AFM image of the SiO$_2$ layer grown by wet thermal oxide on the C-face 4H-SiC selectively etched using Ultra-Etch buffered HF, up to the bottom of the SiO$_2$ layer or surface of SiC. One can clearly find interface states between SiO$_2$ and SiC substrate that could be due to formation of either SiO$_x$C$_y$ or a $\alpha$-CH cluster or both, as marked by the arrow.

Figure 74: Selectively etched SiO$_2$, which is grown on C-face 4H SiC by wet thermal oxidation [38].

Figure 75: Selectively etched SiO$_2$, which is grown on Si-face 4H SiC by sputtering [38].
The wide surface scan of SiO$_2$ layer grown on the C-face 4H-SiC by sputtering is shown in Figure 75. The SiO$_2$ layer is largely featureless with some pit-like structures with RMS roughness of 2.5 nm. Table 6 includes a summary of these measurements.

<table>
<thead>
<tr>
<th>Figure</th>
<th>Process</th>
<th>Face</th>
<th>RMS Surface Roughness (nm)</th>
<th>Depth of Feature (nm)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>71</td>
<td>Raw SiC Wafer</td>
<td>C</td>
<td>1.63</td>
<td>4.0-9.0</td>
<td>C-face is more mechanically delicate than Si-face</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Si</td>
<td>0.08</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>Wet Thermal SiO$_2$</td>
<td>C</td>
<td>0.3</td>
<td>-</td>
<td>C agglomeration</td>
</tr>
<tr>
<td>73</td>
<td>Etching of SiO$_2$</td>
<td>C</td>
<td>8.76</td>
<td>2</td>
<td>Formation of C clusters such as SiO$_x$C$_y$ or $\alpha$-CH (HF resistant)</td>
</tr>
<tr>
<td>74</td>
<td>Selective Etching of SiO$_2$</td>
<td>Si</td>
<td>8.73</td>
<td>-</td>
<td>Etching on Si-face is slower than on C-face</td>
</tr>
<tr>
<td>75</td>
<td>Sputtered SiO$_2$</td>
<td>C</td>
<td>3.2</td>
<td>-</td>
<td>Rough pits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Si</td>
<td>2.5</td>
<td>-</td>
<td>Growth rate is slower</td>
</tr>
</tbody>
</table>

Table 6: Surface roughness measurements of 4H-SiC wafers at different stages of processing.

Throughout the performance of this experiment, I-V and C-V measurements were obtained and plotted. Meanwhile, there was a path of improvement by repeating the experiment and enhancing the steps taken each time. Below, there are two I-V graphs obtained which indicate the breakdown voltage was highly close to applied voltage. Such a result is not desired since it indicates that the oxide layer is not performing as an
insulator. This could be due to the formation of silicon oxycarbides (SiC₇Oₓ) during SiO₂ sputter deposition. This in combination with possible pinhole defects caused by use of low-quality HF solution has contributed to a high interface-state density (Dᵢₜ) causing leakage current in the oxide. Processing of subsequent wafers may include O₂ bleeding in argon gas mixture during sputtering and post-oxidation nitrogen annealing to bond with the excess O₂ atoms forming NO.

Figure 76: Typical I-V Plot for wafer # FW1332-35. Low breakdown voltage indicates high leakage currents in oxide caused by the high interface trap density, which subsequently are remedied by addition of O₂ to sputtering gas mixture and nitrogen annealing.
Figure 77: Typical I-V Plot for wafer # FJ0923-35. Low breakdown voltage indicates high leakage currents were still present in the oxide. Nitrogen annealing was performed at 1131°C for 5 hours. O₂ bleeding was not performed during SiO₂ sputtering.
Figure 78: I-V Plot for wafer #KA0305-36, showing a higher breakdown voltage of 27.90 V. This was due to increased temperature and time during nitridation for 1175° C for 2.5 hours.

The results of the I-V measurements are shown below in Table 7. The wafer with the higher breakdown voltage coincided with an increase in the thermal oxidation and annealing temperatures to 1175° C.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$V_{\text{start}}$</th>
<th>$V_{\text{stop}}$</th>
<th>$V_{\text{bd}}$</th>
<th>$T_{\text{ox}}$</th>
<th>$O_2$</th>
<th>Anneal</th>
<th>Recipe</th>
</tr>
</thead>
<tbody>
<tr>
<td>FW1332-35</td>
<td>-10</td>
<td>+10</td>
<td>&lt;1V</td>
<td>850 Å</td>
<td>No</td>
<td>1025° C, 1.5 hrs, 6.1 ft³/hr N</td>
<td>RF 250 W, 1 hr, .025 mTorr</td>
</tr>
<tr>
<td>FJ0923-35</td>
<td>-10</td>
<td>+10</td>
<td>&lt;1V</td>
<td>250-420 Å</td>
<td>No</td>
<td>1131° C, 5 hrs, 6.1 ft³/hr N</td>
<td>Dry ox: 2.5 hrs, 1100° C</td>
</tr>
<tr>
<td>KA0305-36</td>
<td>-1</td>
<td>+30</td>
<td>27.9 V</td>
<td>350-400 Å</td>
<td>No</td>
<td>1175° C, 2.5 hrs, 4 slpm N</td>
<td>Wet ox: 2.5 hrs, 1100° C</td>
</tr>
</tbody>
</table>

Table 7: Summary of results of I-V measurements, showing breakdown voltage ($V_{\text{bd}}$).
Typical capacitance voltage (CV) curves of the Si-face 4H-SiC/SiO₂ wet and sputter oxide MOS capacitors recorded at high frequency (1 MHz) are shown in Figures 76a and b, respectively. A shift in flat-band voltage is shown from the accumulation, depletion to inversion positions while sweeping from positive to negative applied voltage. The oxide capacitance ($C_{ox}$), flat-band capacitance ($C_{fb}$) and flat-band voltage ($V_{fb}$) are marked, as shown in Figure 76a. The experimental $C_{ox}$ is fairly coinciding with the theoretical value ($\varepsilon_{ox}\varepsilon_0/d$), where $\varepsilon_{ox}$ is the dielectric constant of SiO₂. The thickness ($d$) of wet and sputtered SiO₂ layers employed for MOS capacitors is found to be in the range of 800-1400 Å.

![Figure 79](image)

Figure 79: (a) CV curve of MOS capacitor fabricated on the Si-face 4H-SiC substrate by wet thermal oxide. (b) CV curve of MOS capacitor fabricated on the Si-face 4H-SiC substrate by sputter oxide.

Interface trapped charges ($Q_{it}$), are due to structural defects in the semiconductor-SiO₂ interface which can be oxidation-induced, impurity, or radiation-based. Interface
trap density ($D_{it}$) is given in units of N/A, or the (number of these charges per unit area) • (electron charge), or number/cm$^2$•eV. The interface trap density ($D_{it}$) at flat-band potential, where the surface potential is zero, can be determined by considering the fixed charge ($Q_f$), determined by comparing the flatband voltage shift of an experimental C-V curve with a theoretical curve and measuring the voltage shift. $Q_f$ can be expressed as a function of the flatband voltage by [44]:

$$Q_f = (\phi_{MS} - V_{FB})C_{ox}$$

Also, $N_f$ can be described as $N_f = \frac{Q_f}{q}$, and since $D_{it} = \frac{N_f}{A}$, $D_{it}$ can be expressed as [44]:

$$D_{it} = \frac{(\phi_{ms} - V_{fb})C_{ox}}{qA}$$

where $\phi_{ms} = \phi_m - \phi_s$, $\phi_m$ is the metal work function (5.1 eV), and $\phi_s$ is the work function of 4H-SiC semiconductor. $\phi_{ms}$ is found to be [44]:

$$\phi_{ms} = \phi_m - (\chi + kT \ln \left( \frac{N_C}{N_D} \right))$$

where $\chi$ is the electron affinity of the semiconductor (4.05 eV), $N_C (3.25 \times 10^{15}T^{3/2})$ is the effective density of states in the conduction band, and $N_d (10^{18})$ is the donor concentration. Using these equations, the $D_{it}$ at flat-band voltages of wet and sputtered oxides are found to be $-3.174 \times 10^{12}$ and $-2.893 \times 10^{12}$ cm$^{-2}$eV$^{-1}$, respectively. Also, as shown in Table 8, the comparison of $D_{it}$ for the sputtered oxide versus the wet thermal oxidation suggests the SiO$_2$ grown by sputtering is of higher quality.

We can plot the variation of $D_{it}$ with trap energy level for MOS capacitors by considering the total surface charge of a MOS capacitor: $Q_s = Q_f + Q_{it}$, where $Q_f$ is the fixed oxide charge, which is constant. Thus, surface charge depends on the interface trap
charge: $Q_s = Q_o + C$. Assuming the $D_n$ to be constant at the middle of the band gap, we can express $D_{it}$ as a function of surface potential as [45]:

$$D_{it}(\psi_s) = \frac{Q_{it}}{\psi_s q^2}$$

The $D_n$ can be related to trap energy level with respect to surface potential. The trap level ($E_c - E_t$), which varies from conduction band edge to middle of band gap in $n$-type 4H-SiC, can be calculated using the relation [44]:

$$E_c - E_t = \frac{E_g}{2} - q\psi_s - \phi_B$$

where $\phi_B = E_f - E_i$ is the potential barrier in 4H-SiC, and $E_f$ is the Fermi level. $E_i$ is the intrinsic level, or mid-gap of 4H-SiC. Rearranging the above equation, we get:

$$\psi_s = \frac{-[E_c - E_t] - \frac{E_g}{2} + \phi_B}{q}$$

plugging into $D_{it}(\psi_s)$, we get:

$$D_{it}(\psi_s) = \frac{-Q_{it}}{[E_c - E_t] - \frac{E_g}{2} + \phi_B}$$

Figure 80: Variation of $D_n$ with trap energy level for MOS capacitors (wet oxide (blue), and sputtered oxide (black)).
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Wet thermal oxide</th>
<th>Sputtered Oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flat-band voltage ($V_{fb}$)</td>
<td>13.4 V</td>
<td>-</td>
</tr>
<tr>
<td>Capacitance at $V_{fb}$ ($C_{fb}$)</td>
<td>2.536 nF</td>
<td>-</td>
</tr>
<tr>
<td>Oxide Capacitance ($C_{ox}$)</td>
<td>2.538 nF</td>
<td>-</td>
</tr>
<tr>
<td>Interface Trap Density ($D_{it}$)</td>
<td>$-3.174 \times 10^{12}$ cm$^{-2}$eV$^{-1}$</td>
<td>$-2.893 \times 10^{12}$ cm$^{-2}$eV$^{-1}$</td>
</tr>
</tbody>
</table>

Table 8: Summary of results of I-V measurements, showing breakdown voltage ($V_{bd}$).

The estimated interface trap density ($D_{it}$) decreases in the range from $10^{17}$ to $10^{12}$ cm$^{-2}$eV$^{-1}$ with increasing trap energy ($E_c - E_i$) level from the conduction band edge (0.57 eV) to mid-gap (1.13 eV) of 4H-SiC in the MOS capacitor for wet thermal and sputtered processes, are shown in Figure 80. The curves seem to be in exponential decay. The density of interface traps at band edge of our samples is higher than reported value of $10^{13}$ cm$^{-2}$eV$^{-1}$ [43].
CHAPTER 7: CONCLUSION

The fabrication processes of a 4H-SiC MESFET are described, including simulations to predict the junction depth during ion-implantation doping processes. The optimal parameters for ion implantation are found to be 80 keV for the conductive substrate (KH0384-20) and 90 keV for the high purity semi-insulating substrate (HG0863-19). In the early stages of fabrication, several experiments are conducted in order to characterize the SiO₂ used in the field-oxide for isolation between the source, gate, drain, and between devices. SiC MOS capacitors are fabricated using the Ni/SiO₂/4H-SiC structure in order to characterize the quality of the SiO₂.

The SiO₂ thin films grown by both wet thermal oxide and sputtering process are in good quality but latter exhibits better quality. The growth of SiO₂ is stronger on the Si-face 4H-SiC than on the C-face substrates irrespective of growth techniques. The C clusters form at the interface of SiC/SiO₂ for the growth of wet thermal oxide process, but such activities are not observed in the sputtered SiO₂ growth. In this project, a new model for the formation of secondary phase of α-CH nano-islands with help of AFM analysis is established. The HF etches off SiO₂ layers grown by wet thermal process faster than that of layers grown by sputtering. The HF also etches off SiO₂ films grown on the C-face 4H-SiC substrates faster than SiO₂ grown on the Si-face 4H-SiC substrates. Higher growth rate of SiO₂ layers on the C-face 4H-SiC indicates that the C clusters maybe acting as nucleation centers for the growth of nano-structured SiO₂. The interface trap density (Dₙ) of 4H-SiC Si-face/SiO₂ is in the range of 10¹² cm⁻² eV⁻¹ at flat-band voltage.
REFERENCES


[40] Franceschinis, Surface Profilometry as a Tool to Measure Thin Film Stress, A Practical Approach.


# APPENDIX A: Stopping and Range Table: Nitrogen in Silicon Carbide

---

Calculation using SRIM-2006  
SRIM version --> SRIM-2008.04  
Calc. date --> March 13, 2015

---

Disk File Name = SRIM Outputs\Nitrogen in No. 590 Silicon Carbide

Ion = Nitrogen [7], Mass = 14.003 amu

Target Density = 3.2100E+00 g/cm³ = 9.6419E+22 atoms/cm³

<table>
<thead>
<tr>
<th>Atom</th>
<th>Atom Numb</th>
<th>Atomic Percent</th>
<th>Mass Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>6</td>
<td>050.00</td>
<td>028.95</td>
</tr>
<tr>
<td>Si</td>
<td>14</td>
<td>050.00</td>
<td>70.05</td>
</tr>
</tbody>
</table>

Bragg Correction = 0.00%

Stopping Units = MeV / (mg/cm²)

See bottom of Table for other Stopping units

<table>
<thead>
<tr>
<th>Ion Energy</th>
<th>dE/dx Elec</th>
<th>dE/dx Nuclear</th>
<th>Projected Range</th>
<th>Longitudinal Straggling</th>
<th>Lateral Straggling</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.00 keV</td>
<td>5.663E-01</td>
<td>6.967E-01</td>
<td>192 A</td>
<td>94 A</td>
<td>70 A</td>
</tr>
<tr>
<td>11.00 keV</td>
<td>5.940E-01</td>
<td>6.848E-01</td>
<td>210 A</td>
<td>101 A</td>
<td>75 A</td>
</tr>
<tr>
<td>12.00 keV</td>
<td>6.204E-01</td>
<td>6.730E-01</td>
<td>227 A</td>
<td>108 A</td>
<td>80 A</td>
</tr>
<tr>
<td>13.00 keV</td>
<td>6.457E-01</td>
<td>6.615E-01</td>
<td>245 A</td>
<td>115 A</td>
<td>85 A</td>
</tr>
<tr>
<td>14.00 keV</td>
<td>6.701E-01</td>
<td>6.503E-01</td>
<td>262 A</td>
<td>121 A</td>
<td>90 A</td>
</tr>
<tr>
<td>15.00 keV</td>
<td>6.936E-01</td>
<td>6.394E-01</td>
<td>279 A</td>
<td>127 A</td>
<td>95 A</td>
</tr>
<tr>
<td>16.00 keV</td>
<td>7.164E-01</td>
<td>6.289E-01</td>
<td>296 A</td>
<td>133 A</td>
<td>100 A</td>
</tr>
<tr>
<td>17.00 keV</td>
<td>7.384E-01</td>
<td>6.186E-01</td>
<td>313 A</td>
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Multiply Stopping by

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APPENDIX B: Ion Distribution Data: Nitrogen in Silicon Carbide

====== N (60) into ICRU-245 SiO2+Layer 2 =======
SRIM-2008.04

ION and final RECOIL ATOM Distributions
See SRIM Outputs\TDATA.txt for calculation details

Recoil/Damage Calculations made with Kinchin-Pease Estimates

There are NO RECOILS unless a full TRIM calculation is made.

See file : SRIM Outputs\TDATA.txt for details of calculation
Ion    =  N   Energy = 60 keV

TARGET MATERIAL

Layer 1: ICRU-245 SiO2
Layer Width = 5.0E+02 A   Layer # 1- Density = 6.975E22 atoms/cm3 = 2.32 g/cm3
Layer # 1- O = 66.6 Atomic Percent = 53.2 Mass Percent
Layer # 1- Si = 33.3 Atomic Percent = 46.7 Mass Percent

Layer 2: No. 590 Silicon Carbide
Layer Width = 3.0E+03 A   Layer # 2- Density = 9.641E22 atoms/cm3 = 3.21 g/cm3
Layer # 2- Si = 50   Atomic Percent = 70.0 Mass Percent
Layer # 2- C = 50   Atomic Percent = 29.9 Mass Percent

Total Ions calculated =1000.00
Ion Average Range = 117.4E+01 A   Straggling = 317.3E+00 A
Ion Lateral Range = 295.3E+00 A   Straggling = 371.3E+00 A
Ion Radial Range = 447.1E+00 A   Straggling = 231.8E+00 A

Transmitted Ions =; Backscattered Ions =1
(These are not included in Skewne- and Kurtosis below.)

Range Skewne- = -000.5850 &=\frac{-(X-Rp)^3}{[N*Straggle^3]}\]
Range Kurtosis = 003.0548 &=\frac{-(X-Rp)^4}{[N*Straggle^4]}\]
Statistical definitions above are those used in VLSI implant modelling.

Table Distribution Units are >>> (Atoms/cm3) / (Atoms/cm2) <<<
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%Program which plots the Gaussian impurity profile of an ion implanted 
%4H-SiC MESFET doped with nitrogen. 
%Phelps Model 
clear all; 
close all; 

%=================Pre-Annealing=======================% 
%implant dose cm^-2 
Q1=8E14;  
Q2=2E15;  
epi_4=6E18; %cm^-3

%N in SiC range parameter (changed to cm) 
R1_20=365E-8; %20 keV  
R1_25=407E-8; %25 keV  
R1_30=533E-8; %30 keV  
R1_35=614E-8;  
R1_40=693E-8;  
R1_60=996E-8;  
R1_70=1143E-8;  
R1_80=1289E-8;  

%N in SiC straggle parameter (changed to cm) 
s1_20=119E-8; %20 keV  
s1_25=141E-8; %25 keV  
s1_30=162E-8; %30 keV  
s1_35=182E-8;  
s1_40=201E-8;  
s1_60=267E-8;  
s1_70=297E-8;  
s1_80=324E-8;  

%Peak concentration, N in SiC 
A1_20=Q1/((2*pi).^(0.5)*s1_20); %20 keV  
A1_25=Q1/((2*pi).^(0.5)*s1_25); %25 keV  
A1_30=Q1/((2*pi).^(0.5)*s1_30); %30 keV  
A1_35=Q1/((2*pi).^(0.5)*s1_35); 
A1_40=Q1/((2*pi).^(0.5)*s1_40); 
A1_60=Q2/((2*pi).^(0.5)*s1_60); 
A1_70=Q2/((2*pi).^(0.5)*s1_70); 
A1_80=Q2/((2*pi).^(0.5)*s1_80); 

%=================Post-Annealing=======================% 
Ea=54.5E-3; %Activation Energy of Nitrogen in 4H-SiC (eV)  
k=8.61733E-5; %boltzmann constant eV/K  
T5=1600; %temperature in deg C  
D0=5E-12; %diffusion coefficient of 4H-SiC cm^2s^-1  
t_a=600; %annealing time (sec)  
D1=D0.*exp(-(Ea)./(k*(T5+273))); %diffusivity parameter  
D1=7.2e-15; %diffusivity parameter 
%Peak concentration, N in SiC 
A2_20=Q1/((2*pi).^(0.5)*((s1_20.^2)+2*D1*t_a).^(0.5));
A2_25=Q1/((2*pi).^(0.5)*((s1_25.^2)+2*D1*t_a).^(0.5));
A2_30=Q1/((2*pi).^(0.5)*((s1_30.^2)+2*D1*t_a).^(0.5));
A2_35=Q1/((2*pi).^(0.5)*((s1_35.^2)+2*D1*t_a).^(0.5));
A2_40=Q1/((2*pi).^(0.5)*((s1_40.^2)+2*D1*t_a).^(0.5));
A2_60=Q2/((2*pi).^(0.5)*((s1_60.^2)+2*D1*t_a).^(0.5));
A2_70=Q2/((2*pi).^(0.5)*((s1_70.^2)+2*D1*t_a).^(0.5));
A2_80=Q2/((2*pi).^(0.5)*((s1_80.^2)+2*D1*t_a).^(0.5));

%Plot Doping profile for 20 keV at 1600 C
x0=0:0.0001e-4:5e-4;
for i=1:length(x0);
B1_20(:,i)=(x0(i)-R1_20)./(2.^(0.5)*s1_20); %20 keV
N1_20(:,i)=A1_20*exp(-B1_20(:,i).^2); %20 keV
end

for j=1:length(x0);
B2_20(:,j)=(x0(j)-R1_20)./(2.^(0.5)*((s1_20.^2)+2*D1*t_a).^(0.5));
N2_20(:,j)=A2_20*exp(-B2_20(:,j).^2);
end

q=semilogy(x0,N1_20,'b-');
hold on;
r=semilogy(x0,N2_20,'m-');
hold on;
x1=[0.000005,0.000005];
y1=[1e17,1e21];
plot(x1,y1,'--r','Linewidth',1)
hold on;
x11=[0,0.35e-4];
y11=[6e18,6e18];
plot(x11,y11,'--m','Linewidth',2)
title('gaussian Impurity Profile of N in 4H-SiC: 20 keV');
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Pre-Annealing','Post-Annealing','SiO2/SiC Interface','N+ Conc. 6e18');
grid on;
set(q,'Linewidth',2);
set(r,'Linewidth',2);
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0 0.35e-4 1e17 1e21]);

%Plot Doping profile for 30 keV
x0=0:0.0001e-4:5e-4;
for i=1:length(x0);
B1_30(:,i)=(x0(i)-R1_30)./(2.^(0.5)*s1_30); %30 keV
N1_30(:,i)=A1_30*exp(-B1_30(:,i).^2); %30 keV
end

for j=1:length(x0);
B2_30(:,j)=(x0(j)-R1_30)./(2.^(0.5)*((s1_30.^2)+2*D1*t_a).^(0.5));
N2_30(:,j)=A2_30*exp(-B2_30(:,j).^2);
end

figure
w=semilogy(x0,N1_30,'b-');
% Plot Doping profile for 40 keV
x0=0:0.0001e-4:5e-4;
for i=1:length(x0);
    B1_40(:,i)=(x0(i)-R1_40)./(2.^(0.5)*s1_40);
    N1_40(:,i)=A1_40*exp(-B1_40(:,i).^2);
end

for j=1:length(x0);
    B2_40(:,j)=(x0(j)-R1_40)./(2.^(0.5)*((s1_40.^2)+2*D1*t_a).^(0.5));
    N2_40(:,j)=A2_40*exp(-B2_40(:,j).^2);
end

figure
s=semilogy(x0,N1_40,'b-');
hold on;
t=semilogy(x0,N2_40,'m-');
hold on;
x3=[0.000005,0.000005];
y3=[1e17,1e21];
plot(x2,y2,'--r','Linewidth',2)
hold on;
x13=[0,0.35e-4];
y13=[6e18,6e18];
plot(x12,y12,'--m','Linewidth',2)
title('Gaussian Impurity Profile of N in 4H-SiC: 40 keV');
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Pre-Annealing','Post-Annealing','SiO2/SiC Interface','N+ Conc. 6e18');
grid on;
set(s,'Linewidth',2);
set(t,'Linewidth',2);
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0 0.35e-4 1e17 1e21]);
% Plot Doping profile for 70 keV
x0=0:0.0001e-4:5e-4;
for i=1:length(x0);
B1_70(:,i)=(x0(i)-R1_70)./(2.^0.5*s1_70);
N1_70(:,i)=A1_70*exp(-B1_70(:,i).^2);
end

for j=1:length(x0);
B2_70(:,j)=(x0(j)-R1_70)./(2.^0.5*((s1_70.^2)+2*D1*t_a).^0.5);
N2_70(:,j)=A2_70*exp(-B2_70(:,j).^2);
end

figure
u=semilogy(x0,N1_70,'b-');
hold on;
v=semilogy(x0,N2_70,'m-');
hold on;
x5=[0.000005,0.000005];
y5=[1e17,1e21];
plot(x5,y5,'--r','Linewidth',2)
hold on;
x15=[0,0.35e-4];
y15=[6e18,6e18];
plot(x15,y15,'--m','Linewidth',2)
title('Gaussian Impurity Profile of N in 4H-SiC: 70 keV')
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Pre-Annealing','Post-Annealing','SiO2/SiC Interface','N+ Conc. 6e18');
grid on;
set(u,'Linewidth',2);
set(v,'Linewidth',2);
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0 0.35e-4 1e17 1e21]);

% Plot Doping profile for 80 keV
x0=0:0.0001e-4:5e-4;
for i=1:length(x0);
B1_80(:,i)=(x0(i)-R1_80)./(2.^0.5*s1_80);
N1_80(:,i)=A1_80*exp(-B1_80(:,i).^2);
end

for j=1:length(x0);
B2_80(:,j)=(x0(j)-R1_80)./(2.^0.5*((s1_80.^2)+2*D1*t_a).^0.5);
N2_80(:,j)=A2_80*exp(-B2_80(:,j).^2);
end

figure
u=semilogy(x0,N1_80,'b-');
hold on;
v=semilogy(x0,N2_80,'m-');
hold on;
x4=[0.000005,0.000005];
y4=[1e17,1e21];
plot(x4,y4,'--r','Linewidth',2)
hold on;
Program which plots the Pearson Type-IV impurity profile of an ion implanted 4H-SiC MESFET doped with nitrogen. Phelps Model

clear all;
close all;

Plot Doping profile for 70 keV
y8=[5.63e18 1.13e19 1.13e19 1.69e19 1.69e19 1.69e19 2.82e19 3.38e19 2.25e19 3.94e19 4.51e19 5.63e19 5.63e19 9.58e19 5.63e19 9.58e19 7.99e19 1.13e20 9.58e19 1.07e20 9.58e19 1.46e20 1.24e20 1.86e20 1.69e20 1.97e20 1.86e20 2.31e20 2.99e20 2.70e20 2.37e20 2.08e20 2.76e20 2.20e20 2.31e20 2.54e20 2.20e20 2.48e20 2.08e20 1.18e20 1.13e20 1.13e20 9.58e19 5.63e19 5.07e19 6.20e19 3.94e19 3.94e19 3.94e19 5.63e19];
v=semilogy(x8,y8,'ok');
hold on;
x12=[0.000005,0.000005];
y12=[1e17,1e21];
plot(x12,y12,'-r','Linewidth',1)
hold on;
x13=[0,0.305e-4];
y13=[6e18,6e18];
plot(x13,y13,'-m','Linewidth',2)
title('Ion Implantation Impurity Profile of N in 4H-SiC: 70 keV');
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Pre-Annealing (SRIM)','SiO2/SiC Interface','N+ Conc.: 6e18');
grid on;
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0 0.305e-4 1e17 1e21]);

%Plot Doping profile for 75 keV
figure
x9=[107e-8 178e-8 213e-8 249e-8 284e-8 355e-8 391e-8 426e-8
462e-8 497e-8 533e-8 568e-8 604e-8 639e-8 675e-8 710e-8 746e-8
781e-8 817e-8 852e-8 888e-8 923e-8 959e-8 994e-8 1030e-8 1070e-8
1100e-8 1140e-8 1170e-8 1210e-8 1240e-8 1280e-8 1310e-8 1350e-8
1380e-8 1420e-8 1460e-8 1490e-8 1530e-8 1560e-8 1600e-8 1630e-8 1670e-8
1700e-8 1740e-8 1780e-8 1810e-8 1850e-8 1880e-8 1920e-8 1950e-8
1990e-8 2020e-8 2060e-8 2090e-8 2130e-8 2170e-8 2200e-8 2270e-8 2310e-8];
y9=[5.63e18 5.63e18 1.13e19 1.69e19 5.63e18 5.63e18 5.63e18 5.63e18
1.13e19 5.63e18 1.13e19 1.69e19 5.63e18 5.63e18 5.63e18 1.69e19
2.25e19 1.13e19 5.63e18 1.13e19 2.82e19 3.38e19 5.63e19 3.38e19
5.07e19 4.51e19 4.51e19 6.20e19 6.76e19 1.18e20 5.63e19
5.63e19 1.07e20 1.24e20 1.58e20 1.30e20 1.63e20 1.69e20 1.35e20
2.20e20 1.52e20 2.42e20 2.59e20 2.20e20 2.37e20 1.92e20 2.42e20
2.76e20 2.70e20 2.65e20 1.63e20 1.46e20 1.41e20 9.01e19 1.41e20
1.18e20 5.63e19 5.63e19 3.94e19 2.82e19 1.13e19 5.63e18 5.63e18
5.63e18];
v=semilogy(x9,y9,'ok');
hold on;
x10=[0.000005,0.000005];
y10=[1e17,1e21];
plot(x10,y10,'-r','Linewidth',1);
hold on;
x11=[0,0.305e-4];
y11=[6e18,6e18];
plot(x11,y11,'--m','Linewidth',2);
title('Ion Implantation Impurity Profile of N in 4H-SiC: 75 keV');
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Pre-Annealing (SRIM)', 'SiO2/SiC Interface', 'N+ Conc.: 6e18');
grid on;
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0 0.305e-4 1e17 1e21]);

%Plot Doping profile for 80 keV
figure
x9=[ 391e-8 426e-8 462e-8 497e-8 533e-8 568e-8 604e-8 639e-8
675e-8 710e-8 746e-8 781e-8 817e-8 852e-8 888e-8 923e-8 959e-8
994e-8 1030e-8 1070e-8 1100e-8 1140e-8 1170e-8 1210e-8 1240e-8
1280e-8 1310e-8 1350e-8 1380e-8 1420e-8 1460e-8 1490e-8 1530e-8 1560e-8
1600e-8 1630e-8 1670e-8 1700e-8 1740e-8 1780e-8 1810e-8 1850e-8
1880e-8 1920e-8 1950e-8 1990e-8 2020e-8 2060e-8 2090e-8 2130e-8 2170e-8
2200e-8 2240e-8 2270e-8];
y9=[ 1.13e16 1.13e19 5.63e18 2.82e19 1.13e19 1.69e19 1.69e19
1.69e19 1.13e19 1.69e19 4.51e19 2.82e19 5.07e19 6.20e19 4.51e19
1.13e20 6.20e19 1.01e20 6.20e19 7.89e19 1.46e20 1.46e20 1.35e20
1.63e20 1.24e20 1.46e20 2.03e20 2.03e20 1.35e20
2.95e20 1.69e20 2.25e20 2.65e20 1.86e20 1.92e20 1.41e20
1.13e20 1.07e20 1.13e19 7.89e19 5.63e19 4.51e19 3.94e19 1.69e19
1.13e19 2.54e18 5.63e18];
v=semilogy(x9,y9,'ok');
hold on;
x1=[0.000005,0.000005];
y1=[1e17,1e21];
plot(x1,y1,'-k','Linewidth',2);
hold on;
x2=[0,0.305e-4];
y2=[6e18,6e18];
plot(x2,y2,'--m','Linewidth',2)
title('Pearson Type-IV Distribution of Nitrogen in 4H-SiC')
xlabel('Depth (cm)'); ylabel('Dopant Concentration (cm^-3)')
legend('Nitrogen (90 keV)', 'SiO2/SiC Interface', 'N+ Conc.: 6e18')
grid on;
set(gca, 'Linewidth', 1);
set(gca, 'XMinorTick', 'on');
axis([0.04e-4 0.305e-4 1e17 1e21]);

figure
y3=[ 6.56e18 6.56e18 6.56e18 6.56e18 1.31e19 6.56e18 6.56e18 1.97e19 2.62e19 2.62e19 6.56e18 6.56e18 3.28e19 3.28e19 3.93e19 4.59e19 1.31e19 3.93e19 5.25e19 5.25e19 7.21e19 7.21e19];
v=semilogy(x3,y3,'ok');
hold on;
x4=[0.000005, 0.000005];
y4=[1e17,1e21];
plot(x4,y4, '-k', 'Linewidth', 2);
hold on;
x5=[0,0.305e-4];
y5=[6e18,6e18];
plot(x5,y5, '-m', 'Linewidth', 2);
title('Pearson Type-IV Distribution of Nitrogen in 4H-SiC')
xlabel('Depth (cm)'); ylabel('Dopant Concentration (cm^-3)')
legend('Nitrogen (90 keV)', 'SiO2/SiC Interface', 'N+ Conc.: 6e18')
grid on;
set(gca, 'Linewidth', 1);
set(gca, 'XMinorTick', 'on');
axis([0.035e-4 0.305e-4 1e17 1e21]);

figure
y6=[ 6.56e18 6.56e18 6.56e18 6.56e18 1.31e19 6.56e18 6.56e18 1.97e19 1.97e19 1.97e19 4.59e19 6.56e18 4.59e19 3.28e19 2.62e19 2.62e19 7.87e19 2.62e19 3.28e19 2.62e19 1.31e19 5.25e19 3.28e19 4.59e19 5.25e19]
7.21e19 5.90e19 7.21e19 7.21e19 8.52e19 1.18e20 8.52e19 9.84e19 1.31e20
1.18e20 1.18e20 1.18e20 1.18e20 2.49e20 1.70e20 1.70e20 2.03e20 1.51e20
2.30e20 1.64e20 2.36e20 2.23e20 2.23e20 2.30e20 2.10e20 2.30e20 1.97e20
1.97e20 2.10e20 1.57e20 2.03e20 2.43e20 2.15e20 2.03e20 9.84e19 1.25e20
1.11e20 5.90e19 3.93e19 3.93e19 3.93e19 3.28e19 2.62e19 6.56e18;

v=semilogy(x6,y6,'ok');
hold on;
x7=[0.000005,0.000005];
y7=[1e17,1e21];
plot(x7,y7,'-k','Linewidth',2)
hold on;
x8=[0,0.305e-4];
y8=[6e18,6e18];
plot(x8,y8,'--m','Linewidth',2)
title('Pearson Type-IV Distribution of Nitrogen in 4H-SiC');
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Nitrogen (100 keV)','SiO2/SiC Interface','N+ Conc.: 6e18');
grid on;
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0.04e-4 0.305e-4 1e17 1e21]);

%Plot Doping profile for 80 keV: HG0683-19
clear all;
close all;
figure
x9=[ 391e-8 426e-8 462e-8 497e-8 533e-8 568e-8 604e-8 639e-8
675e-8 710e-8 746e-8 781e-8 817e-8 852e-8 888e-8 923e-8 959e-8
994e-8 1030e-8 1070e-8 1100e-8 1140e-8 1180e-8 1200e-8 1210e-8 1240e-8
1280e-8 1310e-8 1350e-8 1380e-8 1420e-8 1460e-8 1490e-8 1530e-8 1560e-8
2200e-8 2240e-8 2270e-8];
y9=[ 1.13e16 1.13e19 5.63e18 2.82e19 1.13e19 1.69e19 1.69e19 1.69e19
1.69e19 1.13e19 1.13e19 4.51e19 2.82e19 5.07e19 6.20e19 4.51e19 1.13e20
6.20e19 1.01e20 6.20e19 7.89e19 1.46e20 1.46e20 1.35e20 1.63e20 1.24e20
1.46e20 2.03e20 2.20e20 2.03e20 1.13e20 2.59e20 1.69e20 2.25e20 1.86e20
2.37e20 1.92e20 3.04e20 2.25e20 2.65e20 1.86e20 1.52e20 1.92e20 1.41e20
1.13e20 1.07e20 1.01e20 7.89e19 5.63e19 4.51e19 3.94e19 1.69e19
1.13e19 2.54e18 5.63e18];
v=semilogy(x9,y9,'ok');
hold on;
x1=[0.000005,0.000005];
y1=[1e17,1e21];
plot(x1,y1,'-r','Linewidth',1)
hold on;
x2=[0,0.305e-4];
y2=[7.5e18,7.5e18];
plot(x2,y2,'--m','Linewidth',2)
title('Pearson Type-IV Distribution of Nitrogen in 4H-SiC');
xlabel('Depth (cm)');ylabel('Dopant Concentration (cm^-3)');
legend('Nitrogen (80 keV)','SiO2/SiC Interface','N+ Conc.: 6e18');
grid on;
set(gca,'Linewidth',1);
set(gca,'XMinorTick','on');
axis([0.04e-4 0.305e-4 1e17 1e21]);
MICROPPOSIT® S1800® SERIES PHOTO RESISTS

MICROPPOSIT S1800 SERIES PHOTO RESISTS are positive photoresist systems engineered to satisfy the microelectronics industry's requirements for advanced IC device fabrication. The system has been engineered using a toxicologically safer alternative casting solvent to the ethylene glycol derived ether acetates. The dyed photoresist versions are recommended to minimize notching and maintain linewidth control when processing on highly reflective substrates.

MICROPPOSIT S1800 SERIES PHOTO RESISTS
FEATURE:

Product Assurance
- Lot-to-lot consistency through state-of-the-art physical, chemical and functional testing
- Filtered to 0.2 µm absolute

Coating Properties
- 1Cellosolve® Acetate and xylene free
- Striation-free coatings
- Excellent adhesion
- Excellent coating uniformity
- A variety of standard viscosities are available for single-layer processing

Exposure Properties
- Optimized for G-Line exposure
- Effective for broad band exposure
- Reflective notch and linewidth control using dyed versions

Develop Properties
- Optimized for use with the MICROPPOSIT® MF®-319 Metal-Ion-Free DEVELOPER family
- Compatible with Metal-Ion-Bearing MICROPPOSIT DEVELOPERS

Removal Property
- Residue-free photoresist removal using standard MICROPPOSIT REMOVERS

High Resolution Process Parameters
(Marker to Figure 1)

- Substrate: Film on glass
- Process: MICROPPOSIT® S1800® PHOTO RESIST
- Coating: 12.30 µA
- Softbake: 115°C for 55 sec. Hgabale
- Exposure: NB8 1525 G5, EUV/0.54 pm, .35 µm Marine
- Develop: MICROPPOSIT® MF®-319 DEVELOPER
- 15 ± 5 sec. Double Spray Paddle (DSP) @ 21°C

*Registered trademark of Union Carbide Corporation
Instructions for Use

The following instructions cover the use of MICROPPOSIT S1800 SERIES PHOTO RESISTS for all levels of microelectronic device fabrication. Exact process parameters are application and equipment dependent.

Substrate Preparation

MICROPPOSIT S1800 SERIES PHOTO RESISTS work well with the hexamethyldisilazane based MICROPPOSIT PRIMERS. Concentrated MICROPPOSIT PRIMER is recommended when vacuum vapor priming. Diluted PRIMER is recommended for liquid phase priming applications.

Coat

MICROPPOSIT S1800 SERIES PHOTO RESISTS provide uniform defect-free coatings over a wide range of film thicknesses. The film thickness versus spin speed plots displayed in Figures 1 and 2 provide the information required to properly select a MICROPPOSIT S1800 PHOTO RESIST version to meet process dependent thickness specifications. Maximum coating uniformity is typically attained between the spin speeds of 3500 rpm and 5500 rpm.

<table>
<thead>
<tr>
<th>Process Parameters (Refer to Figures 1 and 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
</tr>
<tr>
<td>Coat</td>
</tr>
<tr>
<td>Softbake</td>
</tr>
<tr>
<td>Measure</td>
</tr>
</tbody>
</table>

The dispersion curve and Cauchy equation displayed in Figure 3 describe how the refractive index of the photoresist film varies as a function of the wavelength of light incident upon the film. This information is required to program ellipsometric and other optically based photoresist measuring equipment.

<table>
<thead>
<tr>
<th>Process Parameters (Refer to Figure 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
</tr>
<tr>
<td>Coat</td>
</tr>
<tr>
<td>Softbake</td>
</tr>
<tr>
<td>Measure</td>
</tr>
</tbody>
</table>
Exposure

Proper film thickness selection is critical in order to reduce photospeed and critical dimension variability. The interference curves displayed in Figure 4 illustrate the photospeed variability as a function of film thickness. Doped versions suppress the interference effects which are more pronounced when exposing with monochromatic light sources and when using reflective substrates.

<table>
<thead>
<tr>
<th>Process Parameters (Refer to Figure 4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate: Silicon</td>
</tr>
<tr>
<td>Coat: GCA 1060® WAFERTRAC®</td>
</tr>
<tr>
<td>Softbake: 115°C/60 seconds Hotplate</td>
</tr>
<tr>
<td>Expose: GCA 8500 G-Line (0.35 NA)</td>
</tr>
<tr>
<td>Developer: MF 321/10 + 30 DSP @ 21°C</td>
</tr>
</tbody>
</table>

MICROPOSIT S1800 SERIES PHOTO RESISTS can be exposed with light sources in the spectral output range of 350 nm -450 nm. The exposure properties have been optimized for use at 436 nm. Figures 5 and 6 show the absorbance spectrums for MICROPOSIT S1813 and S1813 J2® PHOTO RESISTS.

<table>
<thead>
<tr>
<th>Process Parameters (Refer to Figures 5 and 6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate: Quartz</td>
</tr>
<tr>
<td>Coat: 12,300A</td>
</tr>
<tr>
<td>Softbake: 115°C/60 seconds Hotplate</td>
</tr>
<tr>
<td>Expose: Oriel Scanning Wedge</td>
</tr>
<tr>
<td>Measure: Hewlett Packard 8450A</td>
</tr>
<tr>
<td>Spectrophotometer</td>
</tr>
</tbody>
</table>

Table 1 summarizes the Dill parameters for each MICROPOSIT S1800 SERIES PHOTO RESIST version. Dill parameters are used in optical exposure models such as SAMPLE and PROLITH.

<table>
<thead>
<tr>
<th>MICROPOSIT S1800 SERIES PHOTO RESISTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 1. Dill Parameters</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Photoposist</th>
<th>365 nm</th>
<th>436 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A (μm²)</td>
<td>B (μm²)</td>
</tr>
<tr>
<td>S1813</td>
<td>1.07</td>
<td>0.31</td>
</tr>
<tr>
<td>S1813 D1</td>
<td>1.05</td>
<td>0.34</td>
</tr>
<tr>
<td>S1811 J2</td>
<td>1.07</td>
<td>0.49</td>
</tr>
<tr>
<td>S1818 J1</td>
<td>1.06</td>
<td>0.42</td>
</tr>
</tbody>
</table>

1 Registered Trademark of GCA, a unit of General Signal
Figure 7 displays a contrast curve for MICROPOSIT S1813 PHOTO RESIST developed with MICROPOSIT MF-321 DEVELOPER. In general, high contrast values correlate to higher angle wall profiles.

### Process Parameters (Refer to Figure 7)

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coat</td>
<td>12,300 Å</td>
</tr>
<tr>
<td>Soft bake</td>
<td>115°C/60 seconds Hotplate</td>
</tr>
<tr>
<td>Expose</td>
<td>GCA 8500 G-Line (0.35 NA)</td>
</tr>
<tr>
<td>Develop</td>
<td>MF-321/10 + 30 DSP @ 21°C</td>
</tr>
</tbody>
</table>

**DEVELOP**

MICROPOSIT S1800 SERIES PHOTO RESISTS are compatible with both Metal-Ion-Free (MIF) and Metal-Ion-Bearing (MIB) developers. A photoresist and developer system is dependent upon specific application requirements. Contact your local Shipley Technical Sales Representative for additional product information.

Figures 8 thru 10 illustrate the lithographic functionality of MICROPOSIT S1813 PHOTO RESIST using process parameters designed to maximize resolution while maintaining excellent exposure and focus latitude (refer to SEM photographs in Figure 1). The functional lithographic responses are summarized in Table 2.

### Process Parameters (Refer to Figures 8 thru 10)

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coat</td>
<td>12,300 Å</td>
</tr>
<tr>
<td>Soft bake</td>
<td>115°C/60 seconds Hotplate</td>
</tr>
<tr>
<td>Expose</td>
<td>Nikon 1505 GGE G-Line (0.54 NA)</td>
</tr>
<tr>
<td>Develop</td>
<td>MF-321/15 + 50 DSP @ 21°C</td>
</tr>
</tbody>
</table>

**MICROPOSIT S1813 PHOTO RESIST with MICROPOSIT MF-321 DEVELOPER**

Table 2. Functional Lithographic Summary Data

<table>
<thead>
<tr>
<th>Sizing Energy</th>
<th>150 mJ/cm² (1.3 E₀)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>0.48 μm</td>
</tr>
<tr>
<td>Masking Linearity (±10% CD)</td>
<td>0.50 μm</td>
</tr>
<tr>
<td>Exposure Linearity (±10% E₀)</td>
<td>65% 45%</td>
</tr>
<tr>
<td>Focus Latitude (±10% CD)</td>
<td>2.25 μm 1.25 μm</td>
</tr>
<tr>
<td>± 65° Wall Angle</td>
<td></td>
</tr>
</tbody>
</table>
Handling Precautions

WARNING MICROPOSIT S1800 SERIES PHOTO RESISTS are combustible mixtures containing propylene glycol monomethyl ether acetate. Contact with eyes, skin and mucous membranes causes irritation. Handle with care. Do not get in eyes, on skin or on clothing. Avoid breathing vapors or mists. Use with adequate ventilation. Wash thoroughly after handling.

Wear chemical goggles, chemical gloves and suitable protective clothing when handling MICROPOSIT S1800 SERIES PHOTO RESISTS.

In case of eye or skin contact, flush affected areas with plenty of water for at least 15 minutes. Then contact a physician at once.

Consult product Material Safety Data Sheet before using.

Toxicological and Health Advantages

The solvent used in MICROPOSIT S1800 SERIES PHOTO RESISTS is propylene glycol monomethyl ether acetate. Toxicological studies reported that propylene glycol derivatives contained in MICROPOSIT S1800 SERIES PHOTO RESISTS do not demonstrate the adverse blood effects and reproductive effects that ethylene glycol derived other acetates demonstrate (NIOSH Current Intelligence Bulletin 9-50/83).

Storage

Store MICROPOSIT S1800 PHOTO RESISTS only in upright, original containers in a dry area at 50°-70°F (10°-21°C). Store away from light, oxidants, heat, and sources of ignition. Do not store in sunlight. Keep container sealed when not in use.

Equipment

MICROPOSIT S1800 SERIES PHOTO RESISTS are compatible with most commercially available photo-resist processing equipment. Compatible materials include stainless steel, glass, ceramic, unfilled polypropylene, high density polyethylene, polytetrafluoroethylene, or equivalent materials.

Technical Literature

Please contact your Shipley Technical Sales Representative for information on the use and performance of Shipley products.
Worldwide Operations
Shipley Company
455 Forest Street
Marlborough, MA 01752-3001
TEL: (508) 481-7950
FAX: (508) 485-9113

European Operations
Shipley Europe Ltd.
Herald Way
Coventry CV3 2RQ
United Kingdom
TELEX: 851311316
TEL: 441 203 457 203

Far East Operations
Shipley Far East Ltd.
Nishida-Nishia
1-83-1, Dokaihama
Itabashi-ku, Tokyo 175
Japan
TELEX: 781 28675
TEL: 81 35 520 5300

Domestic Sales Offices
Marlborough, MA
(508) 481-7950
(800) 832-6200

Carrollton, TX
(214) 446-2400
(800) 527-3730

Tempe, AZ
(602) 894-6499
(800) 826-6477

Santa Clara, CA
(408) 988-3600
(800) 423-9037

International Sales Offices
Evry, France
33 1 60 86 81 62

Milano, Italy
39 2 936 1566

Galdrop, The Netherlands
31 40 853 335

Norrkoeping, Sweden
46 11 108170

Jona, Switzerland
41 55 284 646/647

Esslingen, Germany
49 711-931 32-0

Kowloon, Hong Kong
852 6 940 661

Singapore
65-862-1888

International Distributors
Australia, China, India, Israel, Mexico, Singapore, South Africa, South Korea, Spain, Taiwan, Western Canada.

Manufacturing Locations
Marlborough, MA; Coventry, United Kingdom; Sasagami, Japan.

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