CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

ANALYTICAL MODEL OF HIGH FREQUENCY GALLIUM NITRITE MESFET'S

A graduate project submitted in partial fulfillment of the requirements

For the degree of Master of Science in

Electrical Engineering

By

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ABSTRACT

ANALYTICAL MODEL OF HIGH FREQUENCY GALLIUM NITRIDE MESFET'S

By

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Master of Science in Electrical Engineering

GaN material is a potential candidate for its inherent properties of wide bandgap, high electron velocity, high electric field at breakdown voltage, low thermal generation rate, high breakdown, good thermal conductivity and stability for high power and high frequency amplifier. Physics based analytical model of high frequency GaN MESFET has been developed to study the device physical parameters to achieve large channel current to deliver the high power density. The analytical model also incorporates the effect of the intrinsic parameters such as gate capacitance, transconductance on the cutoff frequency response of GaN MESFET device. In order to achieve high cut-off frequency, all physical dimension of the device such as gate length, active channel thickness and impurity doping concentration of channel and substrate have been taken into account to optimize the value of gate-source capacitance and gate-drain capacitance as well as the transconductance. The analytical model with detailed analysis of device physical parameters has been chronologically described in chapter 5.
Chapter 1 Introduction

1.1 GaN MESFET

In recent years the wide-band gap semiconductors, silicon carbide (SiC) and gallium nitride (GaN), have received incremented attention because of their potential for use in a wide variety of high-power high-frequency devices. High frequency electronic devices have been engendered in GaN and these devices are approaching the commercialization stage. Several candidate electronic devices are under investigation for fabrication in the wide band gap semiconductors due to possible enhanced performance. Their unique material properties, high electric field breakdown due to the wide band gap are what give these materials their incredible potential in the high frequency power device area as well as in the aerospace and microwave device industry [1-4].

Low intrinsic carrier concentration and resistance to ionization is caused as a result of wide energy gap. Additionally because of relatively low dielectric constant, the wide bandgap semiconductors have reduced capacitance loading [5]. High thermal conductivity is very vital since many of the electronic devices of interest are projected for high power applications and the performance of these devices depends upon the ability to extract the heat due to dissipated energy. The thermal conductivity of GaN is pretty much same as Si and the thermal conductivity of SiC is a factor of three higher [6]. Previous researches showed that GaN-based materials on Si are of lesser quality than such materials grown on sapphire and on SiC, mainly because of the larger lattice and thermal mismatches between GaN and Si [7].
Table 1.1 shows a few electrical properties of three major semiconductor materials.

Table 1.1: Some Material Properties of GaN, Si, and SiC [8]

<table>
<thead>
<tr>
<th>Properties</th>
<th>Description</th>
<th>GaN</th>
<th>Si</th>
<th>SiC</th>
</tr>
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<tbody>
<tr>
<td>$E_g (eV)$</td>
<td>Bandgap energy</td>
<td>3.4</td>
<td>1.12</td>
<td>3.2</td>
</tr>
<tr>
<td>$E_{BR} (MV/cm)$</td>
<td>Crystal electric field for breakdown in crystal</td>
<td>3.3</td>
<td>0.3</td>
<td>3.5</td>
</tr>
<tr>
<td>$\mu (cm^2/Vs)$</td>
<td>Mobility of electrons</td>
<td>990–2000</td>
<td>1500</td>
<td>650</td>
</tr>
<tr>
<td>$\varepsilon_R$</td>
<td>Dielectric Constant</td>
<td>9.5</td>
<td>11.9</td>
<td>10.0</td>
</tr>
<tr>
<td>$\kappa (W/0K - cm)$</td>
<td>Thermal Conductivity</td>
<td>1.5</td>
<td>1.3</td>
<td>4</td>
</tr>
</tbody>
</table>

There are many characteristics available today that can impact performance in a high power and frequency device, but the five most dominant characteristics are conduction efficiency, switching efficiency, breakdown voltage, cost, and size. These features determine power density and feasibly attainable system frequency [9]. In the above Table 1.1, the theoretical device conductivity (inverse of on-resistance) was found as a function of material and breakdown voltage after adjusting GaN mobility [10].

GaN has a wide band-gap energy (~3.4 eV at 300K) which is cognate to Si 1.12 eV and GaN 1.42 eV. This property of GaN is very helpful benefit for high temperature conditions [11]. As valence electrons jumps into the conduction band, the possibility of this occurrence during these operations will be much lower [12].

Large bandgap semiconductors bring about less noise; as a result GaN is a favorable one for making such high sensitive detectors in UV range. The conduction band
structure permits for a high saturation velocity \( \left( 3 \times 10^7 \text{cm/s} \right) \), flat field of \( 1500 \text{ cm}^2/\text{Vs} \), a breakdown electric field of \( 4 \text{ V/cm} \) and flat parasitic is suitable for power and frequencies of microwave applications [13]. Furthermore, GaN have thermal conductivity of \( 130 \text{ W/mK} \) and it is pretty much decent as compared to the thermal conductivity of Si, which is \( 149 \text{ W/mK} \) [14].

In compared to Si, GaAs based device, GaN offers ten times higher electrical breakdown characteristics, three times the band gap, and exceptional carrier mobility [14]. Some extraordinary properties that made GaN more suitable than GaAs is shown in Figure 1.1-

![Figure 1.1](image)

**Figure 1.1- Schematic diagram on the advantage of GaN over GaAs [14]**

However, it is said that GaN which has higher carrier mobility in wide temperature \((50 \leq T \leq 1000 \text{ K})\) and concentration \((10^{12} \leq N \leq 10^{19} \text{ cm}^{-3})\) ranges [15]. Also the resistivity could be improved to \(10^{11} \text{Ωcm} \) after optimizing the growth condition by varying GaN buffer layer from 1075 to 1135 °C.
1.2 GaN MESFET Performance

GaN material shows excellent material properties stated in above section GaN based devices exhibit extremely outstanding performance in device specifically frequency and power application.

A research on GaN MESFET device based device was conducted which show cutoff frequency of 900 MHz, delivering 51.1 W output power with 78 % power added efficiency [16]. Also for another GaN MESFET device 10W output power with a PAE of 34% at $V_D = 48V$ with a cut off frequency of 700 MHz and maximum frequency of 1.8 GHz was achieved [17]. A 0.8µm x 150µm GaN MESFET has been reported where cut off frequency ($f_T$) of 6.5 GHz and maximum frequency ($f_{max}$) of 14GHz which are in close agreement with their measured values of 6 and 14 GHz using Volterra-series technique [18] where the 1-dB compression point and output-referred third-order intercept point are 16.3dBm and 22.2 dBm respectively with a constant channel temperature of 300K is assumed whereas some other researchers achieved cut off frequency ($f_T$) of 20 GHz and a maximum frequency ($f_{max}$) of 50 GHz [19]. Another GaN MESFET device has been fabricated where the device performance showed 2GHz cutoff frequency and Power density of 2.2 W/mm with an associated power added efficiency of 27% at $V_{ds} = 30V$ and $V_{gs} = -2V$ [20].Another research investigated that the threshold voltage for GaN MESFETs ranged from 4 V to 20 V with maximum drain currents up to 300 mA/mm and transconductance up to 60 mS/mm which was measured for 100 µm wide devices having potential performance to high frequency application [21].
GaN MESFET offers decent device performance for the next generation of commercial use. Concurrently, a SiC MESFET carried on to mature in performance and manufacturing process stability. But now, GaN MESFET devices attain a power density of approximately 4.0 W/mm and power-added efficiencies greater than 50% on a regular basis. In some previous researches, devices with a source-drain spacing of 2.3 µm, a gate length of 0.3 µm, and a gate width of 2x50 µm were simulated where gate to source spacing was 1 µm which showed a cutoff frequency \( (f_T) \) of 11 GHz [22]. 1-dB minimum noise figure at maximum oscillation frequency of 36 GHz with an associated gain of 7.5 dB has been achieved by some other researcher [23]. Superior noise factor due to low carrier scattering and low radio frequency (RF) losses was grown from a 100-mm Si substrate GaN MESFET which also had showed high current density, high Transconductance, and high frequency performance (above 100 GHz) at the same time showed low dc-to-RF dispersion and low gate and drain leakage currents [24].

Researchers from University of Illinois at Urbana-Champaign [25] fabricated a GaN MESFET which demonstrated a power density of 2.2 W/mm with a power added efficiency of 27% at \( V_{Ds} = 30 \) V and \( V_{Gs} = -2 \) V at 2 GHz, the transconductance \( g_m \) was found 36 mS/mm and unity current gain cutoff frequency \( f_T \) and maximum frequency of oscillation \( f_{max} \) were measured to the value of 28 and 55 GHz which was at least twice the highest frequency data ever reported for GaN MESFETs.

In another research the output power was found to be 230W and cutoff frequency \( (f_T) \) of 30 GHz was obtained with 0.25 µm gate GaN MESFET [26]. Using drain current of 500 mA at \( V_{Ds} = 40 \) V and \( V_{Gs} = 0 \) V another GaN MESFET device was fabricated and this device showed cutoff frequency of 8 GHz, transconductance \( (g_m) \) of 93mS/mm and a
output power of 4W/mm with a power added efficiency of 50% and a gain 20dBm which was better than SiC MESFET simulation by the same researcher [27]. Some other researchers have fabricated a GaN MESFET device with $f_{\text{max}}$ is 15.6 GHz and is $f_T$ 7.2 GHz with a transconductance of 164 mS/mm with a PAE of 38% at $V_{DS}$ = 3.5V [28].

For the non-surface-depleted GaN MESFET, it has been found that the maximum transconductance ($g_m$) and the maximum cutoff frequency are 244 mS/mm, 230 GHz, with a maximum output power of 2.66 W/mm [29]. Another GaN based MESFET research obtained cutoff frequency $f_T$ and maximum frequency $f_{\text{max}}$ as to be 6.35GHz and 10.25 GHz respectively with a 0.3µm gate length [30] whereas for a 0.1 µm gate-length zincblende crystal structure of GaN MESFET showed maximum cutoff frequency and transconductance of 220 GHz and 210 mS/mm respectively [31].

The output power of 9.2 W with power-added efficiency of 65 % with the bandwidth of 500–600 MHz was obtained from GaN MESFET [32]. A GaN MESFET showed RF power of 200W which have a gate width of $2 \times 50 \mu$m were fabricated by some researchers [33]. This device shows cutoff frequency $f_T$ of 11 GHz where maximum output power density reached to 2.2 W/mm with an accompanying power-added efficiency of 27%. GaN based MESFET for microwave devices have been fabricated in order to compare the device performance on SiC and Sapphire substrate where the exceptional power densities 32W/mm and 12W/mm have been observed [34]. Also, very high power added efficiencies of 74% (6 W/mm, 4 GHz) have been attained by Japanese companies where it has been demonstrated power exceeding 150 W with a 2GHz cutoff frequency [35].
On Sapphire GaN/AlGaN based HEMT devices with a 1 nm AlN interlayer at a room temperature mobility of 1780 cm$^2$/Vs and an electron sheet carrier density of $1.2 \times 10^{12}$ cm$^{-2}$ which exhibited a power density of 4.9 W/mm and a linear gain of 14 dB and a PAE beyond 32% are obtained at 10 GHz with a gate width of 1 mm were accomplished [36]. Also for GaN HEMT device, a maximum power added efficiency greater than 56% while maintaining output power of 205 Watts with a cutoff frequency of 1.2 GHz and maximum frequency of 1.4 GHz was designed on SiC substrate for radar application [37].

A GaN high electron-mobility transistors (HEMTs) with a cutoff frequency ($f_T$) of 25 GHz and maximum frequency ($f_{max}$) of 33 GHz was fabricated under pulse and continuous conditions at different temperatures with a gate width of 125x2µm [38]. For another GaN HEMTs a power output of 9.8 W/mm with a cutoff frequency ($f_T$) of 101 GHz and maximum frequency ($f_{max}$) of 155 GHz have been obtained which are potential choices for high-frequency operation [39]. Some researchers showed AlGaN/GaN high-electron-mobility transistors (HEMTs) in SiC Substrate with a conductance ($g_m$) of to 94 mS/mm cutoff frequency ($f_T$) of 9 GHz and maximum frequency ($f_{max}$) of 28 GHz at 600K temperature whereas at 300 K temperature the transconductance ($g_m$) becomes 248mS/mm with the cutoff frequency ($f_T$) of 23 GHz and maximum frequency ($f_{max}$) of 70 GHz for $V_{Ds} = 18$V [40].

Researchers from University of California Santa Barbara have fabricated AlGaN/GaN high electron mobility transistors (HEMT) which provided a current density of 850 mA/mm and transconductance of 93 mS/mm under dc conditions [41]. The cutoff
frequency \( f_T \) was 19 GHz and maximum frequency \( f_{\text{max}} \) of 46 GHz for this 0.7 \( \mu \text{m} \) gate length device.

A research on 17\% AlGaN mole fraction HEMT structure on semi-insulating SiC substrates was conducted which showed an output power of 103 W with a high power density of 5.2 W/mm and power added efficiency (PAE) of 35.3\% [42]. Another research on AlGaN/GaN power HEMT in sapphire substrate achieved an output power densities of 1.1W/mm with PAE of 20.1\% with a cutoff frequency \( f_T \) was 36 GHz and maximum frequency \( f_{\text{max}} \) of 70 GHz where gate-to-drain breakdown voltages up to 230V and channel currents >300mA/mm were obtained [43]. Some researchers obtained the transconductance of 68mS/mm with maximum frequency of approximately 31 GHz and a cutoff frequency of 1.8 GHz with an RF power of 84 mW/mm and maximum drain to source current density is approximately 174 mA/mm for 1400 mm wide gate AlGaN/GaN HMET where \( V_{GS} = -1.1 \text{V} \) and \( V_{DS} = 6 \text{V} \) [44]. Some researchers fabricated AlGaN/GaN high electron mobility transistors (HEMTs) which shows 9.8 W/mm with a cut off frequency of 8 GHz [45].

A research group in Sweden showed an AlGaN/GaN-HEMT device in SiC Substrate that attained a DC transconductance \( g_m \) of 150 mS/mm with a cutoff frequency \( (f_T) \) of 25 GHz and maximum frequency \( f_{\text{max}} \) of 50 GHz with a saturated drain current \( (I_d) \) of 950 mA/mm from S-parameter measurements performed on a 100 \( \mu \text{m} \) HEMT [46].
1.3 Objective

The main objective of this research is the analytical modeling of GaN MESFET to observe the channel current, Transconductance, capacitance and cut-off frequency. The parameters were chosen very carefully centered on the Wurtzite GaN MESFET’s structure. The beginning steps are to calculate the saturation current, channel conductance and Transconductance. In the end, these results will be tested by computer simulation and should agree with experimental data for a GaN MESFET.
Chapter 2 Overview of GaN Material

2.1 GaN Material

Gallium nitride (GaN) is a direct bandgap semiconductor materials of the member in III/V group commonly used in bright light-emitting diodes since the 1990s. Its wide band gap which is estimated as 3.4 eV affords it work in all field especially in optoelectronic, high-power and high-frequency devices but it has noticeable features in electronics devices [8]. Table 2.1 shows the basic information of Ga and N material.

<table>
<thead>
<tr>
<th>Basic Info.</th>
<th>Gallium</th>
<th>Nitrogen</th>
</tr>
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<tr>
<td>Discovered By</td>
<td>Paul-Emile Lecoq de Boisbaudran</td>
<td>Daniel Rutherford</td>
</tr>
<tr>
<td>Symbol</td>
<td>Ga</td>
<td>N</td>
</tr>
<tr>
<td>Atomic Number</td>
<td>31</td>
<td>7</td>
</tr>
<tr>
<td>Atomic Weight</td>
<td>69.723</td>
<td>14.0067</td>
</tr>
<tr>
<td>Standard State</td>
<td>Solid at 298 K (but melts only slightly above this temperature)</td>
<td>Gas at 298 K</td>
</tr>
<tr>
<td>Group in Periodic Table</td>
<td>13</td>
<td>15</td>
</tr>
<tr>
<td>Period in Periodic Table</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Block in Periodic Table</td>
<td>p-block</td>
<td>p-block</td>
</tr>
<tr>
<td>Color</td>
<td>Silvery white</td>
<td>Colorless</td>
</tr>
<tr>
<td>Classification</td>
<td>Metallic</td>
<td>Non-metallic</td>
</tr>
</tbody>
</table>

Table 2.2 shows some parameter which is necessary in the calculation of all properties when using GaN as a material.
Table 2.2: Some Electronic, Thermal Parameters with their unit [11]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap</td>
<td>3.44 eV</td>
</tr>
<tr>
<td>Lattice constant</td>
<td>3.189 Å (a), 5.185 Å (c)</td>
</tr>
<tr>
<td>Breakdown field</td>
<td>$3.3\times10^6\text{V/cm}$</td>
</tr>
</tbody>
</table>
| Dielectric constant              | Zinc blende- 9.7 (static), 5.3 (high freq.)
|                                  | Wurtzite- 8.9 (static), 5.35 (high freq.) |
| Optical phonon energy            | 91.2 meV             |
| Ionization energy                | Si (12 meV), Mg (210 meV) |
| Mobility (cm²V⁻¹S⁻¹)             | $\mu_n=1000$, $\mu_h=<200$ |
| Saturation velocity              | $2.5\times10^7\text{cm/s}$ |
| Thermal Conductivity             | 1.5 W/cm-K           |

2.2 Energy- Band Structure

2.2.1 Band structure of Zinc blende crystal structure

Below Figure 2.1 showed the band structure of Zinc Blende crystal structure of GaN. Here, four different types of energy are observed.

![Zinc blende crystal structure of GaN](image)

Figure 2.1: Band structure of Zinc blende crystal structure of GaN [48].
The energy bandgap $E_g$ in $\tau$-valley is found to be 3.2eV which was measured from the conduction band minima and valance band maxima at $k$ (wave vector) =0. Secondly, bandgap $E_X$ of 4.6 eV is defined as the energy at X-valley in (100) orientation. Another bandgap $E_L$ in the range of 4.8-5.1 eV is found for the energy in (111) orientation. The spin off band $E_{SO}$ in the valence band is confined to the value of 0.02 eV.

2.2.2 Band structure of Wurtzite crystal structure

Below Figure 2.2 showed the band structure of Wurtzite crystal structure of GaN. Here five different types of energy are observed.

![Figure 2.2: Band structure of Wurtzite crystal structure of GaN](image)

At first, the energy bandgap in $\tau$- valley is noted as $E_g$ which have been found to be 3.39 eV. This value was measured from the conduction band minima and valance band maxima at $k$ (wave vector) =0. Secondly, bandgap $E_A$ of 4.7 - 5.5 eV is defined as the energy separation at A-valley. Another bandgap $E_{M-L}$ of 4.5 – 5.3 eV is found for the energy separation at M-L valleys. The spin off band $E_{SO}$ in the valence band is confined to the value of 0.008eV. And finally, the band energy $E_{cr}$ is defined as the energy of
crystal field which is measured to be 0.04 eV. The value of electron affinity for zinc blende and wurtzite crystal structure is about 4.1 eV.

2.2.3 Band gap energy and excitation energies Vs Temperature

For GaN Wurtzite structure the value of $E_g(0)$ which is excitation energy at $0^\circ K$ has a value of 3.47eV and the excitation energy with temperature dependence below 295K is given by [49]:

$$E_g(T) - E_g(0) = -5.08 \times 10^{-4} T^2/(996 - T); \ (T \text{ in K}). \ \ldots \ldots (2.1)$$

$$E_g(300K) = 3.44 \text{ eV}$$

Where $E_g(T)$ is the temperature dependent excitation energy gap. The graphical analysis of excitation energy under different temperatures below 300K is shown in Figure 2.3

![Figure 2.3: Excitation energy vs. temperature [49]](image-url)
It can be determined from the above Figure 2.3 that for Wurtzite structure of GaN, as the temperature increases the excitation energy exponentially drops. There is another expression called Varshni expression [50] which is expressed as below

\[
E_g = E_g(0) - 9.39 \times 10^{-4} \frac{T^2}{(T+772)} \text{ (eV)}; \quad \text{where } E_g(0) = 3.427 \text{ eV} \quad \ldots \quad (2.2)
\]

2.2.4 Band gap energy Vs Temperature for Wurtzite structure of GaN

In many researches by using different techniques, wurtzite structures of GaN samples were grown on different substrates like SiC, sapphire to obtain the band gap energy difference with the effect of temperature [51]. The graphical representation is shown below in Figure 2.4

![Figure 2.4: Band gap energy Vs Temperature for Wurtzite structure of GaN in different substrate [51]]

From the above Figure 2.4 it is observed that the wurtzite structure of GaN shows very different results which are grown in different substrate.
2.2.5 Band gap energy Vs Temperature for Zinc blende structure of GaN in MgO substrate

For GaN zinc blende structure the value of $E_g(0)$ which is excitation energy at $0^\circ K$ has a value of 3.28eV and the excitation energy with temperature dependence is given by [49]:

$$E_g = E_g(0) - 7.7 \times 10^{-4} T^2 / (T+600); \text{ (T in K).} \quad \ldots \ldots \text{(2.3)}$$

For the Varshni expression [49] is expressed as below

$$E_g = E_g(0) - 9.39 \times 10^{-4} T^2 / (T+772) \text{ (eV)}; \quad \text{where } E_g(0) = 3.427 \text{ eV} \ldots \ldots \text{(2.4)}$$

Some researchers have investigated the variance of band gap energy with temperature for zinc blende structure of GaN which was grown on MgO (1x1) substrates [52]. Their findings are graphically represented in Figure 2.5

![Figure 2.5: Band gap energy Vs Temperature for Zinc blende structure of GaN in MgO (1x1) substrate [52]](image)

From the above Figure 2.5, it is observed that bandgap energy drops from 3.30eV to 3.23eV with the increase of temperature from $0^\circ K$ to $300^\circ K$ for a GaN zinc blende structure which is grown in MgO substrate.
2.2.6 Band gap energy Vs Temperature for Zinc blende structure of GaN in Si substrate

In another research a GaN zinc blende structure was grown in Si (100) substrate and band gap energy was observed with the variance of temperature [52]. The temperature dependences were extracted from pseudo dielectric-function spectrum using two different theoretical models. The temperature dependent bandgap for zinc blende is shown in Figure 2.6

![Band gap energy Vs Temperature for Zinc blende structure of GaN in Si substrate](image)

Figure 2.6: Band gap energy Vs Temperature for Zinc blende structure of GaN in Si substrate [52]

2.3 Intrinsic carrier concentration

Intrinsic carrier concentration denoted by \( n_i \) is the concentration of free carriers in both valance band and conduction band of intrinsic semiconductor which were created due to the thermal excitation of a carrier from valance band to the conduction band. Wide bandgap material like GaN has low intrinsic carrier concentration as this brings the inherent quality to possess wide bandgap properties. This intrinsic carrier concentration \( n_i \) can be expressed by using the following equation [53]
\[ n_i = (N_C N_V)^{1/2} \exp(-E_g/(2k_B T)) \] \hspace{1cm} (2.5)

Where T is measured as degree kelvin, \( k_B \) is Boltzmann constant valued as \( 8.6173 \times 10^{-5} \text{eV K}^{-1} \) and \( N_C \) is the effective density of states in the conduction band which can be valued by below equation:

For Zinc blende structure \( N_C \approx 4.82 \times 10^{15} \left( \frac{m_e}{m_0} \right)^{3/2} \frac{T}{T^2} \text{ (cm}^{-3} \text{)} \)

\[ \approx 2.3 \times 10^{14} \frac{T}{T^2} \text{ (cm}^{-3} \text{)} \hspace{1cm} (2.6) \]

For Wurtzite structure \( N_C \approx 4.82 \times 10^{15} \left( \frac{m_e}{m_0} \right)^{3/2} \frac{T}{T^2} \text{ (cm}^{-3} \text{)} \)

\[ \approx 4.3 \times 10^{14} \frac{T}{T^2} \text{ (cm}^{-3} \text{)} \hspace{1cm} (2.7) \]

In equation 2.5, \( N_V \) is the effective density of states in the Valance band which can be valued by below equation:

For Zinc blende structure \( N_V = 8.0 \times 10^{15} \frac{T}{T^2} \text{ (cm}^{-3} \text{)} \hspace{1cm} (2.8) \)

For Wurtzite structure \( N_V = 8.9 \times 10^{15} \frac{T}{T^2} \text{ (cm}^{-3} \text{)} \hspace{1cm} (2.9) \)

The following Figure 2.7 shows the experimental analysis for both Wurtzite and Zincblende structures of GaN [53].

Temperature (K)
Figure 2.7: Intrinsic carrier concentration vs. temperature for GaN, Wurtzite & Zinc Blende structure [53].

From the above Figure 2.7 it is observed that the Wurtzite structure of GaN shows lower intrinsic carrier concentration compare to zinc blende GaN. For lower temperature the most significant aspect is the lower intrinsic carrier concentration of the order $10^{-9}$ for GaN at 300°K compare to Si and GaAs.

2.4 GaN Crystal Structure

GaN forms in two types of crystal structure. These are

1) Zincblende (ZB) Structure.

2) Wurtzite (WZ) Structure.

Zinc blende structure and Wurtzite structure are very closely associated crystallographically in many ways. The next neighbors closeness are tetrahedral. The Bravais lattice of Wurtzite assemblies are hexagonal and the axis perpendicular to the hexagons which is usually labeled as c-axis. The structure along the c-axis can be thought
as a prearrangement of the layer of atoms of the same element (e.g., all N or all Ga) erected from regular hexagons. For the Zinc blende lattice the piling of the layers is [54]:

\[ \ldots Ga_A N_A Ga_B N_B Ga_C N_C Ga_A N_A Ga_B N_B Ga_C N_C \ldots \]

But for the Wurtzite structure the stacking sequence is changed to:

\[ \ldots Ga_A N_A Ga_B N_B Ga_A N_A Ga_B N_B Ga_A N_A Ga_B N_B \ldots \]

For the GaN crystal, the horizontal planes are the polar planes. In Figure 2.8 a stick and ball model of GaN is shown [55]. In that model, for zinc blende \{111\} and for wurtzite \{0001\} is the polar planes.

![Figure 2.8: Planes in GaN Crystal (a) Zinc blende (b) Wurtzite [55]](image)

From above Figure 2.8, it is also observed that two types of nonpolar planes in each structure which are \{110\} and \{112\} in zinc blende and for wurtzite in the a-plane [1120] and in the m-plane [1010]. These two nonpolar planes are orthogonal to each other. The first type which is drawn in blue in Figure 2.8 which contains two bonds of the four
tetrahedral bonds that is \{110\} and \{1120\}. Another type consists of parallel bonds which is drawn in red in Fig. 2.8 which are \{112\} and \{10\overline{1}0\}. Any other vertical planes are known as high-index planes [55].

The atomic arrangements of the four non-polar plane projections have been sketched in Fig. 2.9 Broken lines indicate major inclined planes perpendicular to the projection.

Figure 2.9: Projections of the four nonpolar planes: (a) zincblende type I, \{1\overline{1}0\}-zone axis (b) zincblende type II, \{11\overline{2}\} - zone axis (c) wurtzite type I, \{11\overline{2}0\}-zone axis and (d) wurtzite type II, \{1100\} zone axis [55]

For the ambient condition, it is assumed that a thermodynamically stable structure is WZ for bulk like AlN, GaN, and InN. It is also seen that ZB structure for GaN and InN are
stable for epitaxial growth of thin films on \{0 1 1\} crystal planes of cubic substrates such as Si, SiC, MgO and GaAs [17]. Because of the intrinsic tendency of forming the WZ structure the problem can be overcome by the topological compatibility. Table 2.3 shows some basic parameter for GaN, AlN and InN.

Table 2.3: Lattice constants (a, b) & unit cell parameter (u) for GaN, AlN & InN [50]

<table>
<thead>
<tr>
<th>Parameters</th>
<th>GaN</th>
<th>AlN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3.111 Å</td>
<td>3.189 Å</td>
<td>3.544 Å</td>
</tr>
<tr>
<td>B</td>
<td>4.978 Å</td>
<td>5.185 Å</td>
<td>5.718 Å</td>
</tr>
<tr>
<td>U</td>
<td>0.382 Å</td>
<td>0.377 Å</td>
<td>0.379 Å</td>
</tr>
</tbody>
</table>

2.4.2 Zinc blend (ZB) Structure

The zinc blende structure has a cubic unit cell as shown in Fig.2.8, containing four group III components and four nitrogen components where the lattice constraint of about 4.5Å, An ideal angle was measured as 109.470°, phase is a metastable and observed only for hetero epitaxial layers on highly mismatched cubic substrates like GaAs, Si and MgO. The member of highly unequal substrates, such as hexagonal sapphire, cubic GaAs and Si, there is definite amount of zinc blende phase of the nitrides segregated by crystallographic imperfections from the wurtzite phase.
2.4.3 Wurtzite (WZ) Structure

The wurtzite crystal structure, named after the mineral wurtzite, is a crystal composition for numerous binary compounds as shown in Figure 2.11 b). It is an example of a hexagonal crystal system where the two lattice constants c and a. It contains six atoms of each type. The u value is equivalent to a/c where a is the bond distance in the c direction which also known as the basal plane.
For the ideal wurtzite crystal structure $c/a = 1.633$ and $u = 0.375$ [55- 57]. The wurtzite structure shows two possibilities to deviate from the ideal arrangement, by changing the $c/a$ ratio and by changing the $u$ value. These types of deviations are observed in wurtzite-type structures but there exists a correlation between the $c/a$ ratio and the $u$ parameter. These two parameter behaves as if $c/a$ decreases, then $u$ increases in such a way that the four tetrahedral distances remain nearly unchanged and the tetrahedral angles are distorted[58]. Sometimes the bond lengths would be equal if:

$$u = \frac{1}{3} \left( \frac{a}{c} \right)^2 + \frac{1}{4} \quad [58] \ldots \ldots (2.10)$$

The compounds with the greatest differences of $c/a$ demonstrate the largest departure from the ideal $c/a$ ratio [58]. The distortions were explained by long-range polar interactions. Now the important plane and polarity of wurtzite GaN is shown in Figure 2.12 and 2.13.

![Figure 2.12: Important plane of wurtzite GaN [59].](image-url)
2.5 Charge effects for GaN

The (In, Al, Ga) N–based materials are a promising class of materials for use in many electronic, optoelectronic device which is used in modern everyday life. Unlike from orthodox cubic semiconductors, GaN based materials exist normally in the Wurtzite phase and exhibit strong polarization in the [0001] direction (C-direction) [50]. It is essential to understand the polarization field effects.

2.5.1 Polarization Charge effect

Figure 2.14 (a) shows the ball and stick prototype of GaN in the basal plane and the associated polarization in the crystal. In the classical model, these polarizations charges occur on each unit cell [60]. In Figure 2.14 (b) it is showed that within the crystal, the synopsis of internal polarization is null after leaving ±Qπ charge at each end of the crystal forming a dipole. In Figure 2.14 (c) it is presented that a screening dipole which is the result of placing equal and opposite charges at or close to the charges of polarization dipole is created since of the unscreened dipole which build a non-sustainable dipole moment.
The spontaneous polarization charge density in GaN which is symbolized by \( n_{\pi} \approx 10^{13} \text{ cm}^{-2} \) leads to an electric field \( E_{\pi} \) which is given by:

\[
E_{\pi} = \frac{Q_{\pi}}{\varepsilon} = \frac{n_{\pi}}{\varepsilon} \approx 1.6 \text{ MV/cm} \quad (2.11)
\]

In a crystal of thickness \( d = 1 \mu\text{m} \), the voltage across the material that results from this dipole charge \( (V_{\pi}) \) is given by:

\[
V_{\pi} = E_{\pi} d = 160 \text{ V} \quad (2.12)
\]

In the absence of surface states, as the material becomes impenetrable, the electric field in the material will remain constant until the valence band crosses the Fermi level as
shown in Figure 2.14 (b). The thickness of the film (d_{cr}) at which this occurs is given simply by

\[ d_{cr} = \frac{E_g}{e\pi} = \frac{3.4 \text{ eV}}{1.6 \text{ MeV/cm}} \approx 215 \text{Å} \]  

(2.11)

Where \( E_g = 3.4 \text{ eV} \) is the Bandgap of GaN. Once \( d > d_{cr} \), holes begin to accumulate at the surface (created by generating across the gap), leading to an equal electron concentration which drifts to the substrate-epi interface (the GaN N-face), creating a screening dipole. This is illustrated in Figure 2.14 (c). The degree of the screening charge (\( Q_{scr} \)) upsurges unceasingly with epitaxial layer depth. The evolution of the screening charge with distance \( d \) is obtained by recognizing that the maximum voltage across the structure is the bandgap of the material or

\[ \frac{1}{e} E_g = |\epsilon|. d = \left( \frac{Q_{\pi} - Q_{scr}}{e} \right) d \]  

(2.12)

\[ Q_{scr} = Q_{\pi} - \frac{eE_g}{ed} \]  

(2.13)

As \( d \to \infty \), \( Q_{scr} \to Q_{\pi} \), or in other words for very profuse samples the polarization dipole is fully screened.
If there be existent a surface donor state is expected, a very similar situation matures, except that instead of holes providing the positive screening charge, ionized surface donors do. These states pin the Fermi level at the surface to create a built-in voltage equal to the donor depth as illustrated in Figure 2.15 (a). Figure 2.15 (b) shows the schematic diagram of an n-type GaN sample along with charge profile and band diagram when the effects of surface states are taken into account.

As the epitaxial thickness increases, the donor level ($E_{DD}$) approaches the Fermi level $E_F$ at the GaN surface and the screening charge ($N^+_DD$) increases as given by the Fermi-Dirac occupancy probability [61]

$$N^+_DD = [1-f(E_{DD}(0))] \cdot N_{DD} \quad \text{................. (2.16)}$$
2.5.2 Piezoelectric charge effect in GaN quantum well

By combining the epitaxial growth which is performed in the c plane [0001] orientation of wurtzite crystal structure of GaN creates a piezoelectric field. Associated electrostatic charge densities have showed influence in many properties such as electric field, carrier distribution as well as some optical and electric properties of nitride materials and devices.

The piezoelectric polarization field \( P_{pz} \) can be determined by piezoelectric coefficients \( e_{ij} \) and the strain tensor \( \varepsilon_j \) and is given by [65]

\[
P_{pz} = e_{ij}\varepsilon_j = d_{ij}\epsilon_{jk}\varepsilon_k \quad j, k = xx, yy, zz, yz, zx, xy \ldots \quad (2.17)
\]

Where \( d_{ij} \) are the piezoelectric coefficients relating the polarization to the stress tensor \( \sigma_j = c_{jk}\varepsilon_k \) and \( c_{jk} \) is the elastic tensor.

In Figure 2.16 some results of positional requirement of the piezoelectric polarization, piezoelectric charge distribution and conduction band potential profile for several possible approximations are shown. It has been seen that the band diagram of GaN quantum well (QW) hetero-structures is strongly affected by structural imperfections.
Figure 2.16: (a) Piezoelectric polarization, (b) Piezoelectric charge distribution and (c) Conduction band edge for the 2 nm GaN quantum well [57]

Where $L_1$ and $L_2$ are segregation lengths, $P_{\text{piezo}}$ is piezoelectric polarization for GaN Quantum well in Figure 2.16

2.6 Drift velocity Vs Electric field

In Figure 2.17 the relationship between the drift velocity for GaN wurtzite and zinc blende with respect to electric field has shown. The curve 1 is for wurtzite structure of GaN and the electric field is applied beside (1010) direction and the curve 2 is for zinc blende for which the electric field is applied to (100) direction.
The drift velocity is also temperature dependent. In Figure 2.18 it has shown for the wurtzite structure of GaN, the electric field dependency of electron drift velocity for different temperature 77K, 300K, 500K and 1000K respectively.

2.7 Growth process and nucleation layer

GaN crystal can be grown by using heteroepitaxial approaches which comprises a variety of foreign substrates such as zinc oxide, aluminum nitride, sapphire, silicon carbide, and silicon. The benefit of using sapphire, silicon carbide and silicon is that as
they have very close lattice constant, the lattice mismatch percentage is very low associated to other substrate. Although there are a lot of drawbacks for heteroepitaxial approach like lattice mismatch, thermal expansion coefficient mismatch, mosaic crystal structure, biaxial induced stress, and wafer bowing which diminishes the performance. To overcome these shortcomings, special techniques have been introduced such as low temperature buffer technologies or epitaxial lateral overgrowth (ELOG) techniques which will give enhanced performance by removing the structural defects and need for low-temperature buffer layers by using native substrates.

Nucleation layer construction is one of the important factors for high quality gallium nitride (GaN) growth on a substrate. In Figure 2.20 AFM image of a low temperature GaN nucleation layer development in a sapphire substrate is shown.

![Figure 2.19: AFM image of the GaN nucleation layer [65]](image)

2.7.1 MOVPE Growth:

Metal organic vapour phase Epitaxy (MOVPE) also known as metalorganic chemical vapour deposition (MOCVD) is a highly complex process for creating semiconductor multilayer structures by growing crystalline layers. It is a non-balance
enlargement procedure that depends on vapor transport of the antecedents and resulting responses of alkyls of Group III and hydrides of Group V in a warmed zone and typically at condensed pressure. This strategy came to limelight since the research of Manasevit (1968) who showed that triethylgallium (TEGa) and arsine saved single GaAs pyrolytically in an open tube which was in low temperature divider reactor. The essential MOVPE process for creation of GaN is:

$$Ga(CH_3)_3 (V) + NH_3(V) \rightarrow GaN (S) + 3 CH_4 (V)$$  \[66] \ldots 

In Figure 2.20, approach of MOCVD process is shown.

![Figure 2.20: Approach of MOCVD process [67]](image)

**2.7.2 Molecular Beam Epitaxy (MBE):**

Molecular beam epitaxy is the technique for epitaxial growth with the interaction of one or several molecular beams that occurs on a surface of a heated crystalline substrate.
Figure 2.21: A MBE system [68]

The solid sources materials are placed in effusion cells to provide an angular distribution of atoms or molecules in a beam. The substrate is heated to the necessary temperature and, when needed, continuously rotated to improve the growth homogeneousness.

MBE provides unique capability to study crystal growth in real-time and on a sub-nanometer scale. For having a growth rate of a few Å/s, obligatory need of ultra-high vacuum and for being expensive, it is not that popular type of growth process to the researchers.

2.7.3 Hydride vapour phase epitaxy

The Hydride vapour phase epitaxy (HVPE) is the most widespread growth process used to grow thick, strain relieved buffer layer.
The equations related to HVPE are –

For 700-900°C

\[ Ga + HCl \rightarrow GaCl + \frac{1}{2} H_2 \] [69] … ….. (2.18)

For 900-1100°C

\[ GaCl + NH_3 \rightarrow GaN + HCl + H_2 \] [69]…… ….. (2.19)

\[ GaN \leftrightarrow Ga + \frac{1}{2} N_2 \] ……… (2.20)

\[ Ga + NH_3 \leftrightarrow GaN + \frac{3}{2} H_2 \] ………………… (2.21)

2.7.4 GaN Bulk Crystal Growth:

Recently there is a lot of commotion in research, targeting a suitable growth method for the manufacture of GaN bulk crystals, which could be used as a substrate material for nitride based devices. Compared to the conventional semiconductor materials there are quite a few complications growing GaN from its melt, due to its high vapor pressure and the high melting point.
Figure 2.23: One-cm diameter bulk GaN substrate [69]

Right now, it is very difficult to get native substrates in high quality and large measures. Some reasons behind this are, for not being feasible of classical melt growth due to high N vapor pressure and Low pressure solution growth (liquid phase epitaxy) suffers from low solubility of N.

Some important device properties of GaN epitaxy is compared with heteroepitaxial GaN on SiC, sapphire, or silicon lattice constant mismatch, dislocation density and thermal conductivity have been shown in the Table 2.4 below [69].

<table>
<thead>
<tr>
<th></th>
<th>GaN on Bulk GaN</th>
<th>GaN on SiC</th>
<th>GaN on Sapphire</th>
<th>GaN on Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lattice Constant Mismatch</td>
<td>0%</td>
<td>3.5% mismatch</td>
<td>14% mismatch</td>
<td>17% mismatch</td>
</tr>
<tr>
<td>Dislocation Density</td>
<td>$10^4 - 5 \times 10^6$ / cm$^2$</td>
<td>$1 \times 10^9$ / cm$^2$</td>
<td>$5 \times 10^9$ / cm$^2$</td>
<td>$1 \times 10^{11}$ / cm$^2$</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>2.5 W/cm-K</td>
<td>1.3 W/cm-K</td>
<td>1.2 W/cm-K</td>
<td>2.0 W/cm-K</td>
</tr>
</tbody>
</table>
2.8 Substrate used for GaN

Many substrates are used for GaN such as Sapphire, SiC, Si, GaN, AlN, LiAlO$_2$, ZrB$_2$, MgO and others.

![Substrates comparison for GaN](image)

**Figure 2.24: Substrates comparison for GaN [70]**

From the Figure 2.24 it can be seen that GaN/6H-SiC have very close lattice match and bandgap is almost equal to each other. For GaN and Sapphire lattice mismatch is only 14% and for GaN and Si has only 17% of lattice mismatch.

There are many circumstances including lattice coincidence, lattice matching, thermal expansion coefficient (TEC), temperature stability, conductivity, availability, price are given thought before picking a substrate. Ordinarily sapphire is used as it has improved quality in many cases, high thermal resistance, available up to inches in diameter and most importantly it is economical than any other substrate [70].

Another very favorable substrate for the growth of GaN layer is Si which allows future incorporation of well-established Si centered electronics with GaN-based photonic devices. There are many more advantages of using Si as substrate in GaN layer, such as high quality, large size, low cost and thermal stability at high growth temperature. But,
the growth of GaN on Si substrate with crystalline quality compared to GaN grown on sapphire is still difficult as there is a large mismatch in relevant lattice parameters and large difference in thermal expansion coefficient between GaN and Si [70-72].

Table 2.5: Fundamental properties of materials involved in GaN growth [70]

<table>
<thead>
<tr>
<th>Material</th>
<th>Crystal structure</th>
<th>Lattice Constant (Å)</th>
<th>Thermal mismatch (10^{-6}/K)</th>
<th>Lattice mismatch %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(a)</td>
<td>(c)</td>
<td>(a)</td>
</tr>
<tr>
<td>GaN</td>
<td>Hexagonal</td>
<td>3.18</td>
<td>5.18</td>
<td>5.59</td>
</tr>
<tr>
<td>AlN</td>
<td>Hexagonal</td>
<td>3.104</td>
<td>4.966</td>
<td>4.2</td>
</tr>
<tr>
<td>Si</td>
<td>Diamond</td>
<td>5.43</td>
<td>5.42</td>
<td>3.59</td>
</tr>
<tr>
<td>Sapphire</td>
<td>Hexagonal</td>
<td>4.758</td>
<td>12.99</td>
<td>7.5</td>
</tr>
</tbody>
</table>

The foremost difficulty, which actually averts direct growth of GaN on Si surfaces, is the poor nucleation of GaN on Si, which leads to an island-like GaN structure. In order to vanquish this difficulty, an AlN buffer layer or intermediate layer, grown prior to GaN growth, is usually used. It has been reported that the quality of buffer layer plays an important role in the thick GaN growth [72].

2.9 Growth defects and process induced defects

There could be many defects accompanying to GaN grown in diverse substrate. The most common defects are mismatch of lattice constant, thermal expansion coefficient and dislocation. There are many other defects such as inversion domain, stacking mismatch boundaries, micropipes/nanopipes or voids and surface pits. These faults will cause the periodicity of the crystal to be dislocated over distances of several atomic diameters which will disturb the electronic and optoelectronic properties of the devices. Dislocations defects cause rapid recombination of holes with electrons without
conversion of their available energy into photons, which causes heating up of the crystal and making electronic and optoelectronic devices malfunction [73].

Figure 2.25: Schematic representation of common point defects [73].

Also, another defect is strain which has been identified to cause the lattice constant of a crystal to upsurge (tensile strain) or reduction (compressive strain). Strain measurement, is typically investigated using x-ray diffraction [74]. Figure 2.26 shows effects of lattice strain using x-ray diffraction.

Figure 2.26: Effect of lattice strain (a) no strain; (b) uniform strain; (c) non-uniform strain [74].
Polycrystalline materials hold grains of single crystals with various crystallographic orientations. Each grain is bounded by a layer of interlocking boundary atoms in amorphous phase, called grain boundary. A twin is an imperfection in which a mirror duplicate of the regular lattice is formed. [74]. Figure 2.27 shows the twin effect [75].

Figure 2.27: Schematic diagram of a twin [75].

To lessen these defects, there are many methods have been used. One of them is to rise layer thickness. By doing this, it lessens defect density but it leave quandary such as crack and bow [76]. In Figure 2.28, a 2 inch wafer of GaN/Sapphire with crack after cooling is shown.

Figure 2.28: 2´´ wafers GaN/sapphire with crack after cooling down [76]
Table 2.6 shows the growth process induced defects and their source of defects for growth technique like MOCVD, MBE in different substrate like Sapphire and SiC?

**Table 2.6: Process induced defects and their source [77]**

<table>
<thead>
<tr>
<th>Growth Method</th>
<th>Substrate</th>
<th>Type of defect</th>
<th>Source of defect</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOCVD</td>
<td>Sapphire</td>
<td>Threading dislocations</td>
<td>Nucleation Layer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Grain Boundaries</td>
<td>Misorientation of crystal grains</td>
</tr>
<tr>
<td>MOCVD</td>
<td>6H-SiC</td>
<td>Threading dislocations</td>
<td>The tilt of misaligned island nuclei with respect to the substrate surface</td>
</tr>
<tr>
<td>MBE</td>
<td>6H-SiC</td>
<td>Stacking mismatch boundaries</td>
<td>Substrate/buffer and buffer/film interfaces</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Steps on substrate Nonisomorphic with wurtzite GaN</td>
</tr>
</tbody>
</table>

Researchers have found many techniques to reduce the growth induced defects. Some of them are shown in table 2.7
Table 2.7: Improvement of crystal quality using insertion of interlayers by various research groups [77]

<table>
<thead>
<tr>
<th>Growth technique</th>
<th>Interlayer</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOVCD</td>
<td>2 buffer layer</td>
<td>Etch pits eradicated</td>
</tr>
<tr>
<td>MOVCD</td>
<td>5 interlayers</td>
<td>Threading dislocations reduced by 2 orders of magnitude</td>
</tr>
<tr>
<td>MBE</td>
<td>Double layer</td>
<td>Carrier mobility improved</td>
</tr>
<tr>
<td>MOCVD</td>
<td>$Si_xN_y$ interlayer</td>
<td>Reduction in threading dislocation</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Single interlayer</td>
<td>Threading dislocation reduced to $8 \times 10^7 cm^{-2}$</td>
</tr>
<tr>
<td>PA- MBE</td>
<td>Buffer layers were deposited at growth temperature (450 to 840°C) and thickness (4 to 30nm)</td>
<td>GaN film grown on a 15 nm-thick buffer grown at 525°C has a smooth surface (rms= 0.56nm) Relatively low total threading density ($5.8 \times 10^9 cm^{-2}$)</td>
</tr>
<tr>
<td>MOCVD</td>
<td>2- buffer layers (Mg_xN_y/AlN)</td>
<td>Exhibits smaller x-ray diffraction FWHM of peak Higher electron mobility, lower background concentration”</td>
</tr>
</tbody>
</table>
Chapter 3 Ion Implantation

3.1 Ion Implantation

Since more than thirty years ago, the method of ion implantation has been a prodigiously captivating and efficacious way in many applications, including ion cutting, electrical isolation, dry etching, doping of selective area, etc. of GaN-based devices fabrication [37]. Ion implantation is a doping technique where the high energy dopant ions are bombarded into the semiconductor lattice of the desired impurities (dopants). Ion Implantation techniques offers a huge benefit in both doping with the desired element and particular control over dopant concentration with a well-defined depth distribution. Nonetheless the process generates lattice disorder, the level of which be determined by on a variety of experimental parameters such as implantation temperature and ion Species [38, 39]. In GaN based devices, ion-cutting and wafer bonding of GaN-wafers can be achieved by ion implantation. Figure 3.1 shows an implanted GaN ion $2.6 \times 10^{17} \text{ H}^+/\text{cm}^2$ at 50 keV [78]

![Figure 3.1: As implanted GaN](image)

Figure 3.1: As implanted GaN [78]
The required doping used to be achieved before ion implantation technique was discovered was to diffuse the material into bulk silicon from gaseous source which was kept above the surface or pre-deposited chemical source on wafer surface [40]. This process of diffusion had lack of flexibility and needed a control which was required by device processing. When ion implantation was introduced using the dopant atom it got the popularity right away.

Implantation dose can be found by using this formula [40]

\[
Dose \, \varphi = \frac{\text{Ion Beam current in amps}}{\text{electron charge (q)}} \times (\text{implanted time}) \times \text{Ion beam scanning Area} \quad \ldots \ldots (3.1)
\]

Modern ion implanters use particle accelerator technology which has an energy span of 100eV to several MeV to overcome the coulomb’s barrier and can penetrate to a few nm’s to several microns in depth range [41]. Below table 3.1 shows some typical parameters for ion implantation process.

| Table 3.1: Typical parameters for ion implantation [35] [36] [37] |
|--------------------|-----------------|
| Ion source         | Si, S, Te, O    |
| Ion dopant         | Mg, Ca, Be, C   |
| Dose               | 10^{11}-10^{18} \text{ cm}^{-2} |
| Ion Energy         | 100eV to several MeV |
| Uniformity and reproducibility | +/-1% |
| Temperature        | room temperature |
| Ion flux           | 10^{12}-10^{14} \text{ cm}^{-2}\text{s}^{-1} |

Ionization energy of dopants in GaN is relatively massive and consequently high doses of dopants have to be introduced for engendering low resistive layers. When the
doping is carried out by ion implantation, it can create a heavily damaged or amorphous layer which is resulted from high-dose implantations. With a medium ion beam current of 1mA with a time of 10 seconds doses can create as low as \(10^{16}\) ions.cm\(^{-2}\) [40].

This process is done in high vacuum and hence it’s a very clean process step. In ion implantation beside the dose control, peak depth and spread range can also be controlled which is way better then diffusion process. The diffusivity of ion implanted species are extremely slow, hence the ion implantation process is preferred for GaN based device rather than diffusion process.

### 3.1.2 Ion implantation equipment:

The ion implantation setup extracts from the ion source and converts it into stream of ions then accelerates and focuses them as a beam [75]. This beam enters the mass analyzer for ion determination. The analyzer is usually sensitive enough to differentiate the adjacent mass numbers and the exit beam of desired implant ions is selected depending on the charge to mass ratio of the ions. Ions are then goes through a final acceleration because of which ion beam will be marginally electrostatically deflected and get separated from the neutral atoms which may have formed. Either with the help of electrostatically or mechanically or combination of both the beam is scanned on all over the wafer surface.

Moreover, an electron source may be close to the wafer to surge the surface with the electrons and from preventing a charge build up on insulating surfaces for example, Silicon oxide and silicon nitride. This charge is capable of failing the gate oxide because of electrical breakdown from gate to substrate through oxide. So this charge must be removed. Figure 3.2 shows a basic ion implanter system’s schematic diagram.
Figure 3.2: Schematic diagram of a medium current ion implanter [75]

Figure 3.2 shows a simplified schematic that demonstrates the significant components of medium-current (ion beam currents between 10 µA and ~2 mA) ion implanter. Some of the roles of various parts of this ion implanter are as follows:

1. **Ion source**: Operates comparatively in high voltage (25 Kv) which converts the electrically neutral dopant atoms into gas phase plasma ions and undesired species sources such as arsine, phosphine can be sputtered in ion sources.

2. **Mass Spectrometer**: A magnet bends the ion beam into a right angle and selects the desired impurity ion and removes undesired species. Only selected ions are passed through a slit or an aperture.

3. **High-Voltage Accelerator**: Add energy to beam up to 5 MeV and accelerates the ions to their final velocity. Both the accelerator column and the ion source are operated at a high voltage.

4. **Scanning system**: X and Y-axis deflection plated are used for scanning the beam all over the wafer for the formation of uniform implantation of desired dose.
Prevents the beam in such a way that neutral particles are prevented from hitting the target.

5. Target Chamber: The final destination for the beam current. Targeted surface is being penetrated. Have the facility to measure the ion current and implanted dopant.

3.2 Impurity distribution:

In ion implantation, all the ions navigate in random path to penetrate the target which causes losing some energy due to the nuclear and electronic property. As the doses used in implantation can be high as $10^{16}$ ions/cm$^3$ [65] [67], trajectories of the ions can be predicted with the help of statistical means. By putting together both lateral and vertical motions, the average total path length is determined which is called as range $R$. The projected range $R_p$ is the average depth of implanted ions and with the help of Gaussian the distribution of implanted ions about the depth can be approximated with straggle parameter $\sigma_p$ (or $\Delta R_p$). During the mask edge, the lateral motion of ions can be eliminated. The ion concentration $N(x)$, at depth $x$ is given by the formula,

$$N(x) = N_p \exp \left\{ -\frac{x-R_p}{2\sigma^2} \right\} - N_B \quad [66] \quad \ldots (3.2)$$

Where,

- $N_p$ is the peak concentration,
- $R_p$ is projected range
- $\sigma$ is straggle parameter
- $N_B$ is background concentration

If we have the total implanted dose as $\varphi$, and by integrating the above equation we get the expression for peak concentration $N_p$ which can be given as,
\[ N_p = \phi / \sqrt{2\pi \sigma_p} \] \[ (3.3) \]

There are lots of different distributions which have been employed to give more precise fit to moments of ion implantation which is possible using a Gaussian of which the most important is Pearson IV fit \[68\]. As an example, the fitted distributions for energies between 30 KeV and 800 KeV is compared for experimental boron profiles under non channeling conditions in the Figure given as,

![Figure 3.4: Boron implanted atom distribution \[68\]](image)

The boron profiles become more negatively skewed showed in Figure 3.4 and hence deviates more significantly from a typical Gaussian. For heavier ion such as arsenic, it has positive skewness for low energies which decreases very slow but can be
negative for some higher energy. Skewness nature can be elaborated by increased electronic stopping for faster moving ions.

### 3.2.1 Junction depth and sheet resistance

To understand a semiconductor device’s diffusion, activation and the dopant-point defect interaction it is necessary to achieve the required sheet resistance and junction depth.

Recalling the formula of impurity distribution from equation 3.2-

\[
N(x) = N_p \exp \left\{ \frac{x - R_p}{2\sigma^2} \right\} - N_B
\]

The junction depth \(X_j\) which is defined as the depth where the total concentration, corresponding to the sum of electrically and non-electrically active species atoms, can be valued from [80]

\[
X_j = R_p \pm \Delta R_p \sqrt{2\ln\left(\frac{N_p}{N_B}\right)} \quad \text{......... (3.4)}
\]

In this equation, \(N_p\) is the peak concentration, \(\Delta R_p\) is projected range, and \(\sigma\) is straggle parameter.

Figure 3.5 shows a comparison of apparent junction depth for various implantations conditions for a Si in a Mattson 3000 Plus RTP system which were configured with the Flash Anneal Controller (FAC) [85]. As it can be seen from the figure that for an \(^{11}\text{B}^+\) implant a dose of \(1 \times 10^{15}\ \text{cm}^{-2}\) with 500eV can achieve a junction depth of 280 Å as well as for \(^{49}\text{BF}_2^+\) with an implant a dose of \(1 \times 10^{15}\ \text{cm}^{-2}\) with 2200eV can achieve a junction depth of 185 Å.
Figure 3.5: Comparison of the apparent junction depth for various implantation conditions [85]

The overall ion implantation condition is shown in below Table 3.2

Table 3.2: Overall implantation condition for a Si in a Mattson 3000 Plus RTP system [85]

<table>
<thead>
<tr>
<th>Implant Species</th>
<th>Implant species</th>
<th>Dose (10^{15} \text{cm}^{-2})</th>
<th>(X_J) (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(^{11}\text{B}^+)</td>
<td>500</td>
<td>1</td>
<td>280</td>
</tr>
<tr>
<td>(^{11}\text{B}^+)</td>
<td>500</td>
<td>5</td>
<td>454</td>
</tr>
<tr>
<td>(^{49}\text{BF}_2^+)</td>
<td>1100</td>
<td>1</td>
<td>126</td>
</tr>
<tr>
<td>(^{49}\text{BF}_2^+)</td>
<td>2200</td>
<td>1</td>
<td>185</td>
</tr>
<tr>
<td>(^{49}\text{BF}_2^+)</td>
<td>2200</td>
<td>5</td>
<td>258</td>
</tr>
</tbody>
</table>

From Figure 3.6 [85], the sheet resistance can be seen for this experiment. an \(^{11}\text{B}^+\) implant a dose of \(1 \times 10^{15} \text{cm}^{-2}\) with 500eV achieved a sheet resistant of 10000 Ω per square cm as well as for \(^{49}\text{BF}_2^+\) with a same implant a dose with 2200eV can achieve a sheet resistant of 4000 Ω per square cm at a temperature of 600°C and only for 10s.
3.3 Annealing of dynamics

To trigger the implanted impurities in the samples subjected to ion implantation, annealing is a significant step. As there are defects because of using GaN, it has been considered that highly sufficient dynamic annealing is demonstrated in GaN in the process of ion implantation by Si with the ion energy of 90keV at the temperature of liquid nitrogen, which is also acknowledged as $LN_2$ [72]. To activate thermal annealing for a GaN semiconductor material, the temperature of thermal annealing need to be above the crystal formation temperature. Here the existence of crystal defects in the sample surface and the 2DEG surface is a concern.
Figure 3.7: Dose dependency for the displaced atomic density induced by 180 keV $Ca^+$ and 90 keV $Mg^+$ implantation in GaN at room temperature before (filled dots and triangles) and after (open dots and triangles) rapid thermal annealing at 1150°C for 15 s in flowing $N_2$ [72]

Figure 3.7 shows the displaced atomic density induced by 180 keV $Ca^+$ and 90 keV $Mg^+$ implantation in GaN at room temperature before (filled dots and triangles) and after (open dots and triangles) rapid thermal annealing at 1150°C for 15 s in flowing $N_2$ with respect to implanted ion dose. From this, it is seen that the displaced atomic density for $Ca^+$ is higher compared to $Mg^+$ with same implanted ion dose.

From Figure 3.8(a) and 3.8(b), it is displayed that in GaN, the profiles of damage and defects growth with increasing ion dose, analyzed by RBS/C spectra, stimulated by ion implantation with Au of 300 keV ion energy and $3.1 \times 10^{12}/cm^2.s$ beam flux at liquid nitrogen temperature ($LN_2$) and Au of 300 keV ion energy and $4.4 \times 10^{12}/cm^2.s$ beam flux at room temperature (RT) correspondingly [76].
Figure 3.8: Damage and defect profile in GaN induced by ion implantation of 300keV Au with $3.1 \times 10^{12}$/cm$^2$.s beam flux (a) $4.4 \times 10^{12}$/cm$^2$.s beam flux (b) at LN2 and RT correspondingly. Ion dose is characterized in unit of cm$^{-2}$ [76]

From these two Figures 3.8 (a) and (b), hugely colossal differences of damage and defects which can be found as ion dose growths in implantation at $LN_2$ and RT. At $LN_2$, most of the damage and defects accrue at the surface of GaN for ion dose not beyond $2 \times 10^{12}$/cm$^2$. For the meantime, the damage and defects in the bulk area of GaN, which is around 500A away the surface, increment exceedingly efficient between ion dose of $2 \times 10^{12}$/cm$^2$ and $3 \times 10^{12}$/cm$^2$.

Additionally, through the method of XTEM, it has been approved that amorphization is present when ion dose reaches a higher capability [78]. Damage and
defects in GaN growth at a more gradual speed in the bulk area as ion dose increases in compared to \( LN_2 \). In actual fact, damage and defects in bulk GaN reach a saturation level which is not beyond the capability of random amorphization is composed gradually from the surface of GaN.

In old traditions furnace annealing was used for annealing in which temperature of 600\(^\circ\)C and upwards for a time of few minutes to hours. After completing furnace annealing at 600\(^\circ\)C too it can leave some of the defects on the surface which needs a another higher temperature for annealing.

Annealing process called rapid thermal annealing (RTA) has been applied more recently in which arc and halogen lamps are used. This process is used for higher temperatures such as >1000\(^\circ\)C and for shorter anneal durations which is in seconds. Using the same RTA equipment Spike annealing is carried out which is applied to minimise the diffusion. The dwell time is zero at maximum temperature for spike annealing which uses rapid up and down rates. For example 200\(^\circ\)C and 70\(^\circ\)C are typical values.

### 3.4 Doping impurity distribution of ion implantation after annealing

Normally, the surface donors of GaN include Ge, Si and C occupying the place of Ga and Se, S and O occupying the place of N while the surface acceptors of GaN include Ca, Mg, Zn, Cd and Be occupying the site of Ga and Ge, Si and C occupying the site of N. Table 3.3 shows the properties of the main doping impurities of ion implantation after annealing into GaN [85].
Table 3.4: Properties of Doping Impurities in GaN [85]

<table>
<thead>
<tr>
<th>Donors</th>
<th>Max Available Doping concentration (cm$^{-3}$)</th>
<th>Coefficient of Diffusion (cm$^2$/s)</th>
<th>Ionization Energy (MeV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>$5 \times 10^{20}$</td>
<td>$&lt; 2 \times 10^{-13} (1500^0C)$</td>
<td>28</td>
</tr>
<tr>
<td>S</td>
<td>$5 \times 10^{18}$</td>
<td>$&lt; 2 \times 10^{-13} (1400^0C)$</td>
<td>48</td>
</tr>
<tr>
<td>Se</td>
<td>$2 \times 10^{18}$</td>
<td>$&lt; 2 \times 10^{-13} (1450^0C)$</td>
<td>--</td>
</tr>
<tr>
<td>Te</td>
<td>$1 \times 10^{18}$</td>
<td>$&lt; 2 \times 10^{-13} (1450^0C)$</td>
<td>50</td>
</tr>
<tr>
<td>O</td>
<td>$3 \times 10^{18}$</td>
<td>$&lt; 2 \times 10^{-13} (1200^0C)$</td>
<td>30</td>
</tr>
<tr>
<td>Acceptors</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mg</td>
<td>$\sim 5 \times 10^{18}$</td>
<td>$&lt; 2 \times 10^{-13} (1450^0C)$</td>
<td>170</td>
</tr>
<tr>
<td>Ca</td>
<td>$\sim 5 \times 10^{18}$</td>
<td>$&lt; 2 \times 10^{-13} (1450^0C)$</td>
<td>165</td>
</tr>
<tr>
<td>Be</td>
<td>$&lt; 5 \times 10^{17}$</td>
<td>Defect Assisted</td>
<td>--</td>
</tr>
<tr>
<td>C</td>
<td>N-type</td>
<td>$&lt; 2 \times 10^{-13} (1400^0C)$</td>
<td>--</td>
</tr>
</tbody>
</table>

For the impurity distribution, junction depth $X_j$ before annealing, recalling equation 3.4 [80]

$$X_j = R_p + \Delta R_p \sqrt{2 \ln \left( \frac{N_p}{N_B} \right)}$$

Where $N_p = \frac{\phi}{\sqrt{2\pi\sigma}}$ and $\Delta R_p = \sqrt{\sigma^2 + 2Dt}$

The impurity distribution after annealing [80] can be expressed as -

$$X_j = R_p + \sqrt{\sigma^2 + 2Dt} \sqrt{2 \ln \left( \frac{\phi/\sqrt{\sigma^2 + 2Dt \pi}}{N_B} \right)}$$

Where $\phi$ is the ion dose, D= Diffusion coefficient and t represents the time.

3.5 Fabrication

Silicon substrates are inexpensive, manageable wide widths and have decently defined electrical and thermal functionalities. Much of the exploration is focused around enhancement on sapphire and SiC as the substrate of GaN. Silicon in consideration as a substrate material for GaN development when the first Molecular Beam Epitaxy (MBE)
developed GaN LED on Si was exhibited in 1998 [82,83]. GaN growth on sapphire, SiC or Si utilizes a seed layer or buffer layer to provide accommodations to the lattice mismatch between the substrate and the epilayer.

There are standard operating procedures followed for fabricating a MESFET shown in Figure 3.9. The fabrication of MESFET starts with the inspection and cleaning of the wafer. Once Gallium Nitride cap is deposited by using reactive sputtering, a positive resist is used for the channel implantation. Then Deep etching of gallium nitride is done by alignment registration process and stripping and ashing is done on oxygen plasma. After that by using a positive resist source and drain are implanted by resist patterning.
This also resists the stripping and ashing of O₂ plasma. Using the rapid thermal annealing, ion implants should be annealed. Resist patterning for ohmic contact formations. Etching of gallium nitride is done for the formation of ohmic contacts. Depositing GaN metal for ohmic contacts to source and drain using d-beam evaporation and patterning by using process called liftoff technique. Thermal heating is done on ohmic contact.
Chapter 4 Basic Study on MESFET

4.1 Metal-Semiconductor Field Effect Transistor

A field effect transistor is a voltage operated device that can be used as in amplifier circuit or switching circuit [2-4]. Some major categorized of FETs are like junction-FET or simply JFET, metal oxide semiconductor-FET or simply MOSFET and another one is metal semiconductor-FET or simply MESFET. But there is some subtle limitation of JFET and MOSFET it forbade by MESFET from the semiconductor based research work. MESFET was first proposed and discovered by Mead in 1966. There are three types of metal-semiconductor contacts in MESFET. One of them is one Schottky barrier for the gate electrode. For GaN there is increase of Schottky barrier height which is denoted as $\chi_{GaN}$. There is potential form the Fermi energy to the peak of depletion layer forming energy. This barrier is given below in Fig.4.1.

![Figure 4.1 Metal –semiconductor Schottky barrier diagram [46].](image)

Here Schottky barrier is formed because of lightly doped of channel layer in close to depletion region.
Another type of metal-semiconductor contact is for the source electrodes. When metal and extrinsic semiconductors like n-type semiconductor are joined together then a potential imbalance is occurred in that contact of metal and extrinsic semiconductor. That contact is called ohmic contact. GaN is used as semiconducting material and metal is used as source electrode in Figure 4.2. Ohmic contact is formed where GaN is heavily doped.

![Energy Band Diagram](image)

**Figure 4.2: Metal (source) and Semiconductor (GaN) contact energy band diagram [47].**

Because of the imbalance of potential in between the material (\(\phi_M\)) and source (\(\phi_S\)) which can be expressed as \(\phi_M > \phi_S\), electrons will flow from source to GaN materials. And when, \(\phi_M < \phi_S\), it blocks electron flow and act as a fast switch. The last ohmic contact is used for the drain electrodes which are used in between the drain and GaN.

### 4.2 Types of MESFET

There are two types of MESFET. These are

i) Enhancement (Normally-off) mode MESFET

ii) Depletion (Normally-on) mode MESFET
4.2.1 Enhancement mode MESFET

Enhancement-mode MESFETs (E-MESFETs) are the common switching elements in FET based technology. These devices are OFF at zero gate–source voltage whether it can be turned ON by pulling the gate voltage in the direction of the drain voltage like $V_{DD}$ which is positive for n-doped logic and negative for p-doped logic family [48].

4.2.2 Depletion mode MESFET

Depletion-mode (D-MESFETs) the device is normally ON at zero gate–source voltage. Such devices are used as load resistors in logic circuits. For n-doped depletion-load devices, the threshold voltage might be negative so that it could be turned off. For p-doped gate voltage should be positive [48]. In Figure 4.3 a comparison between Depletion mode MESFET and Enhancement mode MESFET is shown with respect to drain to source current ($I_{ds}$) and gate to source voltage ($V_{gs}$).

![Figure 4.3: Comparison of Depletion and Enhancement mode MESFET [48]](image-url)
4.3 Basic Structure

The structure and band diagram of gate band energy in a MESFET device by GaN is shown in Figure 4.4. Here, $E_c$ is the energy in conduction band; $E_F$ is the energy in Fermi level; $E_c$ is the conduction band energy, $V_{bi}$ is the built in voltage and $\Phi_b$ is the barrier height.

![Figure 4.4: the structure and gate diagram of energy band in a MESFET device by GaN [49]](image)

The base material in MESFET is GaN substrate. The fabrication of GaN transistor where GaN can be grown in growth technique as stated earlier chapter 2 and a middle layer also grow in such a way to isolate the defects of the substrate from the transistor. Figure 3.3 shows the Schematic GaN based MESFET with gate, drain and source
The channel layer is a thin, lightly doped conducting layer to form a Schottky barrier contact in these regions. Since GaN has electron mobility which is 20 times greater than the hole mobility, the conducting channel must be doped by n-type materials. Then a layer with heavily doped ($n^+$) is grown on the surface to aid in the fabrication of low-resistance ohmic contacts and heavily doped layer will be etched away from the channel region [51, 52].

A renowned method like ion implantation may be used alternatively to create the n-channel and the highly doped ohmic contact regions directly in the semi-insulating substrate. The source and drain terminal where they are two ohmic contacts that are fabricated by mechanism of heavily doped and it should be made in such a way to provide access to the external circuit. Then Schottky barrier contact is fabricated between in between the ohmic contact of source and drain [53, 54].
4.4 Basic Operation of MESFET

The MESFET is generally a FET constructed by depositing metal over an FET structure to form metal-semiconductor Schottky barrier junction. MESFET is similar to conventional JFET where semiconductor-semiconductor junction is replaced by metal-semiconductor junction in MESFET. Here also gate to source should be maintained with negative bias and drain to source is biased with positive bias [8]. The drain is positive with respect to the source there drain current starts flowing from drain to source, and this develops a depletion region between the source and the drain as shown in Fig. 4.4. This is similar to conventional JFET where the depletion region formed under the drain and the source. The larger the drain voltage larger drain current will be flow through the channel then larger depletion region is formed under the drain. This larger depletion of charge will tend to pinch-off the channel and a condition arises where the drain current reaches a maximum [9-13].

The drain-current is also dependent on the gate-source reverse bias which also forms a depletion region between the gate and the source. The larger the reverse bias the larger the depletion region is formed and its effect in bringing a pinch-off in the channel which later becomes cut-off to stop the drain current flow [15].

Figure 4.6: Schematic diagram of MESFET [70].
4.5 Drain Characteristics Curve of MESFET

Figure 4.7 shows the drain characteristics of the MESFET. The device gives maximum current with $V_{GS} = 0V$ and gives close to zero drain current when the gate is biased to a large negative value [71].

![Drain Characteristics Curve of MESFET](image)

**Figure 4.7: $I_D$ Vs $V_{DS}$ characteristics of $V_{GS}$ for GaN MESFET [71]**

And oppositely it can be said if the $V_{GS} > 0V$ it will increase the drain current. The device with its micro-miniature structure and short channel length is highly suitable because short channel means lower possibility of scattering and reduced loss of carrier. Because of $V_{DS}$, the voltage across the depletion region is greater at the drain end than at the source end, so the depletion region becomes wider at the drain end. The reducing of the channel and the processing of the expanding of the $V_{DS}$, develop the electric field near the channel, making the electrons to move rapidly. The situation when $V_{GS} = V_p$, the voltage is squeeze off, the channel and the channel current is zero, paying small regard to the nature of $V_{DS}$. The voltage pinch off is determined by the active channel depth, as the depth of the active channel is to be constant throughout the process of fabrication it is situated to voltage breakdown and the pinch-off voltage [73-77]
As the Voltage is been further raised from drain to source ($V_{DS}$), as illustrated in Figure 4.8 (b), when the pinch off voltage is lesser than the voltage of gate to source ($V_{GS}$), there will be an increasing in the channel current, the region of the depletion gets deeper at the end of the drain, and the channel of the conductive gets narrower. The current should be steady throughout the channel. Therefore, if the conductive channel of the drain gets narrower, there will be rapid movement in the electrons [78-81].

As the $V_{DS}$ is above the value that creates the saturation of the velocity (normally just a tenths of volt), the concentration of the electrons other than the velocity should increase to attain the continuity of the current. Therefore, the region of accumulation of the electrons is formed nearby to the gate end. Therefore, as the electrons move throughout the channel and move at velocity into between the drain and the gate, a region of depletion of electrons formed. The depletion region is absolutely charged due to the
ions of the positive donor. If $V_{DS}$ increases, as shown in Figure 4.8(c), the more of the increasing of the voltage is dropped over the region to implement the electrons to cross it and the lesser is dropped over the channel which is the part of unsaturated. This attained region is known as charge domain. A situation is attained where the increasing in $V_{DS}$ is dropped completely over the charge domain, and there is no increase in the drain current.

### 4.6 Advantage of Choice of MESFET

MESFET shows some extraordinary electronic properties like high gain bandwidth, higher mobility of charge carrier, higher current, high switching speed. Also there are some advantages like

i) High carrier mobility then any discovered member of FET family.

ii) As there are two controlling parameter like $V_{GS}$ and $V_{DS}$ which individually creates depletion region and control the flow of drain current.

iii) As depletion region is formed and channel can be shortened so scattering of carrier is low.

iv) There is no creation of possibility of surface mobility.

v) Schottky barrier height does not depend only on gate so overall performance depends on source, drain also.

vi) As the GaN ensures higher amount of carrier mobility so in integration of using MESFET it will increase the carrier mobility than any other combination.
Chapter 5 GaN MESFET Theory

5.1 GaN MESFET Theory

In order to develop the channel current equation, the channel charge has been evaluated and the gradual channel approximation [61] has been adopted to find the channel current as:

\[ I_{ch} = g_0 \left\{ V_i - \frac{2}{3} \left( \frac{(V_i + V_{Bi} - V_{gs})^2 - (V_{Bi} - V_{gs})^2}{V_{po}} \right) \right\} \]  \hspace{1cm} (5.1)

Where, \( I_{ch} \) = channel current

\( V_i \) = voltage drop across the gate region,

\( V_{Bi} \) = Schottky barrier height,

\( V_{gs} \) = gate to source voltage,

\( V_{po} \) = the pinch-off voltage,

\( g_0 \) = channel conductance,

The channel conductance \( g_0 \) can be defined by the following equation as

\[ g_0 = \frac{q \mu N_D WA}{W_G} \]  \hspace{1cm} (5.2)

And \( V_{po} \) is the pinchoff voltage which is denoted as

\[ V_{po} = \frac{q N_D A^2}{2 \epsilon_0 \epsilon} \]  \hspace{1cm} (5.3)

Where, \( q \) = Electronic charge,

\( N_D \) = Doping density,
\( \epsilon_0 = \) Dielectric constant in vacuum

\( \epsilon = \) Permittivity for GaN,

\( A = \) Active channel thickness,

\( W = \) Gate width and

\( W_G = \) Gate length.

\[
\begin{align*}
\text{Figure 5.1: MESFET geometry [59]} \\
\end{align*}
\]

The Transconductance in the saturation region is equal to

\[
g_m \cong \frac{\partial I_{ch}}{\partial V_G} = g_0 \frac{(V_i + V_{BI} - V_{gs})^{\frac{1}{2}} - (V_{BI} - V_{gs})^{\frac{1}{2}}}{V_{po}^{\frac{1}{2}}} \tag{5.4}
\]

The drain-to-gate \( C_{dg} \) \([61]\) (the simplified equivalent circuit of a GaN MEESFET is shown in Figure 5.2) is given by,

\[
C_{gd} = \left( \frac{\partial Q}{\partial V_i} \right)_{V_G=\text{constant}} \tag{5.5}
\]

Finally the gate-drain capacitance can be expressed as
\[ C_{gd} = \frac{2\sqrt{2} WW_G(\varepsilon_0\varepsilon q N_D)^\frac{1}{2}}{AV_l^2} \left[ \frac{3}{2} V_l(V_l + V_{Bl-V_G})^\frac{1}{2} - (V_l + V_{Bl-V_G})^\frac{3}{2} - (V_{Bl} - V_G)^\frac{3}{2} \right] \]

(5.6)

Figure 5.2: Simple equivalent circuit of a GaN MESFET [61]

And the gate-to-source capacitances \( (C_{gs}) \) is implied by

\[ C_{gs} = \left( \frac{\partial Q}{\partial V_l} \right)_{V_l-V_G=constant} \]  

(5.7)

Consequently, the gate-source capacitance can be evaluated as

\[ C_{gs} = \frac{2\sqrt{2} WW_G(\varepsilon_0\varepsilon q N_D)^\frac{1}{2}}{AV_l^2} \left[ (V_l + V_{Bl-V_G})^\frac{3}{2} - (V_{Bl} - V_G)^\frac{3}{2} - \frac{3}{2} (V_{Bl} - V_G)^\frac{1}{2} \right] \]  

(5.8)

The cutoff frequency [61] has been calculated from the transconductance and gate capacitance and given below:

\[ f_T \approx \frac{1}{2\pi} \frac{g_m}{(C_{gs} + C_{dg})} \]  

(5.9)

For the case when \( C_{dg} \ll C_{gs} \), the value of \( f_T \) can be approximated as

\[ f_T \approx \frac{1}{2\pi} \frac{g_m}{C_{gs}} \]  

(5.10)
5.2 Calculating Intrinsic Carrier Concentration

Recalling from chapter 2, the intrinsic carrier concentration $n_i$ can be expressed by using the following equation [53]-

$$n_i = (N_C N_V)^{1/2} \exp(-E_g/(2k_B T)) \quad \ldots \ldots \quad (5.11)$$

Where $T$ is measured as degree kelvin, $k_B$ is Boltzmann constant valued as $8.6173 \times 10^{-5} \text{ eV K}^{-1}$ and $N_C$ is the effective density of states in the conduction band which can be valued by below equation:

For Zinc blende structure 

$$N_C \approx 4.82 \times 10^{15} \left(\frac{m_r}{m_o}\right)^{3/2} T^{3/2} \quad (cm^{-3})$$

$$\approx 2.3 \times 10^{14} T^{3/2} \quad (cm^{-3}) \quad \ldots \ldots \quad (5.12)$$

For 300 K, $N_C = 1.2 \times 10^{18} \quad (cm^{-3})$

For Wurtzite structure

$$N_C \approx 4.82 \times 10^{15} \left(\frac{m_r}{m_o}\right)^{3/2} T^{3/2} \quad (cm^{-3})$$

$$\approx 4.3 \times 10^{14} T^{3/2} \quad (cm^{-3}) \quad \ldots \ldots \quad (5.13)$$

For 300 K, $N_C = 2.2 \times 10^{18} \quad (cm^{-3})$

In equation 5.1, $N_V$ is the effective density of states in the Valance band which can be valued by below equation:

For Zinc blende structure

$$N_V = 8.0 \times 10^{15} T^{3/2} \quad (cm^{-3}) \quad \ldots \ldots \quad (5.14)$$

For 300 K, $N_V = 4.1 \times 10^{19} \quad (cm^{-3})$

For Wurtzite structure

$$N_V = 8.9 \times 10^{15} T^{3/2} \quad (cm^{-3}) \quad \ldots \ldots \quad (5.15)$$
For \( N_V = 4.6 \times 10^{19} \ (cm^{-3}) \)

These Values of \( N_C \) and \( N_V \) are used to calculate the value of intrinsic carrier concentration \( n_i \)

\[
n_i = (N_C N_V)^{1/2} \exp(-E_g / (2k_B T))
\]

For 300K and Zinc blende structure, \( E_g = 3.2 \) eV, \( n_i = 7.86 \times 10^{-9} \)

For 300K and Wurtzite structure, \( E_g = 3.39 \) eV. \( n_i = 2.95 \times 10^{-10} \)

Table 5.1 shows different values of \( n_i \) in different temperature for zinc blende and wurtzite crystal structure

**Table 5.1: Different values of intrinsic carrier concentration for different temperature**

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>Band-gap energy ( (E_g) ) (eV)</th>
<th>Intrinsic carrier concentration ( (n_i) ) ( (cm^{-3}) ) (Zinc Blende Crystal)</th>
<th>Intrinsic carrier concentration ( (n_i) ) ( (cm^{-3}) ) (Wurtzite Crystal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>3.39</td>
<td>7.86 \times 10^{-9}</td>
<td>2.95 \times 10^{-10}</td>
</tr>
<tr>
<td>400</td>
<td>3.29</td>
<td>7.51 \times 10^{-2}</td>
<td>2.61 \times 10^{-3}</td>
</tr>
<tr>
<td>500</td>
<td>3.24</td>
<td>0.7 \times 10^{3}</td>
<td>1.6 \times 10^{4}</td>
</tr>
<tr>
<td>600</td>
<td>3.18</td>
<td>1.005 \times 10^{6}</td>
<td>1.254 \times 10^{6}</td>
</tr>
<tr>
<td>700</td>
<td>3.11</td>
<td>2.032 \times 10^{8}</td>
<td>2.232 \times 10^{8}</td>
</tr>
<tr>
<td>800</td>
<td>3.04</td>
<td>1.003 \times 10^{10}</td>
<td>1.133 \times 10^{10}</td>
</tr>
</tbody>
</table>
Chapter 6 Results and Discussion

In order to determine the GaN based device performance, an analytical model of a GaN-based MESFET device has been developed. The physics based analytical model has been simulated by using MATLAB tool to study the channel current, transconductance, channel conductance, gate capacitance and frequency stated by the following results.

The Figure 6.1 presents the channel currents \( I_{ch} \) versus drain to source voltage \( V_{ds} \) for different gate voltage \( V_g \) = 0V, -10V and -20V with channel doping concentration \( N_d \) of 3x10\(^{17}\) cm\(^{-3}\), substrate doping \( N_a \) of 1x10\(^{15}\) cm\(^{-3}\), gate length \( W_g \) of 1x10\(^{-4}\) cm, device width \( W \) of 100x10\(^{-4}\) cm and active channel thickness \( A \) of 0.95x10\(^{-4}\) cm. The drain currents clearly show the linearity up to the approximate current level of 12.5A at \( V_{ds} = 50V \) and the currents show the non-linearity property upto \( V_{ds} = \)}
250V. All currents saturate beyond the $V_{ds} = 250V$. The drain current at $V_{ds} = 250V$ shows the device having excellent properties of high power aided efficiency. The linearity and non-linearity properties predict the device performance for high speed switching and high frequency applications. This plot has been computed by using the Equation 5.1.

![Transconductance Vs Gate-to-Source Voltage](image)

**Figure 6.2: Transconductance ($g_m$) vs. gate to source voltage ($V_{ds}$) with variation of gate length ($W_g$)**

Figure 6.2 display a graph for the transconductance($g_m$) versus gate-source voltage ($V_{gs}$) for different gate length of $W_g = 0.5 \times 10^{-4}$ cm, $1 \times 10^{-4}$ cm and $1.5 \times 10^{-4}$ cm with channel doping concentration ($N_d$) of $3 \times 10^{17}$ cm$^{-3}$, substrate doping ($N_a$) of $1 \times 10^{15}$ cm$^{-3}$, drain to source voltage of $V_{ds} = 125V$, device width ($W$) of $100 \times 10^{-4}$ cm and active channel thickness ($A$) of $0.9 \times 10^{-4}$ cm. The transconductance ($g_m$) for three gate length ($W_g$) shows a non-linear variation in the regime of non-linearity properties of drain-source voltage. The variation of transconductance ($g_m$) for gate length of $0.5 \times 10^{-4}$ cm
shows a significantly larger value compared to the gate length \(W_g\) of \(1 \times 10^{-4}\) cm and 
\(1.5 \times 10^{-4}\) cm for the gate-source voltage transition from -20V to 0V. The gate length \(W_g\) 
effect on transconductance \(g_m\) will be translated to the frequency response of GaN 
MESFET device. This plot has been created by using the Equation (5.4).

![Graph showing Gate to Drain Capacitance \(C_{gd}\) vs. Drain to Source Voltage \(V_{ds}\) for the variation of gate voltage \(V_{gs}\).]

The Figure 6.3 shows the result of a plot of gate to drain capacitance \(C_{gd}\) versus 
drain-source voltage \(V_{ds}\) for different gate voltages \(V_G\) of 0, -6, -12V with channel 
doping concentration \(N_D\) of \(1 \times 10^{17}\) cm\(^{-3}\), substrate doping concentration \(N_A\) of 
\(1 \times 10^{15}\) cm\(^{-3}\), channel length \(W_G\) of \(1.0 \times 10^{-4}\) cm, channel width \(W\) of \(100 \times 10^{-4}\) cm and 
channel thickness \(A\) of \(0.9 \times 10^{-4}\) cm. The drain-to-gate capacitances \(C_{dg}\) sharply 
decrease for the drain-source voltage transition from 1V to 2V and exponential drop of 
drain-to-gate capacitances \(C_{dg}\) has been observed at the drain-source voltage range of
2V to 10V. Finally the drain-to-gate capacitances ($C_{dg}$) start to saturate at the drain-to-source voltage ($V_{ds}$) range of 10V to 20V. The maximum drain-to-gate capacitances ($C_{dg}$) were found to be 0.32 pF, 0.5 pF and 0.64 pF for gate voltages ($V_G$) of 0, -6, -12V. This plot has been generated by using the equation 5.6.

![Figure 6.4: Gate to source capacitance ($C_{gs}$) vs. gate to source voltage ($V_{gs}$) for the variation of drain voltage ($V_{ds}$).](image)

The Figure 6.4 shows a plot of gate-source capacitance ($C_{gs}$) versus gate to source voltage ($V_{gs}$) for different drain to source voltages ($V_{ds}$) of 10, 20, 30V with channel doping concentration ($N_D$) of $1x10^{17}$ cm$^{-3}$, substrate doping concentration ($N_A$) of $1x10^{15}$ cm$^{-3}$, channel length ($W_G$) of $1x10^{-3}$ cm, channel width ($W$) of $100x10^{-4}$ cm and channel thickness ($A$) of $0.9x10^{-4}$ cm. The gate-source capacitances ($C_{gs}$) exponentially increase during the transition of gate-source voltage from -30V to 5V for various constant drain-source voltages. The maximum gate-source capacitances ($C_{gs}$) were found to be
7x10^{-2} \text{pF}, 4.8x10^{-2} \text{pF} \text{ and } 3.6x10^{-2} \text{pF} \text{ for drain-source voltages (}V_{ds}\text{) of 10, 20, and 30V respectively. The gate depletion region of depletion GaN MESFET significantly is reduced causing a rapid increase of the gate-source capacitances (}C_{gs}\text{). The gate-source capacitances (}C_{gs}\text{) are comparatively lower value compared to the gate-drain capacitances (}C_{gd}\text{). As a result, the gate-source capacitances (}C_{gs}\text{) intensively dominate the gate-drain capacitances (}C_{gd}\text{) to contribute the GaN MESFET device frequency performance stated in the next plot. This plot has been generated by using the equation 5.8.

![Gate Length Vs. Frequency Graph](image)

**Figure 6.5: Gate length (}W_g\text{) vs. cut-off frequency (}f_t\text{) for different gate to source voltage (}V_{gs}\text{)**

The Figure 6.5 exhibits a graph of cut-off frequency (}f_t\text{) versus gate length (}W_g\text{) for different gate-source voltage of }V_{gs}\text{ = -3V and -5V with channel doping concentration (}N_D\text{) of }1x10^{17}\text{cm}^{-3}\text{, substrate doping concentration (}N_A\text{) of }1x10^{15}\text{cm}^{-3}\text{, channel width (}W\text{) of }100x10^{-4}\text{ cm and channel thickness (}A\text{) of }0.8x10^{-4}\text{ cm. The cut-off frequency}
varies from 3.9THz to 2.25THz for the gate length change from $0.1 \times 10^{-4} \text{cm}$ to $1.1 \times 10^{-4} \text{cm}$ for the gate-source voltage of $V_{gs} = -3 \text{V}$. The cut-off frequency also changes from 250GHz to 100GHz for the gate length variation from $0.1 \times 10^{-4} \text{cm}$ to $1.1 \times 10^{-4} \text{cm}$ for the gate-source voltage of $V_{gs} = -5 \text{V}$. The maximum cut-off frequency is observed for the gate-source voltage of $V_{gs} = -3 \text{V}$ because the gate-source capacitance increases to the maximum value of $7 \times 10^{-2} \text{pF}$. Hence the contribution of gate-source capacitance dominates other parameters involved in the device frequency response. The gate length and GaN material parameters is also equally responsible for extreme high frequency performance. This plot has been generated by using the Equation 5.9
Chapter 7 Conclusion

A physics based analytical model of GaN MESFET has been developed by using Mat Lab to determine the I-V characteristics, transconductance, gate capacitance and cut-off frequency. The extracted large drain current shows the anticipated device potential for high power density and power added efficiency. The intrinsic parameters such gate-source capacitance, gate-drain capacitance and transconductance shows significant change with device potentials (gate-source voltage and drain-source voltage). The frequency response of GaN based MESFET shows the feasibility of developing THz device and the significant values of intrinsic parameters is attributed to achieve such frequency response. The nature of frequency response of the device shows the validity of one dimension modeling for submicron gate length and this research work is extremely important for high frequency device development for THz technology in military, space exploration and aerospace applications. The scope of this research is having tremendous potentiality for device design in order to develop GaN MESFET for terahertz technology.
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APPENDIX A

A  Active channel thickness
C_{dg}  Drain-to-gate capacitance
C_{gs}  Gate-to-source capacitance
C_s  Fringe capacitance
d_d  Depletion layer width
D_n  Diffusion constant
E  Electric field
E_b  Breakdown electric field
E_m  Maximum domain field
E_p  Electron peak velocity field
E_s  Domain sustain field
E_v  Electric field of the field electron drift velocity saturation
\epsilon_0\epsilon  Permittivity
f_T  Cutoff frequency
g_d  Channel conductance
g_m  Transconductance
\text{g}_m(\text{obs})  Observed value of the transconductance
I_{ch}  Channel current
I_D  Drain current
I_{sat}  Saturation current
I_{sub}  Substrate current
L_d  Debye length
\mu  Low-field mobility
N_D  Doping density
P  Power
Q  Total positive charge under the gate
Q_s  Stray charge
q  Electronic charge
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_D$</td>
<td>Drain-to-source section resistance</td>
</tr>
<tr>
<td>$R_{dc}$</td>
<td>Drain contact resistance</td>
</tr>
<tr>
<td>$R_D$</td>
<td>Gate-to-source section resistance</td>
</tr>
<tr>
<td>$R_{sc}$</td>
<td>Source contact resistance</td>
</tr>
<tr>
<td>$R_{sub}$</td>
<td>Substrate resistance</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Switching time</td>
</tr>
<tr>
<td>$\tau_m$</td>
<td>Dielectric relaxation time</td>
</tr>
<tr>
<td>$\tau_T$</td>
<td>Energy relaxation time</td>
</tr>
<tr>
<td>$V_{Bi}$</td>
<td>Built in voltage</td>
</tr>
<tr>
<td>$V_C$</td>
<td>Voltage drop across source-gate and gate-drain sections</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Drain voltage</td>
</tr>
<tr>
<td>$V_{dom}$</td>
<td>Domain voltage</td>
</tr>
<tr>
<td>$V_G$</td>
<td>Gate voltage</td>
</tr>
<tr>
<td>$V_i$</td>
<td>Voltage drop across the gate</td>
</tr>
<tr>
<td>$V_{po}$</td>
<td>Pinch-off voltage</td>
</tr>
<tr>
<td>$v_s$</td>
<td>Electron saturation drift velocity</td>
</tr>
<tr>
<td>$W$</td>
<td>Gate width</td>
</tr>
<tr>
<td>$W_G$</td>
<td>Gate length</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
</tbody>
</table>
APPENDIX B

Matlab code for channel current ($I_{ch}$) and Gate to source Voltage ($V_{gs}$)

```matlab
clc;  % clear the command window
clear all;  % clears all function variables, workspaces, etc
close all;  % close all open files
q = 1.6e-19;  % charge of an electron
e=8.85e-14;  % EPS=Eo*Es
epsilon = 8.9*e;
Nd =3.0e+17;  % donor concentration
Na = 1.0e+15;  % acceptor concentration
ni =1.9e-10;  % intrinsic concentration
u=500;  % mobility of an electron
w=100e-4;  % Gate width
wg=1*(10^-4);  % Gate length
A=0.95*(10^-4);  % Device thickness
Vds=0:5:250;  % Voltage drop across the gate, here Vi is Vds
Vbi=(0.0259)*log((Na*Nd)/(ni*ni));  % Built-in Voltage
Vgs=[-20 -10 5];  % Gate Voltage

for i = 1:51  % looping the values for Vds
    for m=1:3  % looping the values for Vgs
        j(i)=Vds(i)+Vbi-Vgs(m);
        Vp0 = ((q*Nd*A*A)/(2*epsilon))
        g0=(q*u*Nd*w*A)/wg;
        nume(m)=(2*((j(i)^1.5) - ((Vbi-Vgs(m))^1.5)));
        denom=(3*(Vp0^0.5));
        I(i,m)=g0*(Vds(i)-(nume(m)/denom));
    end
end
figure(1);
plot(Vds, I);
xlabel('Drain to source Voltage (Vds)'); ylabel('Channel Current(Ich) in A');
title(' Channel Current Vs. Drain Voltage');
hleg1 = legend( 'Vgs=-20v','Vgs=-10v','Vgs=5v');
```
Matlab code for plots Transconductance (Go) and Gate Voltage (Vgs)
% Transconductance Vs Gate Voltage
clc;
%clear the command window
clear all;
%clears all function variables, workspaces, etc
close all;
%close all open files
q = 1.6e-19;
% charge of an electron
e=8.85e-14;
% EPS=Eo*Es
epsilon = 8.9*e;
Nd = 1.0e+17;
% donor concentration
Na = 1.0e+15;
% acceptor concentration
ni =1.9e-10;
% intrinsic concentration
u=500;
% mobility of an electron
w=100e-4;
% Gate width
wg=[0.5 1 1.5]*10^-4
% Gate length
A=0.3*10^-4;
% Device thickness
Vds=125;
% Voltage drop across the Drain
Vbi= (0.0259) * (log((Na*Nd)/(ni*ni)));
% Built-in Voltage
Vgs=[-20 -18 -16 -14 -10 -8 -6 -4 -2 0];
% Gate Voltage

for i1=1:3
    for m=1:10
        j(m)=Vds+Vbi-Vgs(m);
        Vp0 = ((q*Nd*A*A)/(2*epsilon))
        g0=(q*u*Nd*w*A)/wg(i1);
        nume(m)=(((Vds+Vbi-Vgs(m))^0.5) - ((Vbi-Vgs(m))^0.5));
        denom=(Vp0^0.5);
        gm(m)=g0*(nume(m)/denom);
        end
        gm1(i1,:)=gm;
    end
    plot(Vgs, gm1(i1,:),'g');
    hold on
    plot(Vgs, gm1(2,:),'r');
    hold on
    plot(Vgs, gm1(3,:),'b');
    end
xlabel('Gate to source Voltage(Vgs) in V'); ylabel('Transconductance(Gm) in mho');
hleg1 = legend( 'Wg=0.5*10^-4', 'Wg=1*10^-4','Wg=1.5*10^-4');
title(' Transconductance Vs Gate Voltage');
Matlab Code for Gate-Drain Capacitance (Cgd) Vs Drain-to-Source Voltage (Vds)

clc; %clear the command window
clear all; %clears all function variables, workspaces, etc
close all; %close all open files
q=1.6e-19;
epi=8.85e-14;
epsilon=8.9*epei; % EPS=Eo*Es
Nd = 1.0e+17; % donor concentration
Na = 1.0e+15; % acceptor concentration
ni =1.9e-10; % intrinsic concentration
u=600; % mobility of an electron
w=100e-4; % Gate width
Wg=1*10^-4; % Gate length
A=0.9*10^-4; % Device thickness
Vi=0:1:20; %Vi=Vds
Vg=[0 -6 -12];
Vgs=[5 0 -5 -10 -15 -20 -30] % Gate Voltage
Vbi=(0.0259)*(log((Na*Nd)/(ni*ni))) % Built-in Voltage
for i = 1:21
    for m = 1:3
        j(i) = Vi (i) + Vbi-Vg(m);
        k(m)=((2*1.414)/3)*((w*Wg*(epeil*q*Nd)^0.5)/(Vi(i)));
        Vp0 = ((q*Nd*A*A)/(2*epeil))
        Cdg(i,m)=(k(m))*(1.5*(j(i)^0.5))
    end
end
Cgd=Cgd/10^12
figure(1);
plot(Vi,Cdg);
Matlab code for Gate-to-Source Voltage (Vgs) vs Gate-to-Source Capacitance (Cgs)

```matlab
% Gate-to-Source Voltage (Vgs) vs Gate-to-Source Capacitance (Cgs)*/
clc;                                               %clear the command window
clear all;                                         %clears all function variables, workspaces, etc
close all;                                         %close all open files
q = 1.6e-19;                                        % charge of an electron
e=8.85e-14;                                       % EPS=Eo*Es
Nd =3.0e+17;                                       % donor concentration
Na = 1.0e+15;                                      % acceptor concentration
ni =1.9e-10;                                       % intrinsic concentration
u=600;                                             % mobility of an electron
w=100e-4;                                          % Gate width
Wg=1*10^-4;                                        % Gate length
A=0.9*10^-4;                                       % Device thickness
Vds=0:1:30;                                         % Gate Voltage
Vgs=[5 0 -5 -10 -15 -20 -30];                     % Gate Voltage
V2i=[0 4 8 12 16 20 24];
V2g=[4 2 0 -2 -4 -6 -8 ];
Vbi=(0.0259)*(log((Na*Nd)/(ni*ni)))                     % Built-in Voltage
for i=1:3
    for m=1:7
        j2(i)=V2i(m)+Vbi-V2g(i);
        k(m)=((2*1.414)/3)*((w*Wg*(epsilon*q*Nd)^0.5)/(V2i(m)));  
        Vp0=((q*Nd*A*A)/(2*epsilon))
        Cgs(i,m)=(k(m))*((1.5*(j2(i)^0.5)-(1.5*(Vbi-V2g(i))^0.5)))/
    end
end
Cgs=Cgs/10^12;
figure(1);
plot(Vgs,Cgs);
xlabel ('Gate-to-Source Voltage(Vgs)'); ylabel ('Gate-to-Source Capacitance(Cgs) pF');
title ('Gate-to-Source Capacitance  Vs. Gate-to-Source Voltage');
hleg1 = legend ('Vds=10v','Vds=20v','Vds=30v')
```
Matlab code for plots Frequency (Ft) Vs Gate Length (Wg)

% Frequency (Ft) Vs Gate Length (Wg) with Cdg +Cgs

clc; %clear the command window
clear all; %clears all function variables, workspaces, etc
close all; % close all open files
q = 1.6e-19; % charge of an electron
e=8.85e-14; % EPS=Eo*Es
epsilon = 8.9*e;
Nd = 1.0e+17; % donor concentration
Na = 1.0e+15; % acceptor concentration
ni =1.9e-10; % intrinsic concentration
u=500; % mobility of an electron
w=100e-4; % Gate width
Wg=[ 0.1 1 ]*10^-4; % Gate length
A=8*10^-4; % Device thickness
Vgs= [-3 -5] % Gate Voltage
V2i=[4 8 12 16 20 24]; % Built-in Voltage
V2g=[4 2 0 -2 -4 -6 -8 ]; % Gate Voltage
Vbi=(0.0259)*(log((Na*Nd)/(ni*ni))); % Built-in Voltage
Vds=125; % Voltage drop across the gate, here Vi is Vds
for i=1:2
    for m=1:2
        j2(i)=V2i(m)+Vbi-V2g(i);
        k(m)=((2*1.414)/3)*((w*Wg(m))*(epsilon*q*Nd)^0.5)/(V2i(m));
        Vp0=((q*Nd*A*A)/(2*epsilon))
        Cgs(i,m)=(k(m))*((1.5*(j2(i)^1.5)-(1.5*(Vbi-V2g(i))^1.5)))
        Cdg(i,m)=(k(m))*((1.5*(j2(i)^0.5))
        g0(i)=(q*u*Nd*w*A)/Wg(i);
        nume(m)=(((Vds+Vbi-Vgs(m))^0.5) - ((Vbi-Vgs(m))^0.5));
        denom=(Vp0^0.5);
        gm(i,m)=g0(i)*(nume(m)/denom);
        Ft(i,m)=(gm(m)/(2*pi*(Cdg(i,m)+Cgs(i,m))));
    end
end
Ft=Ft/10^9;
figure(1);
plot(Wg,Ft);
xlabel ('Gate Length (Wg) in cm'); ylabel ('Frequency in GHz');
title ('Gate Legth Vs. Frequency');
hleg1 = legend ('Vgs=-3v', 'Vgs=-5v')