Analytical Model of GaN MESFET’s With Velocity Saturation and Negative Differential Resistance

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By

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ABSTRACT

Analytical Model of GaN MESFET’s With Velocity Saturation and Negative Differential Resistance

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Master of Science in Electrical Engineering

A physics based analytical model of GaN MESFET has been developed to study the negative differential resistance (NDR) effect on the carrier drift velocity and carrier mobility to promote the GaN MESFET device for high frequency range in order of terahertz (THz). The NDR effect on the drain-source current, transconductance and gate capacitance has been studied and the domain effect on electrical and intrinsic parameters has been considered to enhance the device frequency response. The domain formation in the channel MESFET has been determined by the electrical field distribution in the channel doping concentration.
CHAPTER 1: INTRODUCTION.

Gallium Nitride having a wide Band-Gap have recently gained interests because this material has thermal generation rate to be very low and breakdown field very high [1]. These properties make this material to have a potential impact on high power, high temperature and microwave applications. For military applications and aerospace applications, the use of Gallium Nitride based devices is efficient [2]. Moreover, Gallium Nitride (GaN) has huge thermal conductivity of 130 W/mk as compared to silicon (Si) which is 149 W/mk [3]. This makes it an advantageous material for high temperature devices. All the above discussed properties, makes GaN the best choice for highly efficient optoelectronic devices.

GaN is one of the wide band-gap energy materials (approx. 3.4 eV at 300K) as compared to other materials such as GaAs (1.42 eV) and Si (1.12 eV). GaN is a best material for making highly sensitive detectors in the UV range since these large band-gap semiconductors bring about less noise. There are numerous attributes available today that can impact performance in a high power and frequency device, however the five most prevailing qualities are conduction efficiency, switching efficiency, breakdown voltage, size and cost. These features determine power density and feasibly attainable system frequency [4]. The thermal conductivity (inverse of on-resistance) of GaN is 1.5, whereas 1.3 for Si and 4 for SiC. This factor is found as a function of material and breakdown voltage after adjusting GaN mobility.
In contrasted with Si, GaAs based gadget, GaN offers ten times higher electrical breakdown qualities, three times the Band-Gap, and extraordinary carrier mobility [5]. Some properties make GaN material more suitable than GaAs demonstrated in Figure 1.

![Figure 1: Schematic diagram on the advantage of GaN over GaAs [5]](image)

1.1 GaN MESFET Performance

GaN material shows fantastic material properties expressed in above area. GaN based gadgets display greatly exceptional execution in device particularly frequency and power application. A research on GaN MESFET device based device was conducted which show cutoff frequency of 900 MHz, delivering 51.1 W output power with 78% power added efficiency [6]. Also for another GaN MESFET device 10W output power with a PAE of 34% at $V_D = 48V$ with a cut off frequency of 700 MHz and maximum frequency of 1.8 GHz was achieved [7]. A 0.8µm x 150µm GaN MESFET has been reported where cut off frequency ($f_T$) of 6.5 GHz and maximum frequency ($f_{max}$) of 14GHz which are in close agreement with their measured values of 6 and 14 GHz using Voltera series
technique [8] where the 1-dB compression point and output-referred third-order intercept point are 16.3dBm and 22.2 dBm respectively with a constant channel temperature of 300K is assumed whereas some other researchers achieved cut off frequency ($f_T$) of 20 GHz and a maximum frequency ($f_{max}$) of 50 GHz [9]. Another GaN MESFET device has been fabricated where the device performance showed 2GHz cutoff frequency and Power density of 2.2 W/mm with an associated power added efficiency of 27% at $V_{ds} = 30V$ and $V_{gs} = -2V$ [10]. Another research investigated that the threshold voltage for GaN MESFETs ranged from 4 V to 20 V with maximum drain currents up to 300 mA/mm and trans conductance up to 60mS/mm which was measured for 100 µm wide devices having potential performance to high frequency application [11].

GaN MESFET offers decent device execution for the up and coming era of business utilization. Concurrently, a SiC MESFET carried on to mature in performance and manufacturing process stability. But now, GaN MESFET devices attain a power density of approximately 4.0 W/mm and power-added efficiencies greater than 50% on a regular basis. In some previous researches, devices with a source-drain spacing of 2.3 µm, a gate length of 0.3 µm, and a gate width of 2x50 µm were simulated where gate to source spacing was 1 µm which showed a cutoff frequency ($f_T$) of 11 GHz [12]. 1-dB minimum noise figure at maximum oscillation frequency of 36 GHz with an associated gain of 7.5 dB has been achieved by some other researcher [13]. Superior noise factor due to low carrier scattering and low radio frequency (RF) losses was grown from a 100-mm Si substrate GaN MESFET which also had showed high current density, high Trans
conductance, and high frequency performance (above 100 GHz) at the same time showed low dc-to-RF dispersion and low gate and drain leakage currents [14].

Researchers from University of Illinois [15] fabricated a GaN MESFET which demonstrated a power density of 2.2 W/mm with a power added efficiency of 27% at $V_{DS} = 30$ V and $V_{GS} = -2$ V at 2 GHz, the trans conductance $g_m$ was found 36 mS/mm and unity current gain cutoff frequency $f_T$ and maximum frequency of oscillation $f_{max}$ were measured to the value of 28 and 55 GHz which was at least two times the highest frequency data ever reported for GaN MESFETs.

In another research the power output was found to be 230W and cutoff frequency ($f_T$) of 30 GHz was obtained with 0.25 µm gate GaN MESFET [16]. Using drain current of 500 mA at $V_{DS} = 40$ V and $V_{GS} = 0$ V another GaN MESFET device was fabricated and this device showed cutoff frequency of 8 GHz, transconductance($g_m$) of 93mS/mm and a output power of 4W/mm with a power added efficiency of 50% and a gain 20dBm which was better than SiC MESFET simulation by the same researcher [17]. Some other researchers have fabricated a GaN MESFET device with $f_{max}$ is 15.6 GHz and is $f_T$ 7.2 GHz with a trans conductance of 164 mS/mm with a PAE of 38% at $V_{DS}= 3.5$ V [18]. For the non-surface-depleted GaN MESFET, it has been found that the maximum trans conductance($g_m$) and the maximum cutoff frequency are 244 mS/mm, 230 GHz, with a maximum output power of 2.66 W/mm [19].
Researchers from University of California Santa Barbara have fabricated AlGaN/GaN high electron mobility transistors (HEMT) which provided a current density of 850 mA/mm and trans conductance of 93 mS/mm under dc conditions [20]. The cutoff frequency ($f_T$) was 19 GHz and maximum frequency ($f_{max}$) of 46 GHz for this 0.7 µm gate length device. A research on 17% AlGaN mole fraction HEMT structure on semi-insulating SiC substrates was conducted which showed an output power of 103 W with a high power density of 5.2 W/mm and power added efficiency (PAE) of 35.3% [21]. Another research on AlGaN/GaN power HEMT in sapphire substrate achieved an output power densities of 1.1W/mm with PAE of 20.1% with a cutoff frequency ($f_T$) was 36 GHz and maximum frequency ($f_{max}$) of 70 GHz where gate-to-drain breakdown voltages up to 230V and channel currents >300mA/mm were obtained [22]. Some researchers obtained the trans conductance of 68mS/mm with maximum frequency of approximately 31 GHz and a cutoff frequency of 1.8 GHz with an RF power of 84 mW/mm and maximum drain to source current density is approximately 174 mA/mm for 1400 mm wide gate AlGaN/GaN HMET where $V_{gs} = -1.1V$ and $V_{ds} = 6V$ [23].

Some researchers fabricated AlGaN/GaN high electron mobility transistors (HEMTs) which shows 9.8 W/mm with a cut off frequency of 8 GHz [24]. A research showed an AlGaN/GaN-HEMT device in SiC Substrate that attained a DC trans conductance $g_m$ of 150 mS/mm with a cutoff frequency ($f_T$) of 25 GHz and maximum frequency ($f_{max}$) of 50 GHz with a saturated drain current ($I_d$) of 950 mA/mm from S-parameter measurements performed on a 100 µm HEMT. The GaN and its alloys are used for both optical and electronic applications because of the direct bandgap [25]. The bandgap of
GaN corresponds to a wavelength in the near ultra violet (UV) region of the optical spectrum at 300K as it has a bandgap of 3.44 eV at this temperature. Figure 2 shows a plot of the bandgap energy versus lattice constant in combination with the visible optical spectrum for various semiconductors including the wide-bandgap materials SiC, GaN and its alloys indium nitride (InN) and aluminum nitride (AlN) [26]. From the Figure 2, it can be observed that the AlxInyGa1-x-yN alloys cover bandgap energies from 1.9 eV to 6.2 eV, which correspond to wavelengths ranging from red to deep UV. GaN has several applications in the fields like Military, LASER, LED and Optical applications [27].

**Figure 2: Energy Band-Gap Vs Lattice Constant.**

The energy band versus lattice constant of Wide bandgap GaN shows a potential application of heterojunction. The material properties application to device has come in to observation because of its provision to blue and UV emitters and elevated temperature elevated power electronic apparatuses. GaN could act vital in achieving higher
frequencies and rapid provisions, for instance, in satellites and all electric airplane for its electronic mechanisms for example high power and high temperature tolerant heterojunction bipolar transistors (HBT's). GaN based field-effect transistors (FET’s) are projected to be highly useful for power amplification and switching in high temperature and high power environment. [28]
2.1 GaN Material

The GaN and GaN-based alloys are wide bandgap semiconductor materials, whose advancement offers the capacity to manufacture RF active devices. The High Electron Mobility Transistors (HEMTs) powered by AlGaN/GaN show extremely improved output power performance [29]. All the improved material properties like high electric breakdown field and high saturated electron drift velocity are the cause of the improved RF output power [30]. They even provide improved thermal conductivity when they are epitaxial grown on semi-insulating SiC substrates. The breakdown field of SIC and GaN is five to six times higher and this gives these materials more scope over Si and GaAs for RF power devices [31]. Though SiC is a wide bandgap material with a bandgap of 3.26eV, it undergo from poor electron transport properties and hence this hinders the use of SiC in very high frequency amplifiers. Also the substrate wafers are expensive, small and poor quality which again limits the use of SiC [32].

2.2. Energy band diagram for GaN.

The GaN energy band diagram is given by two crystal structures

1. Zn Blende crystal structure

2. Wurtzite crystal structure

2.2.1 Band structure of Zn Blende

Figure 3 shows the band structure of Zn Blende crystal structure of GaN. Here, four different types of energy are observed.
The energy bandgap $E_g$ in $\tau$-valley is found to be 3.2 eV which was measured from the conduction band minima and valance band maxima at k wave vector. Secondly, bandgap $E_X$ at X-valley in (100) orientation has a value of 4.6 eV. Another bandgap $E_L$ in the range of 4.8-5.1 eV is found for the energy in (111) orientation. The spin off band $E_{SO}$ in the valence band has a value of 0.02 eV.

2.2.2 Wurtzite crystal

Figure 4 shows the band structure of Wurtzite crystal structure of GaN. Various types of energy can be observed from the figure 4.

First, the energy bandgap in $\tau$- valley is $E_g$ which has a value of 3.39 eV. This value is measured from the conduction band minima and valance band maxima at k (wave vector). Secondly, the energy bandgap $E_A$ which has a value of 4.7 - 5.5 eV is defined as the energy separation at A-valley. Another energy bandgap $E_{M-L}$ which has value 4.5 –
5.3 eV is found for the energy separation at M-L valleys. The split off band $E_{SO}$ in the valence band has a value of 0.008 eV. And at last, the band energy $E_{cr}$ is defined as the energy of crystal field which has a value of 0.04 eV.

Figure 4: Band structure of Wurtzite crystal of GaN [33].
2.2.3. Temperature dependency on band-gap and excitation energy.

Temperature dependent Band-Gap energy can be calculated by the equations below.

The energy gap versus temperature:

\[ E_g = E_g (0) - 7.7 \times 10^{-4} x T^2 / (T + 600) \text{ eV} \quad (2.2.3) \]

\[ E_g (0) = 3.47 \text{ eV (wurtzite)} \quad (2.2.3 \text{ a}) \]

\[ E_g (0) = 3.28 \text{ eV (Zn blende)} \quad (2.2.3 \text{ b}) \]

It is found that

\[ E_g = E_g (0) - 9.39 \times 10^{-4} x T^2 / (T + 772) \quad (2.2.3 \text{ c}) \]

\[ E_g (0 \text{ K}) = 3.427 \text{ eV} \quad (2.2.3 \text{ d}) \]

Where \( T \) is temperature in degrees K.

2.2.4 Wurtzite structure of GaN: Band-Gap energy Versus Temperature

Temperature dependent energy bandgaps for the different temperatures have been presented below.
Figure 5: Wurtzite structure of GaN: Band-Gap and excitation energy Versus Temperature

The Figure 5 shows the plot for energy Band-Gap and excitation energy with respect to temperature variation for GaN Wurtzite structure. The temperature dependence equation can be derived by the following expression valid up to temperature less than 300 K

\[ E_g(T) - E_g(0) = -5.08 \times 10^{-4} \frac{T^2}{(996 - T)} \text{, (T in K).} \]  \[ (2.2.4\ a) \]

\[ E_g(300K) = 3.44 \text{ eV.} \]  \[ (2.2.4\ b) \]
The plot shown in Figure 6 was obtained by growing GaN samples on different substrates like SiC, sapphire to obtain energy Band-Gaps using different techniques. Experimental data are taken from different research works.

2.2.5 Zn blende of GaN in MgO substrate: Band-Gap Versus Temperature

Figure 7: Zn blende of GaN in MgO (1x1) substrate: Band-Gap energy Versus Temperature [35]
From the above Figure 7, it is observed that energy bandgap drops from 3.30eV to 3.23eV with the variation in temperature from $0^\circ K$ to $300^\circ K$ for a GaN Zn blend structure which is grown on MgO substrate.

### 2.2.6 Zn blende of GaN in Si substrate: Band-Gap energy Versus Temperature

![Zinc Blende](image)

**Figure 8: Zn blende of GaN in Si substrate: Band-Gap energy Vs Temperature [35]**

The plot in Figure 8 was obtained during GaN Zn blende structure grown on Si (100) substrate and energy Band-Gap was observed with the varying temperature [35]. The temperature dependences were obtained from pseudo dielectric-function spectrum using two different theoretical models.

### 2.3 Effective Density and \( n_i \) of GaN

The effective density of states in conduction band is given by the following equations

For wurzite crystal,

\[
N_c \approx 4.82 \times 10^{15} \cdot (m_l/m_0)^{3/2}T^{3/2} \ (cm^{-3}) \approx 4.3 \times 10^{14} \times T^{3/2} \ (cm^{-3}). \quad (2.3.a)
\]

For Zn blende crystal,
The effective density of states in the valence band is given by the following equations

For wurzite crystal,

\[N_v = 8.9 \times 10^{15} \times T^{3/2} \text{ (cm}^{-3}\text{)}. \quad (2.3.c)\]

For Zn blende crystal,

\[N_v = 8.0 \times 10^{15} \times T^{3/2} \text{ (cm}^{-3}\text{)}. \quad (2.3.d)\]

The intrinsic carrier concentration can be obtained using effective density of states in both conduction and valence band as shown in equation below (2.3.e).

\[n_i = (N_c \cdot N_v)^{1/2} \exp \left(-E_g/(2kBT)\right). \quad (2.3.e)\]

The Figure 9 shows the analysis of intrinsic carrier concentration plotted against varying temperature".

Figure 9: GaN, Wurtzite & Zn Blende structure: Intrinsic carrier concentration Vs temperature of [37]
2.4. Crystal structure of GaN

GaN appears in two types of crystal structure.

1) Wurtzite (WZ) Structure.

2) Znblende (ZB) Structure.

Wurtzite structure and Zn blende structure are very closely associated with crystallographic in many ways. The neighbor’s closeness are in the shape of tetrahedral. The Bravais lattice of Wurtzite assemblies are hexagonal and the axis perpendicular to the hexagons which is usually labeled as c-axis. The structure along the c-axis can be thought as a pre arrangement of the layer of atoms of the same element (e.g., all N or all Ga) erected from regular hexagons. For the Zn blende lattice the piling of the layers is [54]

For the Wurtzite structure lattice the piling of the layers is

\[ \ldots Ga_A N_A Ga_B N_B Ga_A N_A Ga_B N_B Ga_A N_A Ga_B N_B \ldots \]

For the Zn blende the stacking sequence is changed to [38]:

\[ \ldots Ga_A N_A Ga_B N_B Ga_C N_C Ga_A N_A Ga_B N_B Ga_C N_C \ldots \]

In Figure 10 shown below a stick and ball model of GaN is shown [39]. In this model the horizontal planes are the polar planes for GaN crystal, for Zn blende \{111\} and for wurtzite \{0001\} is the polar planes.
Figure 10: GaN Crystal planes in (a) Zn blende (b) Wurtzite [39]

Figure 11: GaN Wurzite structure.

The Figure 11 shows wurzite structure which is the most common crystal structure of GaN. The lattice stacking for wurzite structure is given by GaANAGaBNBGaCNCGaANAGaBNBGaCN. The space group of wurzite structure is
C₆v₄. Lattice constants a and b are equal (a=b) for the Wurtzite structure. There are Ga-atoms at (0, 0, 0) and at (2/3, 1/3, 1/2) and also there are N-atoms at (0, 0, u) and at (2/3, 1/3, ½+u). The value of ‘u’ is approximately 3/8. In fact for the value of u = 3/8, the nearest tetrahedral 6.

2.4.1 GaN Zn Blende structure.

Figure 12 shown below shows the Zn blende structure which differs a bit in stacking and it is given by: GaANAGaBNBGaANAGaBNBGaANAGaBN

![Figure 12: GaN Zn Blende structure.](image)

2.6. Transport and material properties of GaN.

Monte Carlo and Manual calculations simulations are used to study the transport properties of GaN, AlN and InN. The values shown in the Table 1 below represent calculated or theoretically predicted values. [40-42]
Table 1: Showing parameters of GaN, InN and AlN.

The information about parameters of GaN, AlN and InN are shown in Table 1. However, many of the parameters of these materials are still to be determined more precisely. Table 1 provides some important differences between GaN-based semiconductors and their more conventional counterparts like Si, Ge, III-V or II-VI compounds. The main
difference is the crystal symmetry. GaN based semiconductors have hexagonal (wurtzite) crystal structure and grow along the hexagonal (polar axis). This structure have a pronounced piezoelectric and pyroelectric properties that play a key role in the physics of GaN-based devices as shown in Figure 13.

Figure 13: Piezoelectric constant versus bond ionicity.

Another difference between these materials is a much larger polar optical photon energy (91.2meV for GaN compared to only 35meV for GaAs, for example). This large polar optical photon energy leads to a huge difference in polar optical scattering. The GaN and related compounds can be approximated by a two-step elastic process – first absorption and immediate emission of a high energy polar optical photon. Figure 14 shows the calculated Hall mobility in GaN versus temperature. As shown in the figure, the mobility
in GaN is quite high (than that for Si) and remains fairly high even at elevated temperatures [43].

**Figure 14:** Calculated Hall mobility in GaN versus temperature. Top curve is for \( n_s = 10^{13} \) cm\(^{-2}\) and bottom curve is for \( n_s = 5 \times 10^{12} \) cm\(^{-2}\).

It is seen that the electron velocity in GaN is very high and it remains to be high even at high temperatures. Fig. 15 compares the electron velocity for GaN which is computed using the Monte Carlo technique for different temperatures with that for GaAs [44].
Figure 15: (a) GaN and (b) GaAs: Velocity Vs Electric field Plots.

Figure 15 (b) was computed using the fit to the Monte Carlo calculations reported [45] for the following values of the low field mobility: 7,000 cm²/Vs at 300 K, 3,000 cm²/Vs at 500 K, and 1,100 cm²/V-s at 1,000 K. Figure 33 shows the velocity versus electric field dependences for GaN at different temperatures and doping levels calculated using the Monte Carlo technique [46]. Even at very high doping densities or at elevated temperatures, the predicted electron saturation velocity in GaN exceeds that in GaAs or in Si (which is about 105 m/s) by a factor of two or so which can be seen in the Figure 16.
Monte Carlo calculations show that overshoot effects in high electric fields may play a key role in GaN and as a result, the transit time in very small GaN devices may actually be shorter than for GaAs [45]. Another research compared the computed velocity of electrons injected with low velocities into a constant electric field region into GaN and GaAs. This result is important for short channel GaN devices.
The InN is expected to have better transport properties than GaN, including a much higher mobility (3,200 cm$^2$/Vs at room temperature), a higher peak velocity, and more pronounced overshoot and ballistic effects, as seen in Figure 18 and Figure 19.

Figure 18: Drift velocity of InN versus electric field at different doping levels.
Figure 19: Drift velocity of InN Vs electric field at different temperatures.

Doping concentration $N_d = 10^{17}$ cm$^{-3}$. T (K): 1 -150; 2 - 300; 3 - 500. However, InN is not available with desired device quality and the growth of InGaN with a high molar fraction of In presents a problem [47]. The electron velocity is quite high even in In-GaN alloys, in spite of strong alloy scattering as shown in Figure 20.

Figure 20: In$_x$Ga$_{1-x}$N: Drift velocity Vs electric field calculation by Monte Carlo technique
2.7. GaN Growth

GaN crystal can be developed by utilizing heteroepitaxial methodologies which involves a mixture of outside substrates, for example, Zn oxide, aluminum nitride, sapphire, silicon carbide, and silicon. The profit of utilizing sapphire, silicon carbide and silicon is that as they have close lattice constant, the lattice mismatch rate is low related to other substrate. Although there are lot of downsides for heteroepitaxial methodology like lattice mismatch, thermal expansion coefficient mismatch, mosaic crystal structure, biaxial induced stress, and wafer bowing which lessens the performance. To beat these shortcomings, extraordinary methods have been presented, for example, low temperature buffer technologies or epitaxial lateral overgrowth (ELOG) techniques which will give upgraded execution by removing the structural defects and requirement for low-temperature buffer layers by utilizing native substrates.

2.7.1 MOVPE Growth

Metal organic vapor phase Epitaxy (MOVPE) also known as metalorganic chemical vapor deposition (MOCVD) is a highly complex process for creating semiconductor multilayer structures by growing crystalline layers. It is a non-balance enlargement procedure that depends on vapor transport of the antecedents and resulting responses of alkyls of Group III and hydrides of Group V in a warmed zone and typically at condensed pressure. This strategy came to limelight since the research of Manasevit (1968) who showed that triethylgallium (TEGa) and arsine saved single GaAs pyrolytically in an open tube which was in low temperature divider reactor. The essential MOVPE process for creation of GaN is:

\[
Ga(CH_3)_3 (V) + NH_3(V) \rightarrow GaN (S) + 3 CH_4 (V) \quad [48] \quad (2.7.1)
\]
In Figure 21, approach of MOCVD process is shown.

2.7.2 Molecular Beam Epitaxy (MBE):

Molecular beam epitaxy is the technique for epitaxial growth with the association of one or several molecular beams that occurs on a surface of a heated crystalline substrate.

Figure 22: A MBE system [50]
The strong sources materials are put in effusion cells to give an angular distribution of particles or atoms in a beam. The substrate is warmed to the necessary temperature and, when required, continuously rotated to enhance the development homogeneousness.

MBE gives special ability to study crystal growth in real-time and on a sub-nanometer scale. For having a development rate of a few Å/s, required need of ultra-high vacuum and for being expensive, it is not that popular kind of development methodology to the specialists.

2.7.3 Hydride vapor phase epitaxy

The Hydride vapor phase epitaxy (HVPE) is the most widespread growth process used to grow thick, strain relieved buffer layer.

![Figure 23: HVPE process for GaN [51]](image)

The HVPE related equations are:

For 700-900°C \[ Ga + HCl \rightarrow GaCl + \frac{1}{2}H_2 \] [51]… …… (2.7.3 a)

For 900-1100°C \[ GaCl + NH_3 \rightarrow GaN + HCl + H_2 \] [51]…… …… (2.7.3 b)
\[ \text{GaN} \leftrightarrow \text{Ga} + \frac{1}{2} \text{N}_2 \] ....... (2.7.3)

c) 

\[ \text{Ga} + \text{NH}_3 \leftrightarrow \text{GaN} + \frac{3}{2} \text{H}_2 \] .................. (2.7.3 d)

2.8 Substrate used for GaN

Many substrates such as Sapphire, SiC, Si, \( \text{ZrB}_2 \), MgO, GaN, AlN, LiAlO\(_2\) and others are used for GaN.

![Substrates comparison for GaN](image)

**Figure 24: Substrates comparison for GaN [52]**

From the Figure 24 it can be seen that GaN/6H-SiC have very close lattice match and bandgap is almost equal to each other. For GaN and Sapphire lattice mismatch is only 14\% and for GaN and Si has only 17\% of lattice mismatch.

In many situations including lattice coincidence, lattice matching, thermal expansion coefficient (TEC), temperature stability, conductivity, availability, and price are given thought before picking a substrate. Ordinarily sapphire is used as it has improved quality in many cases, high thermal resistance, available up to inches in diameter and most importantly it is economical than any other substrate [52].
Another very favorable substrate for the growth of GaN layer is Si which allows future incorporation of well-established Si centered electronics with GaN-based photonic devices. There are many advantages of using Si as substrate in GaN layer, such as high quality, large size, low cost and thermal stability at high growth temperature. But, the growth of GaN on Si substrate with crystalline quality compared to GaN grown on sapphire is still difficult as there is a large mismatch in relevant lattice parameters and large difference in thermal expansion coefficient between GaN and Si [52-54].

<table>
<thead>
<tr>
<th>Material</th>
<th>Crystal structure</th>
<th>Lattice Constant (Å)</th>
<th>Thermal mismatch (10⁻⁶/K)</th>
<th>Lattice mismatch %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>(a)</td>
<td>(c)</td>
<td>(a)</td>
</tr>
<tr>
<td>GaN</td>
<td>Hexagonal</td>
<td>3.18</td>
<td>5.18</td>
<td>5.59</td>
</tr>
<tr>
<td>AlN</td>
<td>Hexagonal</td>
<td>3.104</td>
<td>4.966</td>
<td>4.2</td>
</tr>
<tr>
<td>Si</td>
<td>Diamond</td>
<td>5.43</td>
<td>5.42</td>
<td>3.59</td>
</tr>
<tr>
<td>Sapphire</td>
<td>Hexagonal</td>
<td>4.758</td>
<td>12.99</td>
<td>7.5</td>
</tr>
</tbody>
</table>

Table 2: Fundamental properties of materials involved in GaN growth [52]

The principal trouble, which really deflects direct development of GaN on Si surfaces, is the poor nucleation of GaN on Si, which prompts an island-like GaN structure. With a specific end goal to vanquish this trouble, an AlN buffer layer or transitional layer, developed before GaN development, is normally utilized. It has been accounted for that the nature of buffer layer assumes an essential part in the thick GaN development [54].

2.9. Defects in GaN.

The applications of Gallium nitride (GaN) and pairs InN and AlN have given them several importance. The lattice structures involved in the GaN causes it to have several
defects when compared to others. The electrical and optical properties of the primary material involved are affected due to these defects. The functionalities of the materials is affected because the defects involve the isolated and the several intentional defects [55].

2.9.1. Defects in Native Point

These defects present in the materials will affect the optical properties and electrical properties of these materials. These defects also cause annealing in the materials. Vacancies, interstitials, and antisites are the different forms these defects can take. The interaction of isolated native defects causes the formation of complex defects. Figure 25 shows the energy formation at the different levels of the formation energy (eV) [56].

![Figure 25: Formation of Energies at Fermi Level for Native Point Defects.](image)

2.9.2. Antisite and Interstitial Defects

The minor cross section consistent in GaN and the expansive size between Ga and N molecules cause imperfections regularly. Under certain conditions some of the
imperfections might shape yet in extremely little focuses on the other hand. Development of energies of the Ga interstitial (GaN) and huge cross section relaxations are expedited by the imposing size of the Ga particles. Large portability of GaN even at room temperature intimates that GaN is trapped by some different deformities and does not exist in GaN as a confined negative aspect in equilibrium [57].

2.10. Why Si/SiC/Sapphire used for Substrate of GaN Devices.

Electrical and thermal functionalities are recently described in Silicon substrates and also they are less expensive, accessible in expansive widths. The improvement of sapphire and SiC is the center of this stage of exploration. The first MBE developed GaN LED on Si in 1998 showed that silicon can be a considered as a substrate material for GaN development [57-59]. A seed layer or buffer layer to accommodate the lattice mismatch between the substrate and the epilayer is used for the GaN growth on sapphire, SiC or Si. The 6H–SiC, 4H–SiC and 3C–SiC substrates for GaN growth has the effect of surface pre-treatment by exposure and has been studied. The increase in peak are indicated by the Photoluminescence spectra of the pictures developed on Si. In the recent couple of years, serious researches have been done around there and even from an optimistic GaN layers on Si are very nearly similar to GaN layers on SiC.

The deposited GaN film was found to be polycrystalline, after the nitration of Silicon carbide. The development of the seed layer will bring about non-stoichiometric synthesis at flat temperatures and additionally processes a heightened thickness of defects in the structure, along these variations. This also brings down the restraint between Silicon/AlN interfaces. The least resistance utilizing a flat level temperature has been indicated in LEDs of GaN on Silicon [59].
CHAPTER 3: Fabrication of GaN

3.1 GaN MESFET Fabrication.

For the process of fabrication, a gold germanium –nickel metallization is used. Due to the deposition of the aluminum, the Schottky Gate is formed, the ohmic contacts for source and drain region are formed due to the metallization. A thicker metal pad is formed due to the aluminum deposition which is suitable for probing. The E-Beam evaporation method is used for metal deposition in layers and this layer is defined by the liftoff process.

The figure below shows the manufacturing of GaN MESFET

![Figure 26: GaN MESFET fabrication process.](image-url)
Steps followed during fabrication are summarized below.

- First, we have to clean the wafer.
- By the method of reactive sputtering, a 100nm thick silicon nitride cap is deposited.
- For patterning of channel implant, a positive resist thickness of 1.6μ is used.
- The parameters of silicon ion implantation of the device channel are specified as: Maximum ion energy is 180KeV and Ion species is Si\(^{+}\) (singly ionized) and Dose is 5 x 10\(^{12}\).
- For aligning registration purpose using buffered HF solution and plasma etching, Shallow etching of silicon nitride is done.
- Resist stripping and ashing of the above product is done in oxygen plasma.
- Further Resist patterning for source or drain implant is done using resist (positive).
- The device goes through a silicon ion implantation in source and drain regions.
- A 200KeV of ion energy taken is and this is the maximum.
- Si\(^{+}\) is the chosen ion species and it is ionized singly.
- A 1 x 10\(^{13}\) cm\(^{-2}\) of ion dose is used.
- Annealing is the next step further ion implantation and the method used is rapid furnace annealing and the maximum temperature chosen during annealing is 850\(^{0}\) C and the annealing time is 80 to 120 seconds.
- Resist patterning is done later for ohmic contact formations and target resist has a thickness of 0.8μm also Silicon nitride etching is done for ohmic contacts.
- The next step is doing CF\(_4\) plasma etching to semiconductor surface and 50% HCl
is used for final wet etch cleaning of exposed GaN surface.

- Further above step AuGe/Ni metal is deposited for ohmic contacts to source and drain using e-beam evaporation and patterning by liftoff technique.
- Ohmic contact form alloys when rapid thermal heating and maximum temperature chosen is in the range of 475-500°C and time taken is 120 seconds. And then Resist patterning for nitride etch is performed for forming Schottky gate.

3.1.1. Substrate Used for Fabrication of GaN MESFET

Years ago, researchers have shown us that GaN material with silicon has less importance in comparison with the materials such as silicon carbide with sapphire due to thermal non equality between GaN and Si. The GaN layer built on Si has a tension while cooling from the growth temperature to room temperature. The thickness of the GaN MESFET on the silicon wafer is less compared to the sapphire. This is caused because of the formation of the epitaxial layer on the Silicon. During this study the total grown layer thickness was designed to be 1.5μm in order to avoid the formation of cracks and to obtain a mirror-like surface morphology. The device isolation was accomplished by mesa dry etching down to the I-GaN layer by reactive ion etching (RIE) in a BCl$_3$ plasma at an RF power of 10W and a chamber pressure of 3Pa. Making note of its points of interest, for example its utilize as a substrate for heteroepitaxial development of Gallium nitride based materials, Silicon is needed to be an preferable material for heightened power Gallium nitride based materials.

The development of GaN MESFETs on Sb-doped, 0.015 -cm resistivity n-sort Si (111) substrates was completed in a Nippon Sanso MOCVD framework (SR-2000). The reactant species utilized were trimethylgallium (TMG), trimethylaluminum (TMA), and
NH\textsubscript{3} with H\textsubscript{2} as the gas for carrier. Monosilane (SiH\textsubscript{4}) dissolved in H\textsubscript{2} (10ppm) was utilized as the dopant of the n-sort. The substrates were ready by in solvents, emulated by a 5min engraving in H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}S\textsubscript{0}\textsubscript{4} (1:4) and a 1 min carve in HF: DI H\textsubscript{2}O (1:10). A 80nm thick of AlN nucleation layer was developed at 1100\textsuperscript{0} C, accompanied by a 0.25μm thick i-Al\textsubscript{0.27}G\textsubscript{0.73}N layer at 1080\textdegree C, a 0.8μm-thick of GaN layer at 1080\textdegree C and a 0.2μm thick of n-GaN layer with Silicon doped to a value of 2 x 10\textsuperscript{17} cm\textsuperscript{3} at 1080\textdegree C. For the development of the I-AlN layer, the stream rates of the NH\textsubscript{3} and TMA were 51/min and 6.1μmol/min, individually. The stream rates of the trimethylgallium (TMG) and trimethylaluminum (TMA) were 13.9μmol/min and 6.1μmol/min, separately, for the development of the component of the I-Al\textsubscript{0.27}G\textsubscript{0.73}N layer.

3.2 Ion Implantation

Since more than thirty years ago, the method of ion implantation has been a prodigiously captivating and efficacious way in many applications, including ion cutting, electrical isolation, dry etching, doping of selective area, etc. of GaN-based devices fabrication [37]. Ion implantation is a doping technique where the high energy dopant ions are bombarded into the semiconductor lattice of the desired impurities (dopants). Ion Implantation techniques offers a huge benefit in both doping with the desired element and particular control over dopant concentration with a well-defined depth distribution. Nonetheless the process generates lattice disorder, the level of which be determined by on a variety of experimental parameters such as implantation temperature and ion Species [38, 39]. In GaN based devices, ion-cutting and wafer bonding of GaN-wafers can be achieved by ion implantation. Figure 27 shows an implanted GaN ion $2.6 \times 10^{17}$ H\textsuperscript{+}/cm\textsuperscript{2} at 50 keV.
The required doping used to be achieved before ion implantation technique was discovered was to diffuse the material into bulk silicon from gaseous source which was kept above the surface or pre-deposited chemical source on wafer surface. This process of diffusion had lack of flexibility and needed a control which was required by device processing. When ion implantation was introduced using the dopant atom it got the popularity right away.

Modern ion implanters use particle accelerator technology which has an energy span of 100eV to several MeV to overcome the coulomb’s barrier and can penetrate to a few nm’s to several microns in depth range. Below table 3 shows some typical parameters for ion implantation process.

<table>
<thead>
<tr>
<th>Source of Ion</th>
<th>Te, O, Si, S</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dopant of Ion</td>
<td>Be, C, Mg, Ca</td>
</tr>
<tr>
<td>Dose</td>
<td>$10^{11}$-$10^{18}\text{ cm}^{-2}$</td>
</tr>
<tr>
<td>Ion Energy</td>
<td>100eV to several MeV</td>
</tr>
<tr>
<td>-------------------------</td>
<td>----------------------</td>
</tr>
<tr>
<td>Uniformity and reproducibility</td>
<td>+-1%</td>
</tr>
<tr>
<td>Temperature</td>
<td>Room temperature</td>
</tr>
<tr>
<td>Ion flux</td>
<td>$10^{12}$-$10^{14}$ cm$^2$s$^{-1}$</td>
</tr>
</tbody>
</table>

**Table 3: Typical parameters for ion implantation**

### 3.2.1 Equipment used in Ion implantation

The ion implantation setup extracts from the ion source and converts it into stream of ions then accelerates and focuses them as a beam. This beam enters the mass analyzer for ion determination. The analyzer is usually sensitive enough to differentiate the adjacent mass numbers and the exit beam of desired implant ions is selected depending on the charge to mass ratio of the ions. Ions are then goes through a final acceleration because of which ion beam will be marginally electrostatically deflected and get separated from the neutral atoms which may have formed. Either with the help of electrostatically or mechanically or combination of both the beam is scanned on all over the wafer surface.

Moreover, an electron source may be close to the wafer to surge the surface with the electrons and from preventing a charge build up on insulating surfaces for example, Silicon oxide and silicon nitride. This charge is capable of failing the gate oxide because of electrical breakdown from gate to substrate through oxide. So this charge must be removed. Figure 28 shows a basic ion implanter system’s schematic diagram.
Figure 28: Schematic diagram of a medium current ion implanter

Figure 29 shows a simplified schematic that demonstrates the significant components of medium-current (ion beam currents between 10 µA and ~2 mA) ion implanter. Some of the roles of various parts of this ion implanter are as follows:

1. **Ion source**: Operates comparatively in high voltage (25 Kv) which converts the electrically neutral dopant atoms into gas phase plasma ions and undesired species sources such as arsine, phosphine can be sputtered in ion sources.

2. **Mass Spectrometer**: A magnet bends the ion beam into a right angle and selects the desired impurity ion and removes undesired species. Only selected ions are passed through a slit or an aperture.

3. **High-Voltage Accelerator**: Add energy to beam up to 5 MeV and accelerates the ions to their final velocity. Both the accelerator column and the ion source are operated at a high voltage.
4. **Scanning system:** X and Y-axis deflection plated are used for scanning the beam all over the wafer for the formation of uniform implantation of desired dose. Prevents the beam in such a way that neutral particles are prevented from hitting the target.

5. **Target Chamber:** The final destination for the beam current. Targeted surface is being penetrated. Have the facility to measure the ion current and implanted dopant.

Ionization energy of dopants in GaN is relatively massive and consequently high doses of dopants have to be introduced for engendering low resistive layers. When the doping is carried out by ion implantation, it can create a heavily damaged or amorphous layer which is resulted from high-dose implantations. With a medium ion beam current of 1mA with a time of 10 seconds doses can create as low as $10^{16}$ ions.cm$^{-2}$.

This process is done in high vacuum and hence it’s a very clean process step. In ion implantation beside the dose control, peak depth and spread range can also be controlled which is way better then diffusion process. The diffusivity of ion implanted species are extremely slow, hence the ion implantation process is preferred for GaN based device rather than diffusion process.

An analytic description of an ion-implanted MESFET based on the assumption of a resultant Gaussian profile (described by $R_p$, and $\sigma$) and the total implanted dose $Q$ is considered to develop an expression for presenting the impurity distribution as sown in equation 3.2.1.

\[
N(x) = N_p \exp \left[ \frac{-(x-R_p)^2}{2(\Delta R_p^2)} \right] - N_B
\]

(3.2.1)
Where \[ N_p = \frac{Q}{\Delta R_p \sqrt{2\pi}} \]  \hspace{1cm} (3.2.2)

Implantation dose can be found by using this formula

\[ Dose \ \varphi = \frac{(<\text{Ion Beam current in amps per electron charge (q)}) \times (\text{implanted time})}{\text{Ion beam scanning Area}} \]  \hspace{1cm} (3.2.3)

Rp= Range parameter.

Q= Ion dose.

Xj= junction depth and it is given by the equation.

\[ x_j = R_p \pm \Delta R_p \sqrt{2ln\left(\frac{N_p}{N_B}\right)}. \]  \hspace{1cm} (3.2.4)

Figure 29: Junction Depth and Range Parameter

R_p ... Mean projected range

X_j ... Junction depth
Ion implantation of phosphorus ions in GaN at room temperatures, followed by annealing at about 1900° C were adopted for ion implantation in GaN to produce junction diodes. A setup of ion implantation process is shown in Figure 30.

![Ion Implantation Setup](image)

**Figure 30: Industry Setup of Ion Implantation process.**

From the above ion implantation setup boron, aluminum, gallium, and thallium can be implanted at room temperature in an attempt to obtain p-type conductivity. Until now there is no successful technique for ion implantation of both donor and acceptor dopant ions into mono crystalline SiC/GaN which results in appropriately electrically activated n and p-type materials. The flow chart of ion implantation process in as shown in Figure below.
3.3 Annealing

Further ion implantation process the resistivity in GaN device gradually increases due to the damage occurred in the device which has deep level holes and electrons which restricts the free flow of carriers in the channel of the device. Due to the huge bombardment of implanted ions, the lattice of host atoms became damaged due to the formation of random pattern causing amorphous crystal. The carrier mobility became degraded to change the sheet resistance. In order to restore the damage in the crystal structure, the annealing process is required.

The impurity distribution equation after annealing is given by
Where,

\[ n(x, t) = \frac{Q_T}{\sqrt{2\pi} \sqrt{\Delta R_p^2 + 2Dt}} \exp \left[ -\frac{(x-R_p)^2}{2(\Delta R_p^2 + 2Dt)} \right] \]

(3.5)

Q_T = Ion dose.

R_p = Range parameter.

D = Diffusion constant.

t = Time.

3.3.1 Impurity distribution after Annealing

After implantation during the use of high temperatures in further steps, the implanted impurities will diffuse, which widens the implantation profile as shown in the figure 32 and also form the final junction depth.

Figure 32: Impurity distributions after Annealing.
4.1. Physical structure of GaN.

Figure 33 shows the cross-sectional area of GaN MESFET

![Cross-section of GaN MESFET](image)

Figure 33: Cross-section of GaN MESFET.

The substrate of the semi-isolating silicon has a layer of GaN n-type is put away on it. A metal Au/Ge blend is utilized as a part of the substrate. This is regularly joined with the source terminal all through estimations. The n+ ohmic contacts joins the mix of source and the drain with the layer of the n-type. Aluminum covered with Au ordinarily is the metal which structures the gate. This is stored on top of the n-type layer in the middle of drain and source. A Schottky barrier junction is structured by the metal semiconductor intersection of the gate. The stature of the channel of the dynamic layer underneath is controlled by using this intersection by applying a voltage of the predisposition at the gate. In light of the inclination, the area underneath the gate is charged [60].

The length of gate (L), width (W) and depth of the active channel are the most extents of
a MESFET materials. The mechanism is portrayed by these sizes. When the length of the gate is equivalent to 0.3µm and width of the gate is equivalent to 300 µm, a mechanism could be pointed as 0.3x300. The periodicity is verified by the length of the gate. The recurrence will increase with the length of the gate reducing. The width of the gate can confirm the nature of the material. The current capability is one example. The voltage of pinch off of MESFET materials is translated by the channel of the active region.

4.1.1. Operating Principles of Gallium Nitride MESFET

By applying the different voltages, a MESFET material is biased V_GS is between the source and the gate and VDS is between the source and the drain. The current of channel present between source and drain is controlled by the applied voltage by differing the region of the depletion of gate and the electric field. Even without going into profound physical analysis, this functionality might be demonstrated. The I_DS-V_DS characteristic of the MESFET materials can be distinguished for different cases. If V_GS is bigger than the voltage Vp of the pinch off, level V_DS voltage where I_DS directly relative to V_DS, V_DS is the steady value [61].

4.1.2. I-V Characteristics of GaN MESFET

The current of the drain-source against the voltage of the drain-source (IDS - VDS) characteristics of Gallium nitride MESFET on silicon is shown in Figure 34.

![Figure 34: Ids-Vds Plot for Vgs of GaN MESFET.](image-url)
The Figure 4.2 demonstrates various I-V curves of the MESFET, for a perfect, ideal MESFET. The characteristics are plotted for values of $V_{gs}$. The ideal I-V curve displays limited positive slope in the region of saturation and this is evident. This situation can be given numerous explanations. The junction of the carrier into the substrate of the semi-insulating is the junction of the carrier into the substrate of the semi-insulating for the short gate device. In the conductance in the output in a MESFET model, this curve is the source. The actual current is indicated by the dashed curves whereas solid curves are drawn for indication of ideal current.

When $V_{gs} = 0$, the depletion region under the Schottky-barrier gate is relatively narrow, and as $V_{ds}$ is raised, a longitudinal electric field and current are established in the channel. The voltage across the depletion region is greater at the drain end than at the source end because of $V_{ds}$, and so the depletion region becomes wider at the drain end. An electric field is developed near the channel, making the electrons to move rapidly due to the reducing of the channel and the processing of the expanding of the $V_{ds}$. The voltage squeeze off in the situation when $V_{gs} = V_p$ and the channel current is zero, paying small regard to the nature of $V_{gs}$. As the depth of the active channel is to be constant throughout the process of fabrication it is situated to voltage breakdown and the pinch-off voltage and the voltage pinch off is determined by the active channel depth [62].
As illustrated in Figure 35(b), as the Voltage is been further raised from drain to source (V\text{ds}), when the pinch off voltage is lesser than the voltage of gate to source (V\text{gs}), there will be an increasing in the channel current, the region of the depletion gets deeper at the end of the drain, and the channel of the conductive gets narrower. The current should be steady throughout the channel. Therefore, if the conductive channel of the drain gets narrower, there will be rapid movement in the electrons.

Normally just a tenths of volt creates the saturation of the velocity, and as the V\text{ds} is above this value, the concentration of the electrons other than the velocity should increase to attain the continuity of the current. At the gate end, the region of accumulation of the electrons is formed. As these electrons move at velocity into between the drain and the gate throughout the channel, a region of depletion of electrons formed. Due to the ions of

Figure 35: GaN MESFET studied under different biasing; (a) Linear region (V\text{ds} is very low), (b) V\text{ds} at saturation, (c) V\text{ds} is high”.
the positive donor, the depletion region is absolutely charged. The more of the increasing of the voltage is dropped over the region to implement the electrons to cross it and the lesser is dropped over the channel which is the part of unsaturated, if $V_{ds}$ increases, as shown in Figure 35 (c). This attained region is known as charge domain. A situation is attained where the increasing in $V_{ds}$ is dropped completely over the charge domain, and there is no increase in the drain current [63].
In order to develop the channel current equation, the channel charge has been evaluated and the gradual channel approximation [64] has been adopted to find the channel current as:

\[
I_{ch} = g_0 \left\{ V_I - \frac{2}{3} \left( \frac{(V_I + V_{Bl} - V_{gs})^3 - (V_{Bl} - V_{gs})^3}{V_{po}^2} \right) \right\}
\] (5.1)

Where, \( I_{ch} \) = channel current

\( V_I \) = voltage drop across the gate region,

\( V_{Bl} \) = Schottky barrier height,

\( V_{gs} \) = gate to source voltage,

\( V_{po} \) = the pinch-off voltage,

\( g_0 \) = channel conductance,

The below equation defines the channel conductance

\[
g_0 = \frac{q \mu N_D W A}{W_G}
\] (5.2)

And the pinch off voltage, \( V_{po} \) is given by

\[
V_{po} = \frac{q N_D A^2}{2 \varepsilon_0 \varepsilon}
\] (5.3)

Where, \( q \) = Electronic charge,

\( N_D \) = Doping density,
$\epsilon_0 = \text{Dielectric constant in vacuum}$

$\varepsilon = \text{Permittivity for GaN,}$

$A = \text{Active channel thickness,}$

$W = \text{Gate width and}$

$W_G = \text{Gate length.}$

The figure 36 shows the electrical parameters in the active region

$I_d = \text{Drain Current}$

$I_{\text{sub}} = \text{Substrate Current}$

$V_{\text{dom}} = \text{Domain voltage}$

---

**Figure 36: MESFET geometry**
5.1 Carrier Mobility Calculation

![Drift velocity-field characteristics of WZ-GaN](image)

The carrier mobility can be defined by

\[ \mu = \frac{V}{E} \]

Considering the domain effect, the drain source voltage can be expressed as

\[ V_{ds} = E \cdot D \]

Where, \( D \) = Domain Length.

The domain length can be defined as

\[ d = \frac{\epsilon_s}{q n_0} (E_c - E_r) \]

Where, \( \epsilon_s \) = Permittivity of GaN

\( n_0 \) = no. of carrier transferred from lower valley to upper valley

\( E_c \) = Critical Electric field

Figure 37: Drift velocity-field characteristics of WZ-GaN
Er= Minimum Electric field

Hence, The NDR significantly affects the transconductance and gate capacitance stated in the resultant discussion.

Figure 37 shows the drift velocity versus electric field. The plot has been generated from Monte Carlo simulation, where the peak drift velocity of $3 \times 10^7 V/m$ is observed at the critical electric field of $1 \times 10^5 V/cm$. The drift velocity decreases with increase of electric field in the range of $1 \times 10^5 V/cm$ to $2 \times 10^5 V/cm$ and the drift velocity becomes saturated. Therefore, the NDR effect is observed between the electric field in the range of $1 \times 10^5 V/cm$ to $2 \times 10^5 V/cm$ and this NDR effect is reasonable for forcing domain due to lowering the carrier mobility and drift velocity.

The Trans conductance is derived by the following equation

$$g_m = \frac{\partial \chi}{\partial V_G} = \frac{g_0}{V_p^2} \left( \left( \frac{v_{ds} + v_{Bi} - v_{gs}}{v_{gs}} \right)^{\frac{1}{2}} - \left( \frac{v_{Bi} - v_{gs}}{v_{gs}} \right)^{\frac{1}{2}} \right)$$

(5.4)

The drain-to-gate capacitance $C_{dg}$ of a GaN MEESFET is shown in Figure 38 is expressed as,

$$C_{dg} = \left( \frac{\partial Q}{\partial V_G} \right)_{V_G = \text{constant}}$$

(5.5)

The gate-drain capacitance can be obtained as

$$C_{gd} = \frac{2\sqrt{2}}{3} \frac{W W_G (\epsilon_0 \epsilon q N_D)^{\frac{1}{2}}}{A V_l^2} \left[ \frac{3}{2} V_{ds} (V_{ds} + V_{Bi} - V_G)^{\frac{1}{2}} - (V_{ds} + V_{Bi} - V_G)^{\frac{3}{2}} - (V_{Bi} - V_G)^{\frac{3}{2}} \right]$$

(5.6)
Finally the gate-to-source capacitances \( C_{gs} \) is obtained by following equation

\[
C_{gs} = \left( \frac{\partial Q}{\partial V_{ds}} \right)_{V_{ds} = V_G = \text{constant}} \quad (5.7)
\]

Consequently, the gate-source capacitance can be evaluated as

\[
C_{gs} = \frac{2\sqrt{2} W W_{G} \varepsilon_0 \varepsilon N_D}{A V_{ds}^2} \left\{ (V_{ds} + V_{Bi} - V_G)^{\frac{1}{2}} - (V_{Bi} - V_G)^{\frac{1}{2}} - \frac{3}{2}(V_{Bi} - V_G)^{\frac{1}{2}} \right\} \quad (5.8)
\]

Substituting \( V_{ds} \) in the above equation 5.8 with the Electric field and gate length

\[ V_{ds} = EL \]

But we know, \( E = V_d / \mu \)

From transconductance, the cutoff frequency [64] can be calculated and gate capacitance can be derived from the below equation:

\[
f_T \simeq \frac{1}{2\pi} \frac{g_m}{(C_{gs} + C_{gd})} \quad (5.9)
\]
For the case when $C_{gd} \ll C_{gs}$, the value of $f_T$ can be approximated as,

$$f_T \approx \frac{1}{2\pi} \frac{g_m}{C_{gs}} \quad (5.10)$$

### 5.2 Calculating Intrinsic Carrier Concentration

Recalling from chapter 2, the intrinsic carrier concentration $n_i$ can be expressed by using the following equation [53]

$$n_i = (N_C N_V)^{1/2} \exp(-E_g/(2k_B T)) \quad (5.2.1)$$

Where $T$ is measured as degree kelvin, $k_B$ is Boltzmann constant valued as $8.6173 \times 10^{-5} \text{eV K}^{-1}$ and $N_C$ is the effective density of states in the conduction band which can be valued by below equation:

For Zn blende structure $N_C \approx 4.82 \times 10^{15} \left(\frac{m_r}{m_0}\right)^{3/2} T^{3/2} (\text{cm}^{-3})$

$$\approx 2.3 \times 10^{14}. T^{3/2} (\text{cm}^{-3}) \quad (5.2.2)$$

For 300K, $N_C = 1.2 \times 10^{18} (\text{cm}^{-3})$

For Wurtzite structure $N_C \approx 4.82 \times 10^{15} \left(\frac{m_r}{m_0}\right)^{3/2} T^{3/2} (\text{cm}^{-3})$

$$\approx 4.3 \times 10^{14}. T^{3/2} (\text{cm}^{-3}) \quad (5.2.3)$$

For 300 K, $N_C = 2.2 \times 10^{18}. (\text{cm}^{-3})$

In equation 5.1, $N_V$ is the effective density of states in the Valance band which can be valued by below equation:
For Zn blende structure $N_{\nu} = 8.0 \times 10^{15}. T^\frac{3}{2} \ (cm^{-3}) \ \ (5.2.4)$

For 300 K, $N_{\nu} = 4.1 \times 10^{19} \ (cm^{-3})$

For Wurtzite structure $N_{\nu} = 8.9 \times 10^{15}. T^\frac{3}{2} \ (cm^{-3}) \ \ (5.2.5)$

For $N_{\nu} = 4.6 \times 10^{19} \ (cm^{-3})$

These Values of $N_C$ and $N_{\nu}$ are used to calculate the value of intrinsic carrier concentration $n_i$

$$n_i = (N_C N_{\nu})^{1/2} \exp(-E_g/(2k_B T))$$

For Zn blende structure at 300K, $E_g = 3.2 \ eV, n_i = 7.86 \times 10^{-9}$

For Wurtzite structure at 300K, $E_g = 3.39 \ eV, n_i = 2.95 \times 10^{-10}$
CHAPTER 6: Results and Discussion

In order to determine the GaN based device performance, an analytical model of a GaN-based MESFET device has been developed. The NDR effect on intrinsic parameters has been incorporated in the analytical model with intensive study on the material physics and device physics. The analytical model has been simulated by using MATLAB tool to evaluate the channel current, transconductance, channel conductance, gate capacitance and frequency stated by the following results. The GaN material shows a piezoelectric charge, polarization and NDR effect due to large electric field. In the large electric field the carriers with NDR effect on mobility shows the carriers transfer from lower valley to the upper valley, which in turn form the domain in the channel.

![Graph showing channel current vs drain to source voltage for varying gate voltage](image)

**Figure 39: Ich Vs Vds for varying Vgs**
The Figure 39 shows a plot of channel current $I_{ch}$ versus drain source voltage $V_{ds}$ for different gate source voltage $V_{gs}$ of 0V, -10V and -20V with channel doping concentration $N_D$ of $1\times10^{17}$ cm$^{-3}$, substrate concentration of $1\times10^{15}$ cm$^{-3}$, gate length $W_g$ of 1µm, device width $W$ of 100µm, active channel thickness of 0.3µm. The channel current shows a linear properties up to the drain source voltage $V_{DS}=50$V and the pinch off voltage was found approximately 75V in the nonlinear region. The current saturation region has been found at the drain source voltage $V_{DS}=250$V. The I-V characteristics properties shows high power device performance and compatible with ideal behavior of typical MESFET device.

![Figure 40: Channel current (Ich) vs. Active channel thickness for different $V_{gs}$](image-url)

Figure 40: Channel current (Ich) vs. Active channel thickness for different $V_{gs}$
The Figure 40 presents a plot of channel current $I_{ch}$ versus active channel thickness for different gate source voltage $V_{gs}$ of 0V, -10V and -20V with channel doping concentration $N_D$ of $1 \times 10^{17}$ cm$^{-3}$, substrate concentration of $1 \times 10^{15}$ cm$^{-3}$, gate length $W_g$ of 1µm, device width $W$ of 100µm, active channel thickness of 0.3µm. The plot shows that the channel current linearly increases with increase of channel depth for 0.3µm to 1µm. The channel current increases due to large channel depth because of large amount of channel charge. This plot has been generated by important equation

$$I_{ch} = g_0 \left\{ V_I - \frac{2}{3} \left[ \frac{(V_t + V_{Bl} - V_{gs})^3}{V_{po}^2} - \frac{(V_{Bl} - V_{gs})^3}{V_{po}^2} \right] \right\}$$
The Figure 41 displays the plot of trans conductance versus gate voltage \( V_{GS} \) for drain source voltage \( V_{DS}=125V \) at saturation region with channel doping concentration \( N_D \) of \( 1 \times 10^{17} \) cm\(^{-3} \), substrate concentration of \( 1 \times 10^{15} \) cm\(^{-3} \), gate length \( W_g \) of 1µm, device width \( W \) of 100µm, active channel thickness of 0.3µm. The transconductance \( g_m \) increases with the gate voltage transition from -8V to 2V and the characteristics of \( g_m \) plot confirm that it behaves as depletion device. The transconductance plot has been generated by the important equation

\[
g_m \approx \frac{\partial I_{ch}}{\partial V_G} = g_0 \frac{(V_{DS}+V_{BI}-V_{GS})^2-(V_{BI}-V_{GS})^2}{V_{gs}^2}
\]
Considering the variable carrier mobility due to NDR formed by the domain effect.

![Variation of gate-drain capacitance with drain-source voltages](image)

**Figure 42: Cgd Versus Vds for varying Vgs.**

The Figure 42 shows the result of a plot of gate to drain capacitance ($C_{gd}$) versus drain source voltage $V_{ds}$ for different gate voltages $V_{GS}$ of 0, -6, -12V with channel doping concentration $N_D$ of $1 \times 10^{17} \text{cm}^{-3}$, substrate doping concentration $N_A$ of $1 \times 10^{15} \text{cm}^{-3}$, channel length $W_G$ of 1µm, channel width $w$ of 100µm and channel thickness of 0.9µm.
The Figure 43 exhibits the plot of gate source capacitance $C_{gs}$ versus gate source voltage $V_{gs}$ for different drain source voltage $V_{ds}$ with channel doping concentration $N_D$ of $1 \times 10^{17} \text{ cm}^{-3}$, substrate concentration of $1 \times 10^{15} \text{ cm}^{-3}$, gate length $W_g$ of $1 \mu\text{m}$, device width $W$ of $100 \mu\text{m}$, active channel thickness of $0.3 \mu\text{m}$. The $C_{gs}$ exponentially increases with increase of gate source voltage range from -30V to 5V. The maximum $C_{gs}$ value of 0.63 at $V_{gs}$=5V is obtained and the $C_{gs}$ is found to be dominated by Carrier mobility and the drift velocity due to the NDR effect high electric field in the drain region. The plot has been computed by using the equation


$$C_{gs} = \frac{2\sqrt{2}}{3} \frac{WW_G(\varepsilon_0\varepsilon qN_D)^2}{AV_{ds}^2} \left[ (V_{ds} + V_{Bi-V_G})^3 - (V_{Bi-V_G})^2 - \frac{3}{2}(V_{Bi-V_G})^2 \right]$$

Figure 44: Wg Vs cut-off frequency (ft) for varying Vgs

The Figure 44 shows a plot of cut off frequency versus the domain length for $V_{gs}=3V$ and $-5V$ with constant drain to source voltage $V_{ds}=10V$, channel doping concentration $N_D$ of $1\times10^{17}$ cm$^{-3}$, substrate concentration of $1\times10^{15}$ cm$^{-3}$, gate length $W_g$ of 1µm, device width $W$ of 100µm, active channel thickness of 0.8µm.
CHAPTER 7: Conclusion

An analytical model of GaN MESFET has been developed to study the negative differential resistance (NDR) effect on the electron drift velocity and electron mobility to promote the GaN MESFET device for THz. The NDR effect due to the transition of the carrier from lower valley to upper valley has been studied to determine the domain related parameters. The drain-source current, transconductance and gate capacitance has been simulated. The analytical model shows that NDR effect on transconductance and gate capacitance increase the frequency response in the range of THz. The study of drift velocity and electric field is important to understand the mechanism of NDR effect and carrier transition between lower valley and upper valley. This research on GaN material and devices is having extreme potential prospects for future research scope for innovative development of high power THz devices.
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