Evaluation of Base Pedestal Depth on Electrical and Thermal Performance of
Heterojunction Bipolar Transistors

A graduate project submitted in partial fulfillment of the requirements
For the degree of Master of Science in Electrical Engineering

By
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Abstract

Evaluation of Base Pedestal Depth on Electrical and Thermal Performance of Heterojunction Bipolar Transistors

by

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Master of Science in Electrical Engineering

Heterojunction bipolar transistors (HBTs) are heavily used in RF front-end modules for signal amplification. Whether designed as part of a low noise amplifier (LNA) on the receiver end of a RF transceiver system, or as part of the power amplifier (PA) on the transmitter end, HBT performance is a critical element of RF circuit design. Four key parameters that characterize HBT performance are D.C. current gain ($\beta$), thermal resistance $R_{th}$, base-collector junction capacitance $C_{jc}$, and the high-frequency figure of merit, $f_T$.

This graduate project focuses on taking an existing Gallium-Arsenide (GaAs) HBT device, and evaluating performance based upon changes in the HBT device construction process. These changes resulted in build conditions that produced HBT structures with varied base pedestal depths. The evaluation of base pedestal depth on electrical and thermal performance of heterojunction bipolar transistors is presented in this project.
Chapter 1: Introduction

1.1 The Push for Performance

The environment of today’s world of smartphones and tablet devices is a long result of the evolution of mobile communications. In its early days, the primary objective of using a cellular channel was to make an analog voice call. Today, that primary objective has transitioned to the transfer of data. While the standard has not yet been defined for the next advancement in wireless technology, it is interesting to think of the possibilities that are achievable with future fifth-generation (5G) mobile communication. Some of the key things that come to mind are increased downlink and connectivity speeds, use of higher frequency spectrums, new infrastructures of access points constructed around the world, and the release of powerful yet power efficient 5G mobile handsets. Most highlighted of all, the concept of 5G almost assuredly guarantees an uptick in the number of wirelessly connected devices and what is referred to as the internet of things. The ability to move and be mobile while continuously connected to the devices around you, at connection speeds averaging at least 1000 Mbps (1 Gbps), is a key goal and objective of 5G mobile communication.

From a technical perspective, the data rate requirement of 5G likely mandates that the frequency spectrum allocated to cellular systems will move much higher than current standards. These already crowded frequency spectrums wouldn’t be able to support the bandwidths needed for 5G speeds without increased complexity or costs. With the move to higher frequencies new and more numerous access points would be required due to signal attenuation to achieve the same performance. Mobile handset architectures would be constructed to adapt and process the change in frequencies, creating a new set of challenges for integrated circuit (IC) design. These are the practical and technical considerations that need to be ironed out as the 5G wireless standard is established.

However, in the current environment of mobile wireless communication, these concepts related to 5G are simply that – concepts. The high rates of 5G will need to be achieved through a revolutionary technological improvement, most likely through the use of higher frequency bands, up to the millimeter wave frequencies above 30 GHz. This is
because the iterative improvements of the last few generations of mobile wireless standards have nearly reached saturation. The current cellular standards provide the constraints and limits in which the transfer of data can occur. Within these allocated cellular frequency bands, RF IC designers look for new opportunities to improve the performance of their devices to fulfill the requirements and demands of higher bandwidths and data transfer rates. One of the most common devices used by RF IC designers in the design of amplifiers used in mobile communications is the heterojunction bipolar transistor (HBT), which is the primary focus of this graduate project.

1.2 Problem Definition

With the limitations and constraints defined by the frequencies of current cellular standards, in combination with the iterative improvements of RF IC and HBT design nearly reaching saturation, what other solutions exist to improve performance? This graduate project attempts to provide an innovative solution to this question by taking an existing, production released HBT device design and affect performance through modifications in the HBT device construction process. By simply changing key stages in the construction process, can additional performance improvements be extracted, quantified through increased frequency response or gain, in addition to other HBT figures of merit? This is the fundamental goal and objective of this graduate project.

1.3 Project Overview

With this purpose and goal in mind, an existing, production released heterojunction bipolar transistor design was modified in the construction process to create five distinct HBT structures. These changes resulted in build conditions that produced HBT structures with varied base pedestal depths. The evaluation of base pedestal depth on electrical and thermal performance of heterojunction bipolar transistors is presented in this project.
Chapter 2 discusses the background of heterojunction bipolar transistors and the formulated theory behind changing the base pedestal depths and the specific HBT build conditions selected. Chapter 3 discusses the methodology followed in the modification of the device construction process. Chapter 4 provides the results and verification of the HBT construction process, while Chapter 5 presents the electrical measurements and performance of the devices constructed. Lastly, Chapter 6 includes the discussion of the overall results and provides the summary conclusion for this graduate project.
Chapter 2: Background

2.1 The Heterojunction Bipolar Transistor Structure

The heterojunction bipolar transistors involved in this graduate project began with 6-inch wafer substrates of Gallium-Arsenide (GaAs). The bare 6” GaAs wafers were processed through a multilayer deposition process known as epitaxy. Layers of semiconductor crystalline material with specified electrical properties are deposited, one on top of another, forming the desired NPN semiconductor structure; only NPN HBTs were constructed in this project. The three terminal HBT devices, consisting of a layer of P-doped semiconductor in between two N-doped layers, are classified into the emitter, base, and collector regions. The differing semiconductor materials for the emitter-base and base-collector junctions create the heterojunctions for the bipolar junction transistor. This stack of doped semiconductors, grown atop a 6” GaAs wafer substrate, provides the building materials that form the basis for HBT device construction. Figure 2.1 illustrates the diagram of an HBT NPN structure with its corresponding circuit symbol. Figure 2.2 shows an epitaxial wafer grown on top of a 6” GaAs wafer substrate.

![Figure 2.1: Diagram of HBT NPN structure, with Corresponding HBT Circuit Symbol](image)

![Figure 2.2: Epitaxial HBT Stack on Top of 6” GaAs Wafer Substrate (Not-to-Scale)](image)
While Figure 2.1 and Figure 2.2 show the collector region of the HBT structure as a single block of N-doped semiconductor material, the region is actually divided into two sub-sections: 1) a collector and 2) sub-collector. The sub-collector region is a low resistivity layer that serves as the highly conductive medium between the collector and collector metal contact. Because of the distance of the collector metal contact from the collector, the sub-collector region allows for ease of transport of current and electrons across the horizontal path of the device. Figure 2.3 shows the collector and sub-collector regions grown atop the 6” GaAs wafer substrate. Figure 2.4 illustrates a diagram of an HBT NPN structure, with physical device representation. For future reference, the 6” GaAs wafer substrate are omitted from future illustrations; all figures of the HBT devices shown will be implicitly assumed to be constructed on 6” GaAs wafers substrates.

Figure 2.3: Epitaxial HBT Stack with Sub-Collector Region (Not-to-Scale)

Figure 2.4: Diagram of HBT NPN structure, with Physical Device Representation
2.2 Key Dimensions of an HBT Device and Effects on Performance

Two key dimensions of an HBT that affect the performance of the device are: 1) the base-collector junction area and 2) the emitter-width. The base-collector junction area is determined by the width of the base layer and heavily influences the base-collector junction capacitance $C_{jc}$. $C_{jc}$ is an intrinsic, parasitic capacitance that impacts amplifier performance at high operating frequencies (> 2 GHz). High base-collector junction capacitance decreases gain at higher frequencies. While the width of the base constitutes the base-collector junction area, the base-collector effective area includes the base pedestal and collector regions below the junction. The base pedestal is defined as the area identified in Figure 2.5.

The second key dimension of HBT devices is the emitter-width. This area, where the emitter-base junction occurs, is the primary location for the majority of the thermal properties of the device, as electrons move from the emitter through the base, on the way to the collector. Because of this transport of electrons, the main heat generation in HBT devices is at the emitter-base junction. This heat is dissipated down through the base and collector. This is measured and quantified in a parameter defined as the thermal resistance, $R_{th}$. Figure 2.5 illustrates the key dimensions discussed, the base-collector junction area and the emitter-width.

Figure 2.5: Key Dimensions of an HBT Device
2.3 Project Goal and Objective

Evaluating the key dimensions of an HBT device and their impacts provided the opportunity to test an innovative theory and technique to improve device performance. The objective was to take an existing, production released HBT design and affect performance through modifications in the HBT device construction process. Keeping the methods of HBT design normally used to fine-tune performance fixed (such as semiconductor doping, layout, material, etc.), modifications to the construction process were made and tested for performance improvements. These improvements could be quantified through increased frequency response or gain, in addition to other HBT figures of merit. The modification to the construction process would primarily influence the base pedestal structure. The observations and results would answer two key questions. First, for the base-collector junction, is $C_{jc}$ limited to the actual junction, or is there an effect from the effective pedestal area (i.e. the slope of the pedestal and base-collector effective area)? Secondly, for thermal resistance $R_{th}$, how does the base pedestal influence the heat dissipation?

The answers to these questions could provide an additional degree of freedom to HBT design, as well as an immediate performance impact on current product offerings already modeled and characterized. Since RF IC and HBT design is often balanced by trade-offs between performance, power efficiency, device size, and noise, a decrease in $C_{jc}$ could provide additional margin in performance necessary to achieve a customer’s technical requirements. From a factory and manufacturing perspective, the modifications to the HBT construction process tested would provide a study on conditions that would improve manufacturing efficiency and factory throughput.

With this purpose and goal in mind, an existing, production released heterojunction bipolar transistor design was modified in the construction process to create five distinct HBT structures.
2.4 Theory and Selection of the HBT Build Conditions

The base pedestal structure of an HBT device was introduced in Section 2.2, as well as the base-collector junction capacitance $C_{jc}$. While this junction capacitance is known to be dependent on the area of the base-collector junction, it is theorized in this graduate project that there is also a dependence of $C_{jc}$ on the base-collector effective area that includes the base pedestal and collector regions below the junction. By modifying the construction process to vary the depth of the base pedestal and its respective profile, the effective base-collector area can be decreased or increased. This decrease or increase in the amount of doped semiconductor material beneath the base-collector junction area should influence the value of $C_{jc}$, and hence affect the performance of the device. In theory, the less the value of base-collector effective area, the lower the expected value of the base-collector capacitance $C_{jc}$ should be. The opposite is also suggested to be true; by increasing the value of the base-collector effective area, the higher the expected value of $C_{jc}$. The value of the base-collector effective area is proportional to the base pedestal depth; the more shallow the pedestal depth, the less the value of the base-collector effective area, with the opposite also being true.

In addition, it is also proposed that the thermal resistance $R_{th}$ should similarly be impacted as $C_{jc}$ by the base pedestal depth, with the inverse effect. By removing more doped semiconductor material and decreasing the value of the base-collector effective area, there is less area available to dissipate the heat generated from the emitter-base junction, thereby increasing the value of the thermal resistance $R_{th}$. Again, the opposite is also suggested to be true; by increasing the value of the base-collector effective area and the depth of the base pedestal, the lower the expected value of $R_{th}$.

With this hypothesis in mind, five separate HBT build conditions are proposed and selected in this graduate project, including one control condition that utilizes the standard base-collector effective area and base pedestal depth, formed by the HBT construction process of record. Two HBT build conditions that decreased the effective base-collector area were constructed: HBT Build Condition #1 (most shallow base pedestal, compared to the standard) and HBT Build Condition #2 (shallow base pedestal, compared to the standard). In addition, two HBT build conditions that increased the
effective base-collector area were constructed: HBT Build Condition #4 (deeper base pedestal, compared to the standard) and HBT Build Condition #5 (deepest base pedestal, compared to the standard). The standard base-collector effective area (control) is classified as HBT Build Condition #3. Table 2.1 illustrates the five HBT build conditions, with corresponding base pedestal depths and base-collector effective areas. The exact specifications for the HBT build conditions, as well as the mechanisms for increasing/decreasing the base-collector effective area by varying the base pedestal depth, are presented next in Chapter 3.

<table>
<thead>
<tr>
<th>HBT Build Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Most Shallow Base Pedestal Depth, Least Base-Collector Effective Area</td>
</tr>
<tr>
<td>2</td>
<td>Shallow Base Pedestal, Decreased Base-Collector Effective Area</td>
</tr>
<tr>
<td>3</td>
<td>Standard Base Pedestal Depth, Standard Base-Collector Effective Area</td>
</tr>
<tr>
<td>4</td>
<td>Deep Base Pedestal, Increased Base-Collector Effective Area</td>
</tr>
<tr>
<td>5</td>
<td>Deepest Base Pedestal, Highest Base-Collector Effective Area</td>
</tr>
</tbody>
</table>

Table 2.1: Description of HBT Build Conditions
Chapter 3: Methodology – Modification of HBT Device Construction Process

3.1 Existing HBT Device Construction

The device construction process used in this graduate project was Skyworks Solutions patented BiFET process technology [2]. The process involves integrating an HBT device with a field effect transistor (FET) on the same IC chip. For the purposes of this project, only the HBT portion of the construction process was modified and characterized; the FET devices on each of the build conditions remained unchanged. The BiFET process from Skyworks Solutions begins with an HBT stacked epitaxial wafer grown atop a 6” Gallium Arsenide (GaAs) wafer.

From the HBT stack, material is carved out to form the HBT structure, complete with metal contacts that serve as the terminal connections, as illustrated by Figure 3.1. In order to form the terminals to the emitter, base, and collector layers of the HBT, the semiconductor material for each region must be exposed through a series of fabrication processes. The exception to this is the emitter layer, which is already located at the top of the epitaxial stack. Once the region of semiconductor is open, a metal pad can be deposited and placed in direct contact with the layer material, forming the terminal connection.

Figure 3.1: Device Representation of HBT with Metal Terminals Contacts
It is through this process that the metal terminal contacts are formed for the emitter and base HBT regions. From this point, the focus on the HBT construction process is placed on the formation of the base pedestal and collector contact stages. The construction process for the base pedestal and collector contact stages consist of two major etch steps that remove semiconductor material in the epitaxial stack, defining the base and collector regions. The first etch (Etch 1) forms the base pedestal, with 5000 Angstroms (Å) of material removed. One key feature of the base pedestal etch is the negative slope that is formed. The second etch (Etch 2) creates the contact area for the collector metal, with 9800 Å of material removed. The total amount of semiconductor material removed reaches an etch depth of 14800 Å, measured from the top of the base layer to the metal contact area for the collector region. A diagram of the etch processes and their respective depths can be seen in Figure 3.2.

![Figure 3.2: HBT Diagram of Etch Processes](image)

The two etches play an important factor in defining the key areas that impact the performance of the device discussed in Section 2.2. These etch processes form the device structure according to the layout of the HBT design. The base pedestal slope and profile, as well as the overall depth is defined by Etch 1, while the pocket created for the collector contact is defined and formed by Etch 2. It is in these two main stages of Skyworks Solutions BiFET process where the HBT build conditions proposed in Section 2.4 were modified.
3.2 Experimental Conditions – Varying the Base Pedestal Depth

Five 6” GaAs wafers were processed through Skyworks Solutions BiFET process up until the base pedestal formation stage. Each of the five wafers represented the HBT build conditions selected for this graduate project. At the base pedestal step, the standard HBT construction process of record was modified to build HBT devices with various conditions of base pedestal depth. The standard base pedestal etch (Etch 1) targets an etch depth of 5000 Angstroms (A). The process was modified for additional conditions of base pedestal depths of 1000, 3000, 7000, and 9000 A, respectively. A total of five different HBT build conditions, including one control, were constructed from a processing lot of five 6” epitaxial GaAs wafer substrates.

With the change of target values for the base pedestal etch (Etch 1), a corresponding change was required at the collector contact etch (Etch 2) for each condition. This compensation in the collector contact etch depth was necessary in order to maintain the overall desired etch depth of 14800 A. Table 3.1 shows the various base pedestal depth targets, with corresponding collector contact depth, for the experimental build conditions.

<table>
<thead>
<tr>
<th>HBT Build Condition</th>
<th>Etch 1 Target (A)</th>
<th>Etch 2 Target (A)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1000</td>
<td>13800</td>
<td>Shallow Base Pedestal, Deep Collector</td>
</tr>
<tr>
<td>2</td>
<td>3000</td>
<td>11800</td>
<td>Below Target Base Pedestal, Above Target Collector</td>
</tr>
<tr>
<td>3</td>
<td>5000</td>
<td>9800</td>
<td>Standard Condition (Control)</td>
</tr>
<tr>
<td>4</td>
<td>7000</td>
<td>7800</td>
<td>Above Target Base Pedestal, Below Target Collector</td>
</tr>
<tr>
<td>5</td>
<td>9000</td>
<td>5800</td>
<td>Deep Base Pedestal, Shallow Collector</td>
</tr>
</tbody>
</table>

Table 3.1: Etch Targets and Description of HBT Build Conditions

Varying Etch 1 and Etch 2 depth targets would yield five different vertical HBT structures, each with a unique base pedestal formation. While the primary difference for each condition would be the base pedestal depth, of equal importance would be the difference in the overall profile of the base-collector area. This is a result of the different etch techniques used for the respective etches.
The base pedestal etch (Etch 1) uses a dry etching process where an inductively-coupled plasma is formed in a vacuum chamber. The plasma is formed by igniting a reactant etchant gas with an RF power source. The etch mechanism in this process is both physical and chemical in nature. The ions in the plasma bombard the region of exposed semiconductor, causing material to be physically knocked off. In addition, there is a chemical reaction that occurs when the etchant gas comes into contact with the exposed semiconductor material. The result is a negatively sloped profile that occurs due to polymer formation as the etch progresses in depth. The polymers, a byproduct of the reactions, form on the edges of the etched material and progress down, blocking the etch in the process and forming the negative slope. Etch 1 is processed in a tool known as a dry etcher, where wafers are etched individually in a single-wafer processing system. A wafer cassette is loaded into a transfer chamber, where a mechanized robotic arm loads the wafers onto a grounded chuck. The wafers are etched one at a time in a serial process, until all the wafers in the cassette are completed. Figure 3.3 illustrates the base pedestal formation through the Etch 1 process.

The collector contact etch (Etch 2) uses a wet etching process that is strictly chemical in nature. An etching solution is formed in a bath that is located in a tool known as a wet etch bench. Wafers are loaded into an etch resistant Teflon cassette, and the cassette is submerged in the etching solution for a fixed time to complete etch process. The etch solution chemically reacts with the exposed semiconductor material and the etched material is removed by the agitation of the liquid etchant solution. The result is an undercut profile that is considerably different than the sloped result of the dry etch.
process used in Etch 1. It is this specific undercut that is the primary mechanism in the change to the base-collector profile for each HBT build condition. This undercut forms the pocket in which the collector metal contact is deposited. Figure 3.4 shows the Etch 2 process and the collector contact pocket formation.

![Figure 3.4: Etch 2 Collector Contact Pocket Formation](image)

By varying the depth of the base pedestal depth, from shallow to deep, the introduction of Etch 2 is also varied. In the shallow base pedestal depths (1000, 3000 A), the undercut is introduced earlier than the normal depth, replacing the sloped nominal profile with a significant undercut. This undercut results in more semiconductor material being removed from the base-collector region than the standard control process. For illustrative purposes, Figure 3.5 illustrates a diagram of the existing HBT process construction profile (top) versus the most shallow base pedestal depth built (1000 A) and its resulting undercut profile.
3.3 Test and Validation

Five wafers were processed through the HBT construction process for the purposes of this graduate project, with modifications completed at the base pedestal etch (Etch 1) and collector contact etch (Etch 2). The results of the varied conditions of the HBT construction process were tested and validated. Base pedestal and collector etch depths were measured in-line to ensure accurate construction. In addition, the HBT vertical profile of the base-collector regions for each build condition were visually observed for evaluation. Electrically, the different HBT devices were tested under both DC and RF test conditions. For DC, various parametric parameters were evaluated for device comparison. For RF test conditions, 2-port S parameter network analysis was performed to obtain comparative data. The results of these etches, the in-line measurements, and the visual verification of the etch profiles are presented in Chapter 4.
Chapter 4: Etch Results and Verification

4.1 The Etch Mask Process

For both etches, Etch 1 and Etch 2, a photolithography process was used to define the desired for material removal and protect the areas where no etch was desired. The technique involves the use of an etch mask process that is used to define the areas of etch. The process involves using a light-sensitive chemical material known as positive photoresist \[^3\]. The photoresist material is coated onto the wafer surface, where a pattern is imaged into the material by using a light mask, also referred to as a reticle. The process is completed on a system known as an optical stepper \[^3\]. Using the light mask, the optical stepper exposes portions of the wafer with light through reticle, selectively defining the desired pattern or image. The light-sensitive properties of the photoresist cause the areas exposed to light to be developed out, exposing the underlying surface. Areas of photoresist that are not exposed to the light, blocked by the reticle mask, remain on the wafer, creating the etch mask used for both Etch 1 and Etch 2. The remaining photoresist acts as a protective block to both etches, an attribute that led to the material being called “resist” from its ability to resist the actions of the etchants \[^3\].

4.2 Etch 1 – Base Pedestal Formation

After completing the steps of the HBT construction process that formed the emitter and base contacts, the wafers reached the first stage where build conditions would be modified. All five wafers had received identical processing up until this step. In order to achieve the desired targeted etch depths for each wafer build condition, new recipes were created on the dry etch tool used for Etch 1. The base pedestal etch uses a timed etch recipe that controls the duration plasma is exposed to the wafer. Using the standard base pedestal etch recipe of 70 seconds used to achieve an average etch depth target of 5000 Angstroms (A), additional recipes were created for the various desired base pedestal depths. Using a ratio calculated from the standard recipe (70 seconds / 5000 Angstroms), rough etch times were extrapolated to create four additional recipes. These experimental
recipes were fine-tuned through a series of test runs and in-line measurements. The finalized times for the various conditions of Etch 1 are shown in Table 4.1.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>Target Etch Depth (in Angstroms)</th>
<th>Etch Time (in Seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition 1</td>
<td>1000</td>
<td>9</td>
</tr>
<tr>
<td>Condition 2</td>
<td>3000</td>
<td>40</td>
</tr>
<tr>
<td><strong>Condition 3 (Standard)</strong></td>
<td><strong>5000</strong></td>
<td><strong>70</strong></td>
</tr>
<tr>
<td>Condition 4</td>
<td>7000</td>
<td>95</td>
</tr>
<tr>
<td>Condition 5</td>
<td>9000</td>
<td>123</td>
</tr>
</tbody>
</table>

Table 4.1: Etch 1 Recipe Times by Condition

With the recipes finalized, the five wafers representing each HBT build condition were processed through the dry etch tool. The wafers were loaded into a transfer chamber, where a mechanized robot transported each wafer to and from the single wafer processing module containing the grounded wafer chuck. The wafers were etched one at a time in a serial sequence, with each wafer dry etched with the corresponding recipe to achieve the targeted etch depth for each condition. Figure 4.1 shows the transfer chamber and processing module for the Etch 1 dry etch tool.

Figure 4.1: Transfer Chamber (Right) and Processing Module (Left) for Etch 1 Tool
Following the etch, the wafers were subjected to an in-line metrology step that provided an accurate measurement of the etch depth. On a tool known as an *automated surface profiler*, the wafers were all individually loaded onto a measurement stage. The movable stage was then programmed with the coordinates of test structures located at the top, center, and bottom of the wafer, each with an etched window. A fine point stylus was lowered directly onto the test structure, moving along the window opening and recording the step height created by the etch. By measuring the etch depths at the three locations, the mean value could be calculated, as well as the range (maximum point minus the minimum point). These values are shown in Table 4.2. Figure 4.2 shows the automated surface profiler tool used to obtain the etch depth measurements.

<table>
<thead>
<tr>
<th>Wafer Build Condition</th>
<th>Site 1 (Top)</th>
<th>Site 2 (Center)</th>
<th>Site 3 (Bottom)</th>
<th>Mean Etch Depth</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition 1</td>
<td>1213</td>
<td>1024</td>
<td>1180</td>
<td>1139</td>
<td>189</td>
</tr>
<tr>
<td>Condition 2</td>
<td>3195</td>
<td>2903</td>
<td>3245</td>
<td>3114</td>
<td>342</td>
</tr>
<tr>
<td>Condition 3</td>
<td>5361</td>
<td>4831</td>
<td>5393</td>
<td>5195</td>
<td>562</td>
</tr>
<tr>
<td>Condition 4</td>
<td>7070</td>
<td>6294</td>
<td>7189</td>
<td>6851</td>
<td>895</td>
</tr>
<tr>
<td>Condition 5</td>
<td>8926</td>
<td>8024</td>
<td>9102</td>
<td>8684</td>
<td>1078</td>
</tr>
</tbody>
</table>

Table 4.2: Etch 1 Depth Measurement (All Values in Angstroms)

Figure 4.2: Automated Surface Profiler Used to Obtain Etch Depth Measurements
The measurements show that the actual resulting mean etch depths were accomplished within the acceptable tolerance of +/- 6.0% from the targeted values. Varying the recipe times for Etch 1, the base pedestal depth was successfully defined per the desired HBT build conditions. With the formation of the base pedestal complete, the wafers were moved on to continue identical processing until the collector contact stage where Etch 2 was scheduled to take place.

4.3 Etch 2 – Collector Contact Pocket Formation

With the emitter and base contacts formed, as well as the base pedestal area defined, the last major step in the HBT construction process involved creating the pocket in which the collector contact metal would be deposited. This process, occurring in the collector contact stage, was the second and final step where build conditions would be modified. The collector contact etch (Etch 2) is a timed wet etch step where the first step is calculating the etch rate of the chemical bath. This is accomplished by using the measurement data from the previous run. As more and more wafers are etched in the chemical solution, the added semiconductor material removed in the etch changes the etch rate properties of Etch 2 and recipe times need to be continually adjusted.

Using this method, the desired etch times for the various HBT build conditions were calculated. Before processing, all five wafers were measured at the automated surface profiler to obtain the pre-etch measurements. Using test structures specifically open for the collector contact etch, the stylus measured the etch depths at three locations: top, center, and bottom, where the mean value was recorded. The wafers were then individually processed through Etch 2 according to the calculated etch times. Each wafer was loaded into a separate Teflon cassette and processed on the automated wet etch bench for Etch 2. The Teflon cassette for each build condition was loaded onto the load station platform and picked up by an automated robot arm, then submerged in the etchant solution for the specified recipe time. At the conclusion of the etch time, the wafer was then removed from the etchant chemical bath and submerged into bath of deionized
water, to immediately rinse off the etchant chemical and quench the etch. Figure 4.3 shows the automated wet bench used for Etch 2, with the load station platform shown on the left and the etchant bath on the right.

![Automated Wet Etch Bench](image)

Figure 4.3: Automated Wet Etch Bench, with Load Station Platform (Left) and Etch 2 Chemical Etchant Bath (Right)

It is important to note that for the purposes of this graduate project, five separate single wafer runs were completed for Etch 2, with each run specified by the HBT build condition and its corresponding Etch 2 depth target. The single wafer runs were required due to the varied etch depths. In full volume manufacturing, the collector contact Etch 2 step is a batch process (versus single wafer processing), where the entire cassette is submerged in the etchant solution and the etch simultaneously occurs on all wafers. The right image of Figure 4.3 illustrates full lot cassettes running the standard Skyworks Solutions BiFET process for Etch 2.

The final step of the Etch 2 wet etch process was to load the wafers into a spin-rinse dryer, where the wafers were rotated at high revolutions and subjected to one final rinse of deionized water, followed by warmed nitrogen (N2) to dry. At the completion of Etch 2, the wafers were then once again loaded onto the automated surface profiler to perform the post-etch measurements and calculate the total etch depths. The recipe times
and bath etch rate are shown in Table 4.3. The pre/post measurements and the resulting Etch 2 etch depths are shown in Table 4.4.

<table>
<thead>
<tr>
<th>Recipe</th>
<th>Target Etch Depth (in Angstroms)</th>
<th>Etch Time (in Seconds)</th>
<th>Bath Etch Rate (Angstroms/second)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition 1</td>
<td>13800</td>
<td>78</td>
<td>174</td>
</tr>
<tr>
<td>Condition 2</td>
<td>11800</td>
<td>66</td>
<td>175</td>
</tr>
<tr>
<td><strong>Condition 3 (Standard)</strong></td>
<td><strong>9800</strong></td>
<td><strong>54</strong></td>
<td><strong>179</strong></td>
</tr>
<tr>
<td>Condition 4</td>
<td>7800</td>
<td>44</td>
<td>177</td>
</tr>
<tr>
<td>Condition 5</td>
<td>5800</td>
<td>33</td>
<td>179</td>
</tr>
</tbody>
</table>

Table 4.3: Etch 2 Recipe Times and Etch Rate by Condition

<table>
<thead>
<tr>
<th>Wafer Build Condition</th>
<th>Pre-Measurement</th>
<th>Etch Time (in seconds)</th>
<th>Post-Measurement</th>
<th>Mean Etch Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition 1</td>
<td>17022</td>
<td>78</td>
<td>30575</td>
<td>13553</td>
</tr>
<tr>
<td>Condition 2</td>
<td>17146</td>
<td>66</td>
<td>28705</td>
<td>11559</td>
</tr>
<tr>
<td>Condition 3</td>
<td>17161</td>
<td>54</td>
<td>26802</td>
<td>9641</td>
</tr>
<tr>
<td>Condition 4</td>
<td>17147</td>
<td>44</td>
<td>24928</td>
<td>7781</td>
</tr>
<tr>
<td>Condition 5</td>
<td>17256</td>
<td>33</td>
<td>23175</td>
<td>5919</td>
</tr>
</tbody>
</table>

Table 4.4: Etch 2 Depth Measurement (All Values in Angstroms)

The measurements show that the actual resulting mean etch depths were accomplished within acceptable tolerance of +/- 5.0 % from the targeted values. Varying the recipe times for Etch 2, the collector contact pocket was defined per the desired HBT build conditions. With a total targeted etch depth of 14800 A, the combination of Etch 1 and Etch 2 successfully accomplished the objective of creating the HBT build conditions outlined in this graduate project. The results of the total etch depth created by Etch 1 and Etch 2 are illustrated in Table 4.5.

<table>
<thead>
<tr>
<th>Wafer Build Condition</th>
<th>Etch 1 Depth</th>
<th>Etch 2 Depth</th>
<th>Total Etch Depth</th>
<th>Difference from Target (14800)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition 1</td>
<td>1139</td>
<td>13553</td>
<td>14692</td>
<td>-108</td>
</tr>
<tr>
<td>Condition 2</td>
<td>3114</td>
<td>11559</td>
<td>14673</td>
<td>-127</td>
</tr>
<tr>
<td>Condition 3</td>
<td>5195</td>
<td>9641</td>
<td>14836</td>
<td>36</td>
</tr>
<tr>
<td>Condition 4</td>
<td>6851</td>
<td>7781</td>
<td>14632</td>
<td>-168</td>
</tr>
<tr>
<td>Condition 5</td>
<td>8684</td>
<td>5919</td>
<td>14603</td>
<td>-197</td>
</tr>
</tbody>
</table>

Table 4.5: Total Etch 1 and Etch 2 Depth Measurement (All Values in Angstroms)
Through the in-line measurement of the etch depths for the base pedestal etch (Etch 1) and the collector contact (Etch 2), it was able to be observed that the desired etch depth targets were successfully achieved. The next step in the process would be to verify the base-collector profile, which is the topic of the next section.

### 4.4 FIB Cross-Section Verification

The profile of the base-collector regions formed by Etch 1 and Etch 2 were verified through a method referred to as FIB. The term is an acronym for *focused ion beam* and is commonly processed on tools known as FIB microscopes. In this process, a sample is placed under vacuum, where the majority of all moisture and air particles are removed from the environment. An ion beam of Gallium is formed, with each ion accelerated with an energy of approximately 30 keV. The beam is focused onto the desired area of the sample, where the bombarding Gallium ions sputter or remove material exposed to the beam. The amount of current in the beam designates how much material is removed and how deep the area of removal is defined. The removed area, known as a FIB cut, exposes a cross-section of the sample on the sidewalls of the cut. From there, a scanning electron microscope (SEM) is positioned at a 52 degree angle from the sample, allowing an image to be displayed of the cross-sectioned sample. An example of a SEM image performed on a FIB cut is shown in Figure 4.4.

![Figure 4.4: Example of FIB Cut and Cross-Section](image-url)
For the purposes of this project, the FIB of each experimental condition was completed at the end of the HBT construction process. The FIB cuts were made to provide a one-dimensional view of the HBT structure and profile of the base-collector region. The formation of the various base pedestal structures were observed and compared to the control base pedestal depth condition of 5000 A, shown in Figure 4.5.

![Figure 4.5: Cross-Section of Standard Base Pedestal (Control, 5000 A BP)](image)

The FIB and cross-sections of the various wafer conditions provided visual verification of the base-collector profiles formed by modifying the HBT construction processes at Etch 1 and Etch 2. This visual comparison is shown in Figure 4.6.

![Figure 4.6: Comparison of Base Pedestal Formation by HBT Build Condition](image)
Based upon the mechanisms of the dry etch for Etch 1 and the wet etch for Etch 2, the cross-sections show the effect of the different etches on the base-collector regions. The profile is shaped depending on when the undercut of the wet etch process for Etch 2 was introduced. For HBT build conditions 1 and 2, the undercut is introduced earlier than the control process, showing more of the collector semiconductor material removed than the standard condition. Vice-versa, the undercut of Etch 2 is introduced later than the control process, showing a deeper negative slope (formed by Etch 1) and more semiconductor material than the standard condition. Will these changes in the base-collector regions of the various HBT build conditions show any impact to HBT performance? The device electrical test and measurements of this graduate project are presented in Chapter 5.
Chapter 5: Electrical Measurements & Device Performance

5.1 Process Control Monitor

Measurements of the five HBT build conditions were performed on a testable structure known as a process control monitor, or PCM. These PCM sites are located in the center of the reticle used in the photolithography process discussed at the beginning of Chapter 4. The reticle comprises the set of patterns to be imaged onto the wafer in one field. Once one field is exposed on a wafer in an optical stepper, the wafer is moved (i.e. a step is taken) and the exposure is repeated until the entire wafer is patterned \textsuperscript{[3]}. Figure 5.1 shows an example of a reticle field exposure pattern onto the wafer. While the PCM in Figure 5.1 is shown in the lower left corner of the reticle field, this is for illustrative purposes only. The actual PCM sites tested in this graduate project were located in the center of the reticle field, surrounded by device die.

![Figure 5.1: Example of Reticle Field and Repeated Exposure on a Wafer \textsuperscript{[4]}](image)

Two different designs of heterojunction bipolar transistors inside the PCM were used to verify the electrical results of the HBT build conditions. The two designs utilize separate layout configurations that result in different area dimensions for the emitter, base, and collector structures. The primary difference in the two HBT devices is the configuration of the emitter. The first PCM HBT design, referred to as \textit{Type 1}, uses a
horseshoe shaped emitter device. The second PCM HBT design, referred to as Type 2, uses a straight-finger emitter device. Figure 5.2 illustrates the different HBT device configurations. The contact metals for the emitter, base, and collector regions are connected to test pads via interconnected metal lines. Figure 5.3 shows the layout of the PCM HBT devices, Type 1 and Type 2, connected to the test pads via the interconnect metal.

Figure 5.2: Horseshoe Emitter Device (Left), Straight-Finger Emitter Device (Right) [5]

Figure 5.3: Horseshoe Emitter Device Layout Connected to Test Pads (Left), Straight-Finger Emitter Device Connected to Test Pads (Right)

5.2 Device Test Procedure

With PCM test structures present on each of the five varied HBT build condition wafers, measurements were performed using a semi-automated wafer test station. The test station is comprised of two main elements: 1) an Electroglas Model 2001X wafer prober and 2) a test rack equipped with a Network Analyzer and DC and RF power supplies. The wafer prober contains a heated chuck where the wafer is mounted. This chuck is heated to a constant temperature of 25° Celsius (C) to ensure all device
temperatures are controlled during testing. Fine measurement probe tips, located above the wafer chuck, are lowered directly onto the test pads, providing the contact and connection between the wafer and measurement equipment. Figure 5.4 shows the wafer test station (with wafer prober and test rack) in the left image; the wafer measurement chuck is shown in the right image.

Figure 5.4: Semi-Automated Wafer Test Station (Left), and Wafer Measurement Chuck, Mounted with a Calibration Substrate (Right)

Once the wafer chuck reaches the operating test temperature (25° C), a calibration procedure is performed for the Network Analyzer. Using a calibration substrate, shown mounted on the wafer measurement chuck in the right image of Figure 5.4, a 2-port LRM (line-reflect-match) calibration is performed. Performed over the frequency range of 900 MHz to 6.0 GHz, this procedure is completed utilizing known line (or thru), reflect, and match (or load) standards on a calibration substrate [6]. Through 2-port S-Parameter analysis, values for S11, S21, S12, and S22 are obtained for each LRM standard and compared to a specification: the power at the input of the device under test (DUT) should not exceed -20 dBm, with a power slope of 0.1 dBm/GHz. Figure 5.5 illustrates an example of S-Parameter plots obtained for one LRM standard measurement.
Once the calibration for the Network Analyzer is completed, the next step of the wafer test procedure included the parasitic de-embedding process of the device under test (DUT). This step is primarily done to isolate the contributing effects of the test pads and metal lines connected to the metal contacts of the emitter, base and collector regions of the tested HBT devices. Using a set of engineering wafers that contain the same device pad footprint as the Type 1 and Type 2 PCM HBT devices, 2-port S-Parameter measurements are taken for pad-only test structures under two configurations: 1) an OPEN structure and 2) a SHORT structure. This yielded values of the parasitic components (capacitances and inductances), as well as resistive and series losses associated with the test structures. These are subtracted from the final values obtained by measuring the wafers constructed for this graduate project.

With these initial steps completed, the process to measure the five wafers constructed for the varied HBT build conditions could finally take place. 2-port S-parameter measurements were performed on the DUT test structures. Five PCM sites on each wafer were mapped out on an automated test program, with a single Type 1 and Type 2 HBT device measured at each site, yielding ten sets of measurements for each
wafer and build condition. Figure 5.6 illustrates the location of the PCM test sites selected for measurement. The data is presented in the next two sections.

![Figure 5.6: PCM Test Sites Selected for Measurement](image)

5.3 Direct Current Parameters and Results

Full characterization of the devices built for this graduate project was performed using the semi-automated wafer test station. A complete and extensive list of electrical parameters were calculated and derived using specialized Skyworks Solutions proprietary test algorithms. For direct current (d.c.) bias conditions, two specific HBT parameters were observed for this graduate project: 1) d.c. current gain ($\beta$), also referred to as $beta$ and 2) thermal resistance, $R_{th}$, discussed in Chapter 3.

D.C. current gain beta is defined as the ratio of the collector and base currents, respectively, and is a key parameter for bipolar transistors [7]. The equation for beta is presented here: $\beta = \frac{I_C}{I_B}$, where $I_C$ is the collector current and $I_B$ is the base current. Using a Gummel plot, which is the plot of $I_B$ and $I_C$ as a function of the voltage across the base and emitter ($V_{BE}$), beta was measured and calculated for two current densities: 1) a LOW condition in mA/$\mu$m$^2$ and 2) a HIGH condition in mA/$\mu$m$^2$ for each of the HBT test structures. The horseshoe devices were classified as Type 1, while the straight-
finger devices were classified as Type 2. The results for beta, at the respective current densities, displayed through quantile box plots with standard deviation and means, are shown in Figure 5.7 and Figure 5.8. To compare the various build conditions versus the standard (HBT Build Condition #3), upper and lower specification limits defined by +/- 4 sigma from the median of HBT Build Condition #3 are also outlined in the plots.

Figure 5.7: Beta versus HBT Build Condition for Type 1 and Type 2 HBT Devices at LOW Condition (Current Density in mA/µm²)

Figure 5.8: Beta versus HBT Build Condition for Type 1 and Type 2 HBT Devices at HIGH Condition (Current Density in mA/µm²)
For the thermal resistance, $R_{th}$, the parameter cannot be completely derived on its own, but is extracted via a Skyworks Solutions custom test algorithm with the junction voltage coefficient over temperature ($\phi$) or $\text{phi}^{[8]}$. While $\phi$ is not completely a constant term, it is approximately in the range 1.1 mV/°C. For the purposes of comparing the thermal resistance $R_{th}$, it is identical across the different build conditions. Figure 5.9 shows the plots for $\text{phi}^* R_{th}$ for the different HBT build conditions by device type, with +/- 4 sigma limits derived from the median of the control wafer.

![Figure 5.9: (Phi* Rth) versus Build Condition for Type 1 and Type 2 HBT Devices](image)

### 5.4 RF Parameters and Results

Under RF bias test conditions, the primary parameter observed for this graduate project was the base-collector junction capacitance, $C_{jc}$, discussed in Chapter 3. The bias conditions for this test were performed at 0 V, with both the voltage across the base and emitter ($V_{BE}$) and the voltage across the collector and emitter ($V_{CE}$) set equal to zero. Performing 2-port $S$-parameter measurements over a frequency range of 0.9 GHz to 5.9 GHz, the base-collector junction capacitance, $C_{jc}$, was accurately calculated by de-embedding the parasitics discussed in Section 5.2. Figure 5.10 shows the results of the base-collector junction capacitance, $C_{jc}$, for the different HBT build conditions by device type. Figure 5.11 shows the same data, but only for the window of defined values designated by +/- 4 sigma from the control wafer (HBT Build Condition #3).
One key figure of merit that characterizes the performance of heterojunction bipolar transistors at high frequencies is the cutoff frequency \( f_T \), defined as the frequency at which the current gain \(|h_{21}|\) is equal to unity (or 1) \[^9\]. The cutoff frequency \( f_T \) was extracted at three different current density conditions (LOW, MID, and HIGH), with the voltage across the collector and emitter \( (V_{CE}) \) set to 1.5 V. Figure 5.12, Figure 5.14, and Figure 5.16 each show the measurements for \( f_T \) at the respective current density.
conditions (LOW, MID, and HIGH). Figure 5.13, Figure 5.15, and Figure 5.17 show the same sets of data, but only for the window of defined values designated by +/- 4 sigma from the median of the control wafer (HBT Build Condition #3).

Figure 5.12: Cutoff Frequency ($f_T$) at LOW mA/µm² and $V_{CE} = 1.5$ V versus Build Condition for Type 1 and Type 2 HBT Devices

Figure 5.13: Cutoff Frequency ($f_T$) at LOW mA/µm² and $V_{CE} = 1.5$ V versus Build Condition for Type 1 and Type 2 HBT Devices, with +/- 4 Sigma Window
Figure 5.14: Cutoff Frequency ($f_T$) at MID mA/µm$^2$ and $V_{CE} = 1.5$ V versus Build Condition for Type 1 and Type 2 HBT Devices

Figure 5.15: Cutoff Frequency ($f_T$) at MID mA/µm$^2$ and $V_{CE} = 1.5$ V versus Build Condition for Type 1 and Type 2 HBT Devices, with +/- 4 Sigma Window
With the test measurements of all five HBT build conditions complete and the desired HBT performance parameters calculated, the data was analyzed and key observations were made. The discussion of the test results, observations, and overall conclusion are presented in Chapter 6.
Chapter 6: Conclusion

6.1 Discussion of Results

The set of measurements obtained from the semi-automated wafer test station allowed for full characterization of the HBT devices constructed for this graduate project. From the measurements, a list of electrical parameters was calculated and derived using specialized test algorithms for each of the wafers representing the five HBT build conditions. These sets of data allowed for direct comparison of HBT performance parameters between the various HBT build conditions. As a visual aid, upper and lower specification limits, defined by +/- 4 sigma from the median of the standard wafer (HBT Build Condition #3), were displayed in each of the plots. As a result, observations could be easily made in comparing the various HBT build conditions to the control HBT device constructed from the standard Skyworks Solutions BiFET HBT construction process.

Analysis began with the parameters obtained under d.c. bias conditions: d.c. current gain ($\beta$) beta and the thermal resistance $R_{th}$, extracted via the product $\phi^* R_{th}$. These results, shown in Figure 5.7, Figure 5.8 and Figure 5.9, illustrated that there was little difference between the values of the various HBT build conditions. For beta and $R_{th}$, each of the wafers was within the acceptable +/- 4 sigma window defined by the median value of the control condition (HBT Build Condition #3). The results answered one of the key questions presented as a project goal and objective; for thermal resistance $R_{th}$, the depth and formation of the base pedestal has little influence to the heat dissipation of an HBT device. As detailed in Section 2.2, the primary location of the thermal properties of the device occurs at the emitter-base junction, and the heat generated by the movement of electrons from the emitter through the base to the collector is completely dissipated through the base and collector/sub-collector. Varying the base pedestal depth and altering the base-collector profile of an HBT had no impact.

Moving to the RF bias test conditions, the primary parameter observed for this graduate project was the base-collector junction capacitance, $C_{jc}$. Examining Figure 5.10, it was clearly seen that the devices from HBT Build Condition #1 were significantly
different than the devices from the other build conditions. This build condition represented the most shallow base pedestal depth of all the HBT devices constructed (1000 A), therefore representing the lowest base-collector effective area of all the conditions. It was theorized in Section 2.4 that there existed a dependence of $C_{jc}$ on the base-collector effective area, and that decreasing the base pedestal depth would decrease the amount of doped semiconductor material beneath the base-collector junction area and hence decrease the value of $C_{jc}$. However, the results show that the mean junction capacitance $C_{jc}$ of the Condition 1 wafer (82.0333 fF) was twice as much all of the other conditions, with a range of almost 40 fF between the maximum and minimum values and a standard deviation of 16.623. This was a completely counter to the expected result and ultimately led to the question of why?

The answer was found in examining the FIB and cross-sections of the devices of HBT Build Condition #1. In examining the structure, it was observed that the base pedestal formed by the target of 1000 A of Etch 1 did not completely break through the base layer into the collector region. Figure 6.1 shows the cross-section of an HBT Build Condition #1 device, both at low and high magnification. The two white arrows define the illustrated thickness of the base layer, with the red line designating the base collector junction. It can be seen that the negative slope formed by the Etch 1 process ends and forms the plateau within the base region.

![Figure 6.1: Low and High Magnification of Base Pedestal for HBT Build Condition #1](image)
Examining the FIB cross-section images obtained for HBT Build Condition #2 (3000 A base pedestal depth) and HBT Build Condition #3 (standard 5000 A base pedestal depth) showed that the negative slope for each of the respective conditions extended beyond the base layer into the collector region. Figure 6.2 shows the HBT Build Condition #2 on the left, and HBT Build Condition #3 on the right. Reviewing the values for the junction capacitance $C_{jc}$ for these conditions did not show the same high values as HBT Build Condition #1.

By not etching completely through the base layer, it was found that a significant amount of leakage was occurring at the base-collector junction for HBT Build Condition #1, and thereby affecting the measurement for the junction capacitance $C_{jc}$. The negative slope profile formed by the Etch 1 process is concluded to have a major role in providing a sufficient leakage barrier between the base and collector region. It is theorized that the polymers, a byproduct of the chemical and physical reactions, serve to damage the semiconductor material exposed to the etch creating proper isolation along the profile of the base pedestal. If the slope does not extend past the base-collector junction, a leakage issue between the two HBT regions will occur. Figure 6.3 illustrates the base-collector leakage values for the various HBT build conditions. The plot on the left shows the range for all values of $bclk$ (base-collector leakage) while the plot on the right is zoomed in to provide better resolution. It can be seen that as the pedestal depth is increased, $bclk$ decreases.
Continuing the analysis, Figure 5.11 excluded the result of the base-collector junction capacitance for HBT Build Condition #1 and examined the other build conditions. It was observed that the two devices, Type 1 and Type 2 had a separate response in their values of $C_{jc}$. For the Horseshoe emitter Type 1 HBT devices, all values of $C_{jc}$ were nearly identical to the standard condition. For the straight-finger emitter Type 2 HBT devices, the value of $C_{jc}$ increased with base pedestal depth, supporting the primary theory in this graduate project. With the decrease in base pedestal depth and base-collector effective area, the base-collector junction capacitance decreased. Similarly, increasing the base pedestal depth and base-collector effective area increased the base-collector junction capacitance for the Type 2 HBT devices. Type 1 did not see this response. Would this change in $C_{jc}$ for Type 2 HBT devices be enough to affect device performance?

Analyzing the high frequency key HBT figure of merit $f_T$ would provide the answer. In observing the values of $f_T$ at the various current densities in Figure 5.12 through to Figure 5.17, it was seen that the differences between the HBT build conditions were negligible (outside of HBT Build Condition #1). The small difference in $C_{jc}$ of the Type 2 HBT devices did not reflect any significant change to the high frequency response of the HBT devices constructed. It is concluded that the amount of undercut provided by the Etch 2 process for the various HBT build conditions was not sufficient enough to provide a significant impact to $C_{jc}$. The amount of semiconductor material added or
removed in the base-collector profile by varying the base pedestal depth was negligible for the purposes of this graduate project (outside of HBT Build Condition #1). The innovative technique attempted in the modification of the HBT construction process to improve HBT device performance was not realized with the existing conditions attempted in this graduate project.

6.2 Summary and Conclusion

While there were no significant improvements in performance, evaluating the build conditions from this graduate project did yield a beneficial outcome from a factory manufacturing perspective. It was observed that the devices built with a base pedestal depth of 3000 A (HBT Build Condition #2), were statistically comparable to the devices built with the standard base pedestal depth of 5000 A (HBT Build Condition #3). There was little difference in the electrical performance of the HBT devices between the two build conditions. As shown in Section 4.2, the etch time for HBT Build Condition #2 was 40 seconds per wafer, versus an etch time of 70 seconds per wafer for the standard base pedestal depth for HBT Build Condition #3. This represents a decrease of 30 seconds per wafer for the Etch 1 process. Recall that Etch 1 occurs in the dry etcher tool and is a single wafer process, where the wafers are individually etch in a serial sequence until all wafers in the wafer lot are complete. This represents a time savings of 10 minutes of Etch 1 processing time for every 20 wafer lot.

The change to the Etch 2 process to compensate for the shallow base pedestal would only be an additional 12 seconds submersion in the etchant chemical bath, achieved concurrently on all wafers through the batched chemical dip. This time savings equates to additional tool capacity and manufacturing efficiency at the Etch 1 dry etch process, which is a bottleneck stage based upon the length of time required for the etch. By making a global change to Skyworks Solutions BiFET process at the Etch 1 dry etch stage, the improvement will serve to be extremely beneficial as factory volume is ramped through production.

Overall, the purpose and goal of this graduate project was to take an existing, production released heterojunction bipolar transistor design and modify the construction
process to test an innovative theory and technique to improve device performance. While the results did not quantify any responses in performance, the efficiency and capacity improvements realized from a factory manufacturing perspective did provide benefits to be implemented and applied.

6.3 Future Work

The RF IC devices from HBT Build Condition #2 will be used in a front-end module package and subjected to device reliability testing. The reliability testing is part of the standard qualification procedure for new construction process changes and serves to stress the part under various conditions to evaluate the ruggedness and dependability. In addition, the control wafer for HBT Build Condition #3 will go through the identical process to serve a baseline for comparison. In addition, further work will be completed in attempting to further increase the undercut mechanism that results from the Etch 2 wet etchant process. The theory detailed in this graduate project will look to be realized in order to meet the continuing and evolving requirements for device performance.
References


