CALIFORNIA STATE UNIVERSITY, NORTHRIDGE

Survey and Study of MICROPROCESSORS

A graduate project submitted in partial satisfaction of the requirements for the degree of Master of Science in Engineering

by

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The graduate project of Henry H. Liu is approved:

Committee Chairman

California State University, Northridge

August, 1974

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FIGURES

SYMBOLS AND ABBREVIATIONS

1.	μP	:	Micro Processor
2.	μComputer	:	Micro Computer
3.	LSI	:	Large Scale Integration
4.	CPU	:	Central Process Unit
5.	MOS	:	Metal Oxide Semiconductor
6.	TTL	:	Transistor Transistor Logic
7.	(C,CM) ROM	:	(Control, Command) Read Only Memory
8.	RAM	:	Random Access Memory
9.	PC	:	Program Counter or Printed Circuit
10.	POS	:	Point of Sale
11.	JCN	:	Jump on Condition
12.	I/O	:	Input/Output
13.	CRT	:	Cathode Ray Tube
14.	ALU	:	Arithmetic Logic Unit
15.	μsec	:	Micro-second
16.	Sync	:	Synchronization
17.	MHz	:	Mega Hertz
18.	KHz	:	Kilo Hertz
19.	OPR	:	Operation Register
20.	OPA	:	Operation Address
21.	S.R.	:	Shift Register
22.	INT	:	Interrupt
23.	INTE	:	Interrupt Enable
24.	HLDA	:	Hold Acknowledge
25.	$\overline{WR}$	:	Not Write
26.	DBFL	:	Data Bus Flow
27.	HLTA	:	Halt Acknowledge
28.	INTA	:	Interrupt Acknowledge
29.	INP	:	Input
30.	OUT	:	Output
31.	RI/WO	:	Read Input/Write Output
32.	MEMR	:	Memory Read
33.	DMA	:	Data Memory Access or Direct-Memory Access
34.	CMOS	:	Complementary Metal Oxide Semiconductor
35.	PPS	:	Parallel Processing System
36.	IR	:	Instruction Register
37.	DB	:	Data Bus
38.	MUX	:	Multiplexer
39.	PIP	:	Programmable Integrated Processor
40.	PSW	:	Program Status Word
41.	BCD	:	Binary Coded Decimal

ABSTRACT

Survey and Study of

MICROPROCESSORS

By

Henry H. Liu

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The objective of this project is to study and investigate various microprocessors (μP) and their unique hardware and software characteristics.

A rapidly expanding technology on digital electronics field attracts interest to today's microprocessors. When used as replacements for hardwired logic, the microprocessors provide significant economies. The large-scale integration (LSI) chip performs the basic control processing unit (CPU) functions of a computer.

SECTION 1
INTRODUCTION

The purpose of this report is to study and update today's digital technology. In the expanding digital world, the microprocessors play the most significant role; anywhere the one use hardwired logic, should consider a microcomputer as a cost effective alternative. The rule of thumb is: If ones design uses more than 30 TTL integrated circuit chips, then using a microcomputer should be considered. A microcomputer would save months of new system design time and money in costly redesigns to meet new customer requirements by hardware techniques.

The report makes a very complete survey and study of today's microprocessors for most users. Any reader interested in microprocessors and computers should find this study a very comprehensive round up of good "bench mark" information. The compilation of this report is to look at:

1. Microprocessors and Microcomputers.
2. What's available in today's manufacturers of "microproducts".
3. Future sources of microproducts.

Therefore, the report will provide the reader the information to select the one which best fits his new system design requirements. This is one area which has been neglected in previous compilations.

The many applications of this device make it a powerful tool. One of the accomplishments of the survey and study is to show these applications; the report shows several examples of these applications and the potential of the microprocessor.

SECTION 2

THE MICROPROCESSOR

The state-of-the-art microprocessor

A microprocessor is a general purpose digital processing unit contained on a set of MOS-LSI chip. Contained with the microprocessor is the processing unit itself, a set of registers, a control unit--usually microprogrammed, and a rudimentary set of I/O and interrupt logic. Frequently, several TTL packages are required for buffering and level conversion. Required with the microprocessor in any system application are a read/write memory for data, another memory --possibly read/write but usually read-only for the program (not to be confused with the control read only memory, CROM, which is used to implement the basic instruction set), and circuits for performing the required input/output operations. Figure 1 shows Functional Blocks of a Microprocessor.

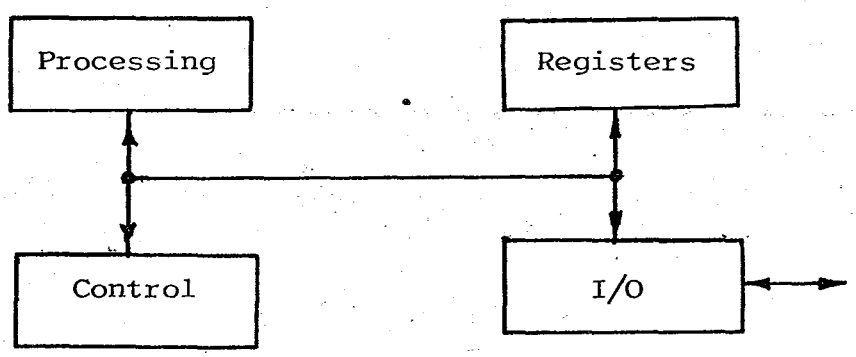
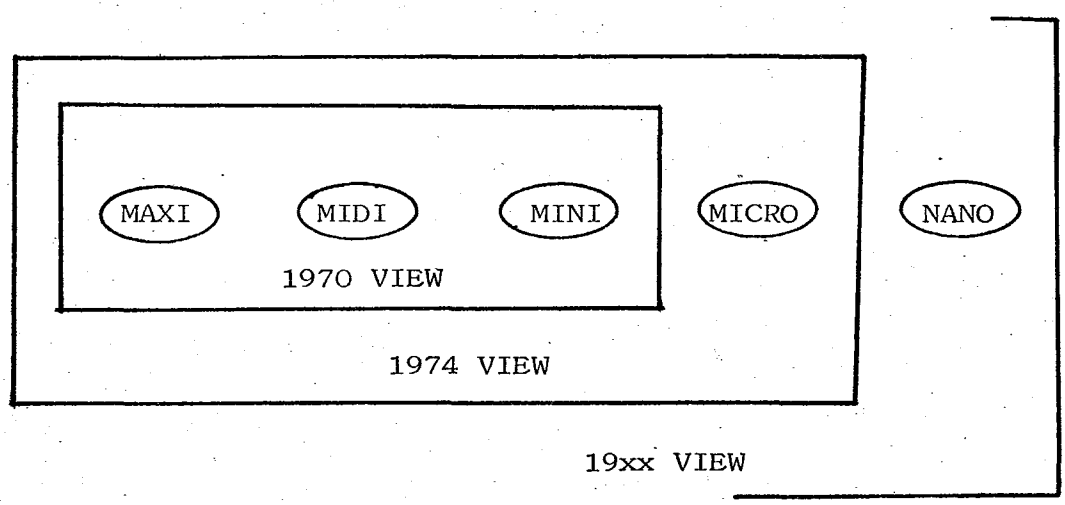


Figure 1. Functional Blocks of a Microprocessor



CDC 7600	B1700	PDP/11	MCS/8	xx	EXAMPLES
B6700	370/115	NOVA	PPS/4		
370/168	HP 3000	SYS/3	GPC/P		
> $1M	$100-1000K	$10-100K	$50-1000		SYSTEM COST

Figure 2. μ Computer capability transfer thru technology

Microcomputer

The distingushing characteristic or component of a microcomputer is the microprocessor. A typical 0.16-inch square package(thus the "micro" designation) are the usually elements of any processor. The devices are fabricated by metal oxide semiconductor(MOS) techniques. MOS offers extremly high

densities of transistors-per-unit-area, but is inherently slower than bipolar devices. Current MOS speeds for a logic element or chip range from 40 nanosec for fast, n-channel silican gate devices, to 200 nanosec for p-channel metal units. It is fair to say that an LSI microprocessor has a substantial cost advantage over a typical minicomputer CPU. For example, a complete LSI CPU may be purchased for as little as $120, compared to $1000 to $2000 for a minicomputer CPU(See Figure 2.)

The CPU power consumption of an LSI microcomputer is 66-75 percent less than that of a comparable minicomputer. For a system containing but one CPU the difference would not be significant considering the overall system's power requirements. However, in application where many CPUs are required, the power differences would be substantial.

A MOS /LSI microcomputer operates at 50 to 33 percent of the speed of commercially available minicomputers. Typical memory-to-memory add times for a moderately priced mini are between 5 and 20 microsecond compared to 15 to 60 microsecond for a microcomputer. The speed of a microcomputer is derived from the particular MOS process used in fabrication. As these processers improve, so will the speed.

With integrated circuits, system reliability is largely a function of the number of printed circuit (PC) board interconnections. Since each LSI package replaces from 50 to 100

TTL packages, the interconnections required by microcomputers are reduced and total system reliability is increased, The LSI microcomputer can be built into a light and compact configuration because of the higher number of gates per package module and the simplicity of interconnection.

Microprocessor architecture is similar to that of a bus-oriented minicomputer. Applications can generally be categorized by bit width; four-bit microprocessors for calculators; eight-bit units for microcontrollers; and sixteen-bit units for microcomputers. The range of characteristics is broad:

Data Word Size	4 to 100 bits
Instruction Set	40 to 120
Instruction Format	8 to 24 bits
ROM	400 23 bit to 16K 8-bit
RAM	up to 65K 16-bit
General-purpose Registers	1 to 16
Cycle Time to Fetch & Execute an Instruction	0.54 to 62 μsec. with 5 to 10 μsec. common
Stack Depth	2 to 32 levels
Interrupt Capability	None to full
Parallelism	mostly parallel to serial/parallel

Applications of Microprocessors

The potential applications of microprocessors extend over a broad spectrum of products. Their principal use to date has been in electronic calculators--the extremely high volume quantities required by this market segment dictating the architecture of many microcomputers..

Terminals will be the next major market area to utilize microcomputers. Low-cost data terminals use microprocessors for simple data handling tasks. Remote terminals, by the addition of a microprocessor become "intelligent" and perform off-line editing, compiling and processing. Point-of-sale (POS) terminals perform calculations, data storage and inventory control functions, and control keyboard, tag reader, display and printer peripherals under microcomputer control.

Microprocessors are useful for tasks normally associated with large-scale systems. In addition to performing channel control functions, they relieve the large central processor of the overhead associated with scheduling, text editing or file management. In a similar manner, microprocessors can be used for sequencing, control, formatting and error detection in tape or disc units. It is probable that more microprocessors will be buried in computer peripherals than will be used as computing devices.

LSI microprocessors, combined with low-cost memory and moderate performance peripherals like floppy discs,

CRT displays or medium-speed printers, can provide all the processing power needed for many applications. A large multi-user computer system may soon be needed only for accessing large, on-line data bases or for a few CPU-bound program tasks. Microprocessors and microcomputers are or soon will be applied to the following types of equipment:

Calculators, both programmable and fixed-function, and small business/accounting computers

Terminals, both keyboard and special-purpose

Measurement systems, from panel meters to full-scale monitoring systems

Automotive systems and traffic controls(Figure 3)

Medical equipment

Process and machine control

Computer peripherals and system control.

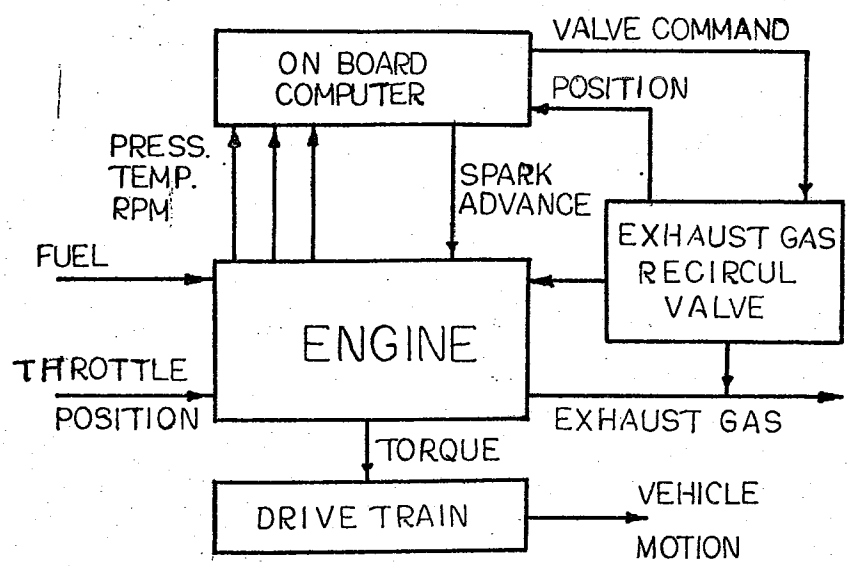


Figure 3. Economy car

The LSI microcomputer offers better price-performance, lower power consumption and heat dissipation, higher reliability, and smaller physical size than a mini-computer. The microcomputer further offers the flexibility of microprogramming, which, in a given application, has many advantages. Although execution speeds comparable to today's minicomputer have not yet been achieved, several architectural techniques have emerged which will eventually increase microcomputer speeds. LSI microprocessors and microcomputers will soon replace conventional minicomputers and controllers in many applications where a mini or controller is overpriced or overpowered. Microprocessors now satisfy those minicomputer applications where high speeds are not required. Speeds of minicomputers have increased over the years mainly as an enhancement due to changing technology rather than in response to an overall need. While TTL logic was the least expensive technology, very little cost reduction could be realized by producing slower minis. The advent of the LSI microprocessor thus is forcing a re-examination of minicomputer price-performance tradeoffs.

SECTION 3

THE MANUFACTURERS OF MICROPROCESSORS

BURROUGHS, Paoli, Pennsylvania

The Burroughs Mini-D is a unique departure in design. All data into and out of the little Mini-D flows serially over a 1-bit bus. The ALU operates on this serially. However, internal data storage registers are eight bits wide, and the system timing handles the bit stream in 8-bit chunks. The timing rattles data along at a fairly lively clip, taking only 1 μsec for each bit, or 9 μsec for each 8-bit chunk.

The program ROM is contained right on one chip as in the calculators. It can contain up to 256 of the 12-bit wide instruction words. That is rather short, even by microprocessor standards. If longer programs are needed, multiple chips must be used, with each assigned to recognize and do its portion of the processing task.

Internal organization of the processor provides for four general-purpose 8-bit registers and an 9-bit program location counter for the ROM. (There are six 8-bit registers in all.) Reference to external data storage is, like access to peripherals, through the 1-bit wide data bus.

While the microprogrammable Mini-D can be made to obey external macroinstructions, I suspect that most applications are programmed directly into the ROM. Then, as the ROM is part of the

processor chip and must be uniquely custom mask-programmed for each application, the Mini-D would be practical only for very large-volume products, such as consumer-credit terminals.

The instruction set for the Mini-D is quite obscure, having been designed for maximum flexibility within the constraint of 12 bits. But the instruction sets of all microprogrammable computers tend to be a bit obscure to outsiders, as the design goal is machine-level efficiency rather than software understandability.

INTEL CORPORATION, Santa Clara, California

Intel, an early advocate of microprocessors, markets three μPs a 4-bit parallel 4004(Figure 4), 8-bit parallel 8008 (Figure 5), and 8080 8-bit parallel chip(Figure 6).

The 4004 chip consists of a 4-bit adder, a 64-bit (16 x 4) index register, a 48-bit (4 x 12) program counter and stack (nesting up to three levels is possible), an address incrementer, an 8-bit instruction register and decoder, and control logic. Information flows between the 4004 and the other chips through a 4-line data bus. One 4004 may be combined with up to 48 ROM (4001) and RAM (4002) chips in any combination.

A typical machine cycle starts with the CPU sending a synchronization signal (SYNC) to the ROM's and RAM's. Next, 12-bits of ROM address are sent to the data bus using three clock cycles (@ .75 MHz). The address is then incremented by one and stored

in the program counter. The selected ROM sends back 8 bits of instruction or data during the following 2 clock cycles. This information is stored in two registers: OPR and OPA. The next three clock cycles are used to execute the instruction.

The ROM bank is controlled by a command ROM control signal (CM-ROM) and up to four RAM banks are controlled by four command RAM control signals ($CM\text{-}RAM_o$, $CM\text{-}RAM_1$, $CM\text{-}RAM_2$, $CM\text{-}RAM_3$). Bank switching is accomplished by the execution of the DCL (Designate Command Line) instruction.

An input test signal (TEST) is used in conjunction with the jump on condition (JCN) instruction. An external RESET signal is used to clear all registers and flip-flops. To fully clear all registers, the RESET signal must be applied for at least 8 instruction cycles (8 x 8 clock periods). After RESET the program will start from "O" step and $CM\text{-}RAM_o$ will be selected. The instruction repertoire of the 4004 consists of:

(a) 16 machine instructions (5 of which are double length).

(b) 14 accumulator group instructions.

(c) 15 input/output & RAM instructions.

The characteristics of 4004 summarized:

1. 4-Bit Parallel CPU with 45 Instructions
2. Instruction Set includes Conditional Branching, Jump to Subroutine and Indirect Fetching
3. Binary and Decimal Arithmetic Modes

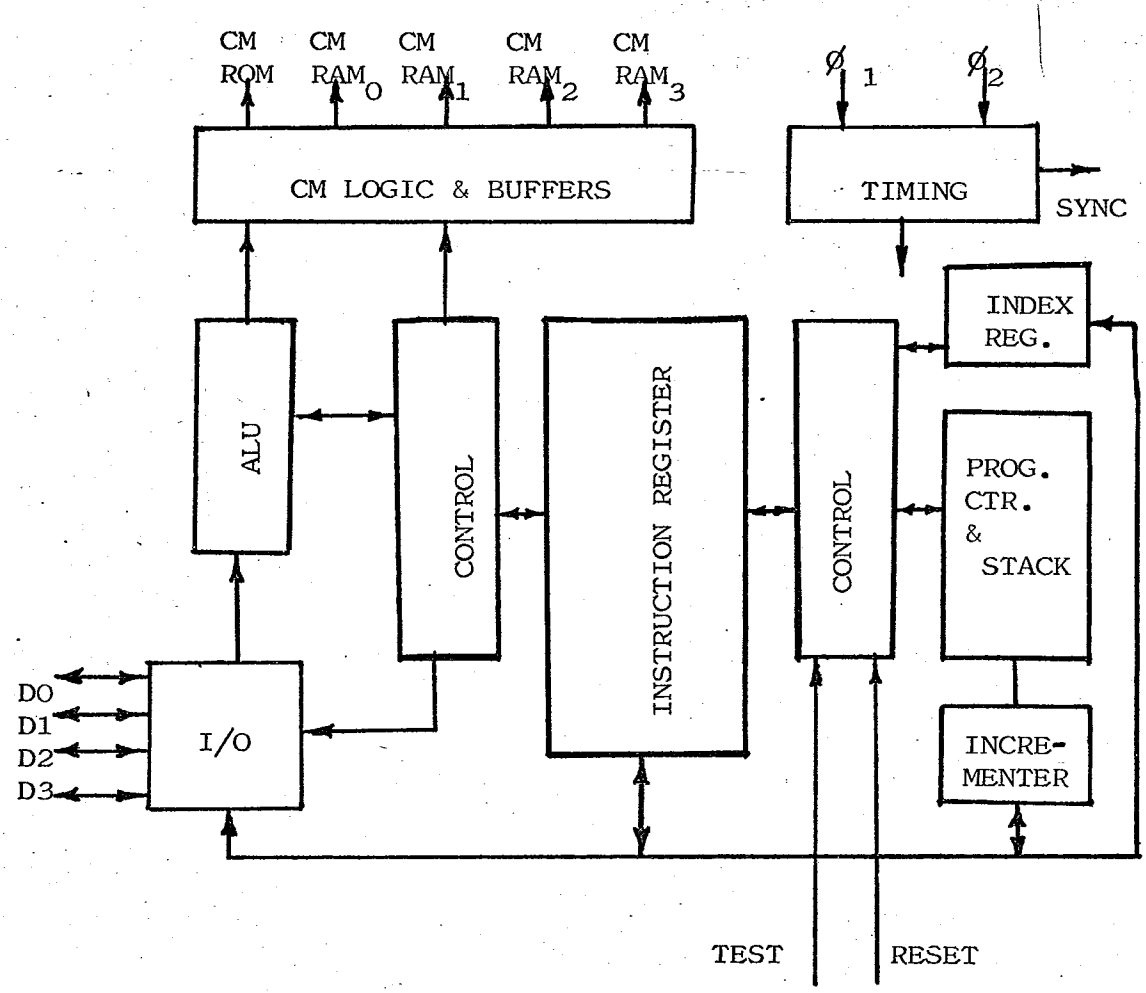


Figure 4. Intel 4004 μP blocks

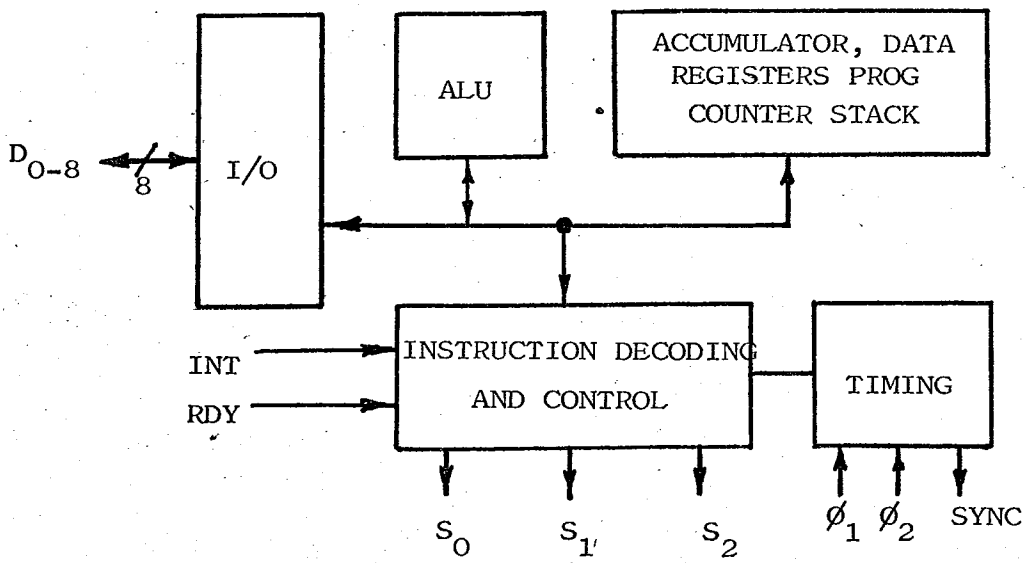


Figure 5. Intel 8008 μP blocks

4. Addition of Two 8-Digit Numbers in 850 Microseconds
5. 2-Phase Dynamic Operation
6. 10.8 Microsecond Instruction Cycle
7. CPU Directly Compatible with MCS-4 ROMs and RAMs
8. Easy Expansion - One CPU can Directly Drive up to 32,768 bits of ROM and up to 5120 bits of RAM.
9. Unlimited Number of Output Lines
10. Packaged in 16-Pin Dual In-Line Configuration

The 8008 is a single chip MOS 8-bit parallel central processor unit. A microcomputer system is formed when the 8008 is interfaced with any type or speed standard semiconductor memory up to 16K x 8-bit words.

The processor communicates over an 8-bit data address bus (D_0 through D_7) and uses two input leads (READY and INTERRUPT) and four output leads (S_0, S_1, S_2, and Sync) for control. Time multiplexing of the data bus allows control information, 14-bit addresses, and data to be transmitted between the CPU and external memory.

This CPU contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits (carry, zero, sign, parity), and an 8-bit parallel binary arithmetic unit which implements addition, subtraction, and logical operations. A memory stack containing a 14-bit program counter and seven 14-bit words is used internally to store program and subroutine addresses. The 14-bit address permits the direct

addressing of 16K words of memory (any mix of RAM, ROM or S.R.).

The control portion of the chip contains logic to implement a variety of register transfer, arithmetic control, and logical instructions. Most instructions are coded in one byte (8 bits); data immediate instructions use two bytes; jump instructions utilize three bytes. The 8008 operates with a 500 kHz clock, and executes non-memory referencing instruction in 20 microsec the 8008-1 operates with an 800 kHz clock and executes non-memory referencing instructions in 12.5 microseconds.

All inputs (including clocks) are TTL compatible and all outputs are low power TTL compatible.

The instruction set of the 8008 consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutine.

The normal program flow of the 8008 may be interrupted through the use of the INTERRUPT control line. This allows the servicing of slow I/O peripheral devices while also executing the main program.

The READY command line synchronizes the 8008 to the memory cycle allowing any type or speed of semiconductor memory to be used.

The characteristics of 8008 summarized:

1. 8-Bit Parallel CPU on a Single Chip.
2. 48 Instructions, Data Oriented.
3. Complete Instruction Decoding and Control Included.
4. Instruction Cycle Time - 12.5 μs with 8008-1 or 20 μs with 8008.
5. TTL Compatible (Inputs, Outputs and Clocks).
6. Can be used with any type or speed semiconductor memory in any combination.
7. Directly addresses 16K x 8 bits of memory (RAM, ROM or S.R.).
8. Memory capacity can be indefinitely expanded through bank switching using I/O instructions.
9. Address stack contains eight 14-bit registers (including program counter) which permit nesting of subroutines up to seven levels.
10. Contains seven 8-bit registers.
11. Interrupt Capability.
12. Packaged in 18-Pin DIP.

The 8080 is a single chip MOS 8-bit parallel central processor. This CPU, like the 8008, contains six 8-bit data registers, an 8-bit accumulator, four 8-bit temporary registers, four testable flag bits and an 8-bit parallel binary arithmetic unit.

However, many improvements were made on the 8080.

1. High Speed of Operation

This CPU is able to execute non-memory referencing instructions in 2 microseconds, operating with a 2 MHz clock, which is 1/10th the time required by the 8008 using a .5 MHz clock.

2. Multiple Interrupt Handling Capability

This CPU contains a 16-bit stack pointer and a 16-bit program counter instead of an address stack with eight 14-bit locations.

A portion of the external memory can be used as a last in/first out pushdown stack addressed by the stack pointer upon the execution of a CALL, RETURN, or RESTART.

The most important improvement is that not only the program counter but also the data registers, the accumulator and the flags can be saved in the pushdown stack.

This means that multiple interrupts can be handled easily.

3. High Interfaceability with Memory and I/O Device

The 8080 CPU does not make use of the time multiplexing of the data bus for data and address as in the 8008. The 8080 contains a 16-bit tri-state address line, an 8-bit bidirectional data bus and a number of decoded control lines. (READY, INT, INTE, RESET, HOLD, HLDA, $\overline{WR}$, WAIT, SYNC and DBFL). The status information (HLTA, INTA, INP, OUT, RI/WO, MEMR, M1 and STACK) is sent out at the beginning of each machine cycle. Notice that

it is not necessary to decode the control signals and status information simplifying interface considerably. "Explanation of pin configuration" shows the detailed activity.

This CPU contains a 16-bit address latch which can be directly interfaced with up to 64K 8-bit words of memory without requiring an external address register. The address lines, moreover, send the I/O device number upon the execution of the I/O instructions. In that case, byte two of the I/O instructions can denote the I/O device number (up to 256 devices).

Communication on the address lines and the data lines can be interlocked by using the HOLD pin. When the HLDA (Hold Acknowledge) signal is issued by the CPU, the CPU is suspended and the address and data lines are forced to be in the FLOATING state. This permits "OR-tying" the address and data busses with other devices such as data memory access channels (DMA).

4. <u>The New Processor Programming Instructions</u>

The 8080 has many new instructions which are extremely useful in extending the range of applicability of the CPU. The new instruction groups are as follows:

- Direct Load/Store Accumulator
- Save, Restore Data Registers, Accumulator and Flags
- Double Length Operation in Data Registers
    - Increment/Decrement
    - Direct Load/Store (H and L)
    - Load Immediate

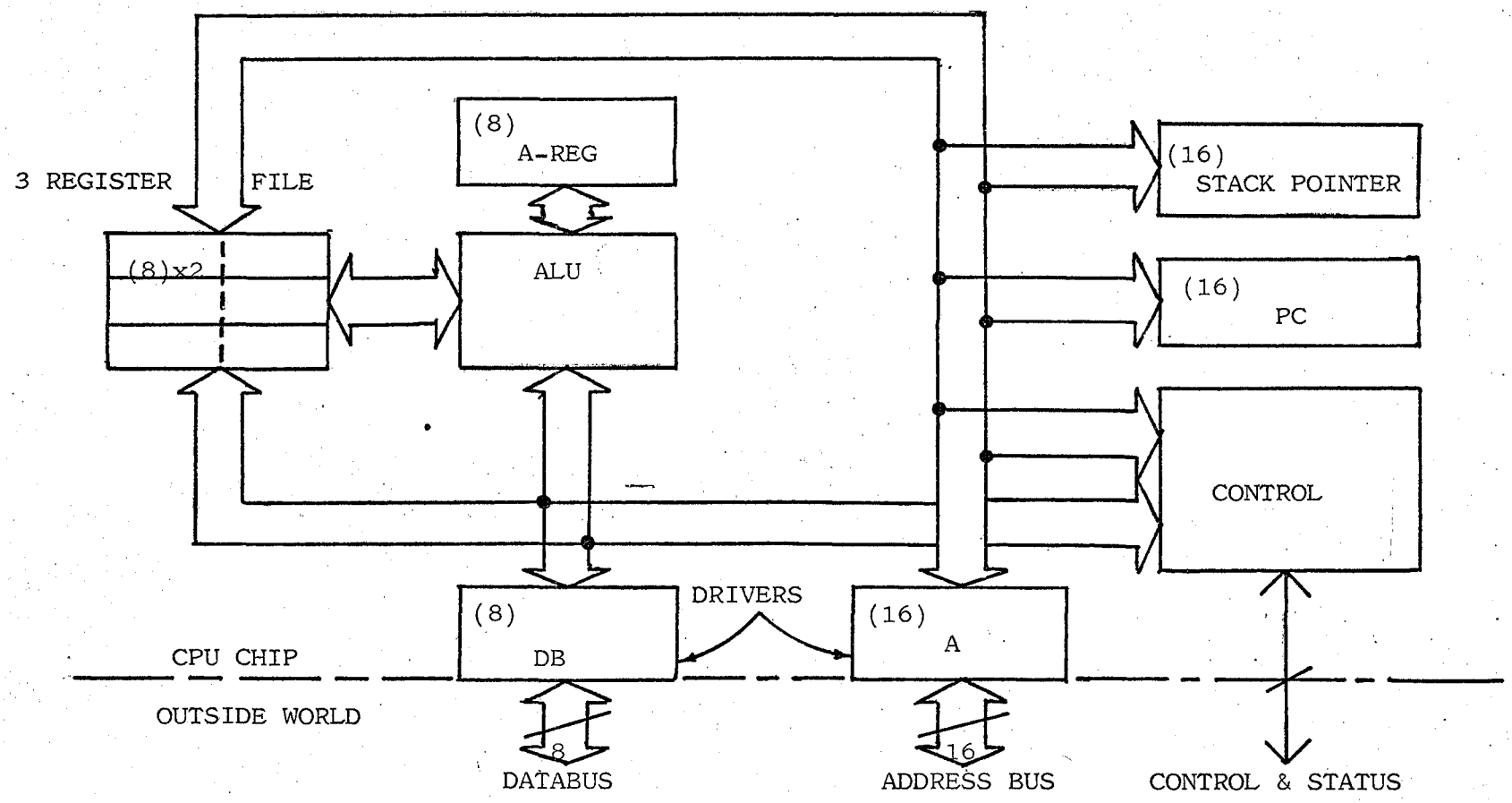


Figure 6. Intel 8080 μP blocks

- Index Register Modification
- Index Jump
- Stack Pointer Modification
- Decimal Arithmetic Package
- Set and reset interrupt enable flipflop
- Increment/Decrement Memory

INTERSIL, Cupertino, California

The ISD-8 of Intersil has been purposely patterned after the well-known DEC PDP-8 so that it can make use of the mountain of software that DEC has developed for its 10-year-old minicomputer. The Intersil microprocessor will have the identical instruction set but is expected to run about one-third slower than current PDP-8's - taking 4 μsec to do instructions that PDP-8 does in 3 μsec. The CPU of the μP version ought, however, to cost less, even though it is in the expensive CMOS technology. Intersil has laid it out in a small 160 x 190-mil chip, and because it is CMOS, it will only need a single, very low-drain, 5V power supply.

The ISD-8 will come in a 40-pin DIP package like most of the other second-generation 8's and should be available by December of this year. An Intersil source says that DEC has given the venture at least an unofficial blessing as this μP version of the ancient PDP-8 may give the old-timer yet another lease on product life.

MOTOROLA, Phoenix, Arizona

Motorola has made successful prototype chips for the CPU of its M6800 microprocessor family and expects to have the product generally available by the end of 1974. The strong point of the Motorola 8-bit'er is not so much the CPU itself, but the fact that Motorola has taken a lesson from some of the 4-bit'ers and is offering not just the CPU, but a whole family of compatible chips(See Figure 7. The Motorola 6800 CPU.)

The M6800 CPU executes instructions in 2 to 12 μsec, which is quite fast considering that, even though it is an n-channel chip, it only has the single +5V supply. It does not have any general purpose data scratch-pad registers on the CPU like most of the other 8-bit systems. But, it does have some direct addressing instructions that can bring data into the accumulators (there are two accumulators) in 3 μsec. Because of their compact 1-byte addresses, these "direct" instructions can only reach the first 256 locations in external memory.

To its credit, the M6800 CPU has a genuine index register which is a full 16-bits long. Some other μP manufacturers have been trying to pass off general registers as index registers, when in fact indexing in the true sense is not possible with them. (There is a similar misuse of the term "indirect addressing" in μP sales literature.)

In most other respects, the M6800 would appear to be similar to the Intel 8080, for the M6800 has a 16-bit stack pointer

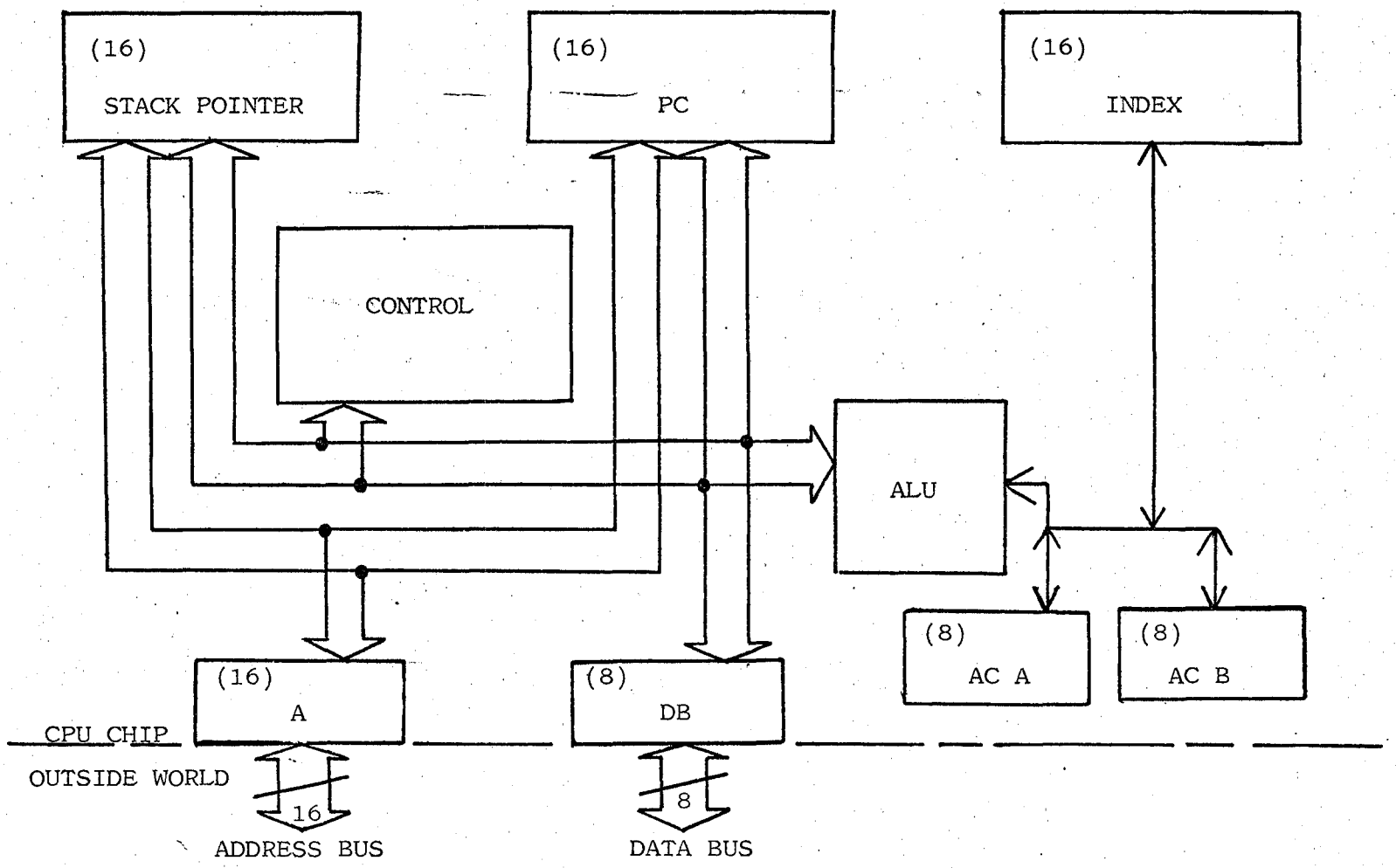


Figure 7. The Motorola 6800 CPU

and BCD capability in its ALU.

The RAM that Motorola is offering in the M6800 family ought to find uses in the general marketplace as well, for it is organized as full 8-bit bytes (128 x 8) and has a bi-directional, tri-state data port. All of the M6800 devices have bi-directional, tri-state data ports so they can be strung without further ado on a common data bus. The ROM is organized as 1024 x 8. Of course, these M6800 family memory devices are only intended for systems with limited memory needs. In applications where sizable amounts of RAM are needed, the designer will want to switch to banks of large 4k x 1 for the sake of economy (despite the nuisance of multiple power supplies and dynamic operation).

RCA, Somerville, New Jersey

The RCA microprocessor appears to be the most "symmetrical" μP offered to date. Its architecture designers selected "rational" instruction codes, without concern for missing bit patterns. There is - like in the Intel 8080 - a central register bank that has a RAM matrix of sixteen 16-bit registers. These can be accessed from memory address or data side, either full-width for memory addressing or half-width as data bytes. But the RCA architecture provides even more software flexibility for getting at these registers than in the Intel 8080.

There are three sets of 4-bit pointer registers that can be used to address any of the sixteen 8-bit halves of the registers. Each of these 4-bit pointers turns the register it points at

into the function associated with that pointer. The "P" pointer identifies the register as the program-location counter. The "X" pointer selects the register that is to be used during data transfers involving indexing. The "N" pointer serves as the address half of the instruction and provides a compact 4-bit way of indirectly addressing the external RAM via the contents of the bank register at which N is pointing(See Figure 10.)

RCA designers believe that with the 4-bit pointers and the combination of these multiple 4-bit pointers, plus the combined address and data scratch pad, they have achieved one answer to the problem of obtaining efficient operation in a μP. All this despite the restriction of very short word widths.

For example, they say that with this architecture it is possible to form multiple push-down stacks in the register bank by incrementing and decrementing the address values in the pointers. Or, if deeper stacks are desired, to increment and decrement the contents of the 16-bit registers themselves to form stacks out in the external RAM. The characteristics of this architecture allow efficient I/O operations, including high-throughput direct-memory address transfers.

But it is risky to predict just when the COSMAC will be available in an economical commercial form. At present, it is implemented on two oversized prototype CMOS chips - 236 x 246 and 256 x 254 mils. RCA predicts they will be able to compress the COSMAC CPU onto a single 200-mil square CMOS chip and sell it

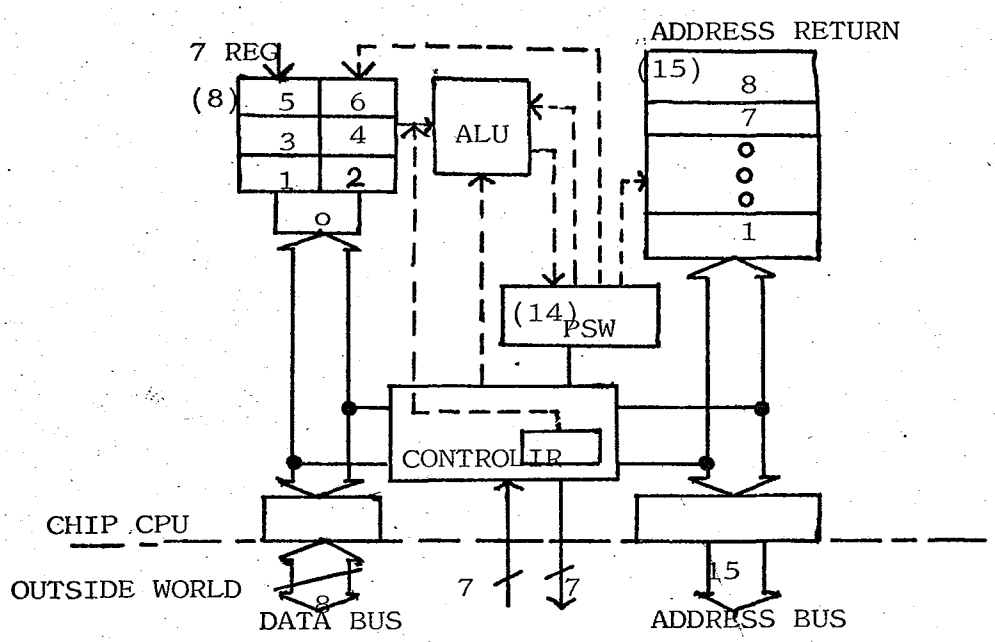


Figure 9. The Signetics PIP CPU

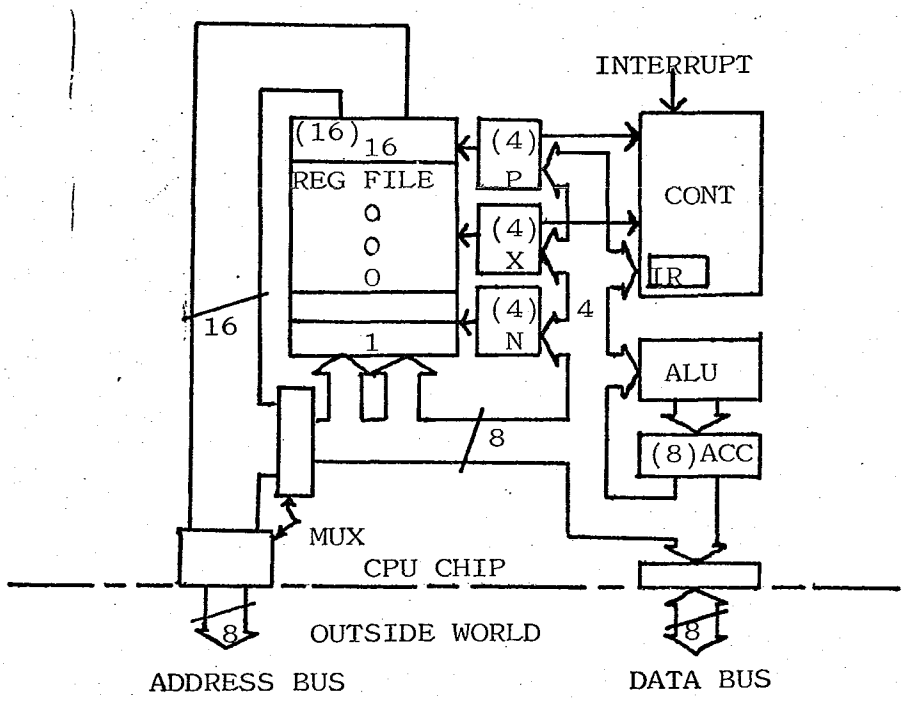


Figure 10. RCA COSMAC μP

at a price not too far above the other PMOS and NMOS microprocessors. That will not happen before the end of the year, however.

ROCKWELL/MICROELECTRONICS, Anaheim, California

MOS/LSI circuits designated as a Parallel Processing System (PPS) are manufactured by Rockwell. The basic PPS-4 family consists of a 4-bit CPU, ROM, RAM, I/O interface in a single 42-pin package plus special printer controller, keyboard and display circuit, and bus interface modules. The CPU utilizes an 8-bit parallel data bus to transfer instructions from ROM to CPU and I/O, and also for data transfer in a dual bidirectional 4-bit mode between the RAMs and I/O and CPU. Operation takes 5 microsec for an instruction cycle, and two 8-digit decimal numbers may be added in 240 microsec. Up to 16K bytes of ROM and 8K x 4-bit words of RAM may be directly addressed, and the PPS can be configured with up to 384 discrete I/Os. As a design aid, Rockwell also provides an evaluation board which contains the CPU, two RAMs, two general-purpose I/Os and a crystal-controlled clock; a ROM emulator or computer simulation of ROM can be used instead of ROM circuits. Assembler and simulator programs for microprogram development on computers offering Fortran IV compilers are available through Tymshare, Inc.

PPS-8 is a bigger, better PPS-4(Refer to Figure 8)

The Rockwell PPS-8 appears to be a scaled-up version of the 4-bit PPS-4. But it is not only bigger; it is better. It has important "second-generation" features such as priority interrupt

and direct-memory access (DMA). The PPS-8 will probably be available to the general marketplace as soon as the other 8080 competitors. Rockwell has not processed chips yet, but it is using the same 4-phase circuit design approach and the same conservative PMOS manufacturing process for the -8 that has been proven out in high-volume production of the -4.

The PPS-8 should be 2-1/2 times faster than the PPS-4. It will be processing twice as many data bits in parallel for one thing, and the nominal clock rate will be 250 kHz vs. 200 kHz for the previous μP. Actual computing throughput will be much faster than this slow external clock rate would suggest. The dynamic 4-phase operation on the chip effectively multiplies the clock rate by four, making it 1 MHz. Overlapped fetch-execute cycles between successive instructions (as in the PPS-4) give a further doubling of the speed. Therefore, despite its slow clock, the PPS-8 is expected to complete instructions in 4 μsec, which puts it in the same speed category as some of the more exotic n-channel contenders, which only have non-overlapped 2-phase operation.

However, the PPS-8 will, like the PPS-4, tend to remain in a class by itself because Rockwell makes no attempt to be compatible with TTL signals and power supplies as do most of the other microprocessor makers. The PPS-8 has a single -17V power supply and comes in Rockwell's special 42 pin package.

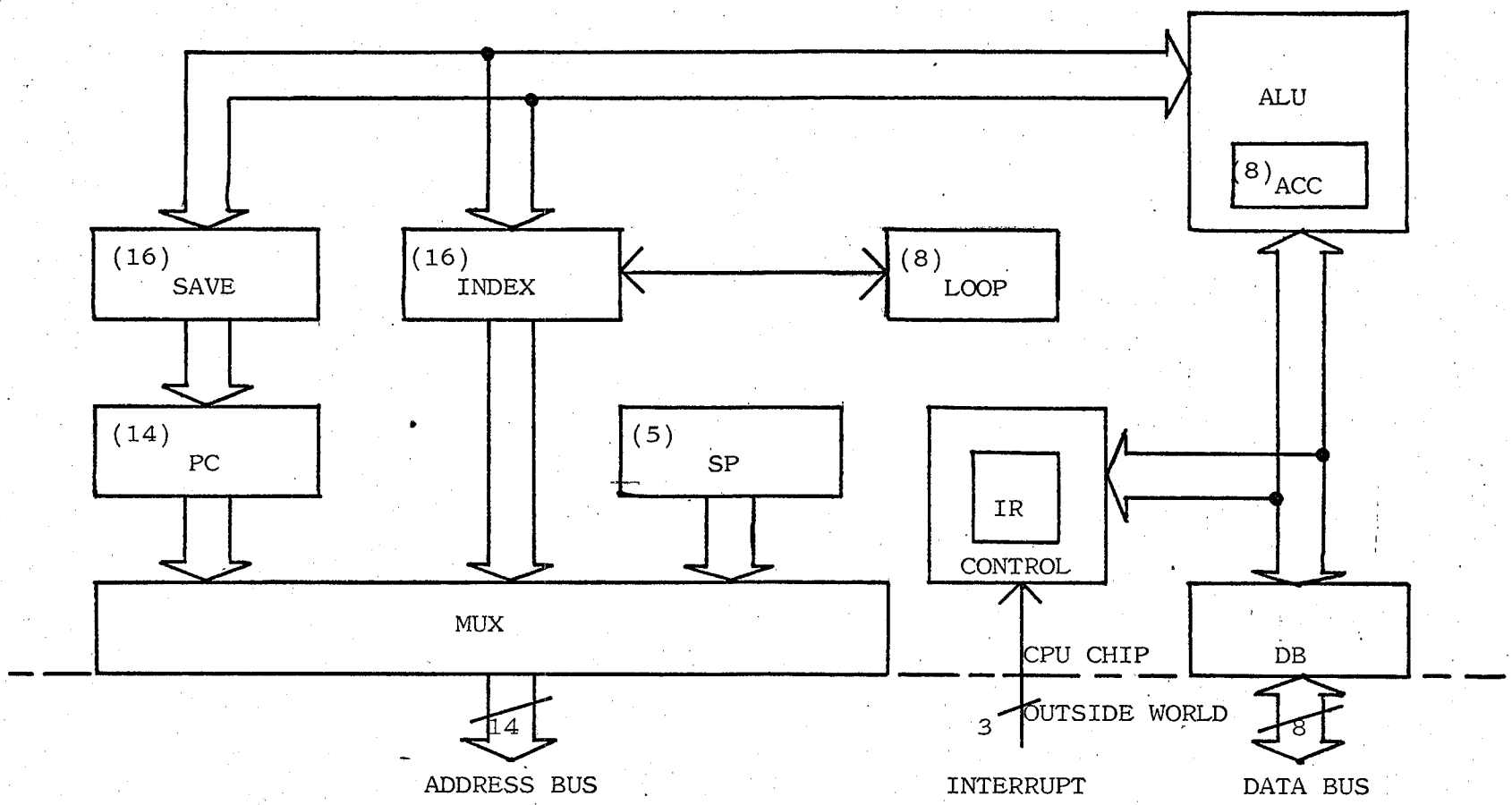


Figure 8. Rockwell PPS-8

As with the PPS-4, Rockwell has provided the PPS-8 CPU with a family of mated PMOS/LSI ROMs and RAMs and I/O devices. The PPS-8 can use two of the members of the PPS-4 family - the clock chips and a simple I/O chip. But new 8-bit wide ROM and RAM chips have been developed for the PPS-8. Also, a more versatile I/O device has been developed especially for the -8.

The PPS-8 follows Rockwell's reasoning that it is only with such a dedicated and optimized family set that the very high-volume user can achieve minimum cost. But Rockwell has maintained interest in the problems of the small-volume user, for it is developing programmable ROMs and nonvolatile MNOS "ROM/RAMs."

SIGNETICS, SUNNYVALE, CALIFORNIA

The Signetics "PIP" (for Programmable Integrated Processor) is generally like the Intel 8080 and the Motorola 6800. It is behind them considerably in schedule because it is just now going through device development. The PIP probably will not be available on even a sample basis until the end of this year.

However, some users may feel it worth waiting for because it ought to be an easy chip to use. Like Motorola, Signetics μP is an n-channel device that runs slow enough (1.25-MHz clock) that it can use a single +5V power supply. But Signetics plans to go one step further than Motorola and use just a single clock input, for the PIP (Figure 9) is a static chip.

It has, however, only half the addressing reach of the other two CPUs as the PIPs address bus is but 15-bits wide. Signetics

says its market surveys indicate the average μP user will only want to address 8k locations, so the 15 lines of the PIP (which will reach 32k locations) is more than adequate. The 16th bit is used for determining whether the address is direct or indirect.

Another difference between the PIP and the Intel and Motorola parts is that the PIP retains the return-address stack on-chip like first generation μP's. This limits the PIP to eight levels of subroutine nesting, but it's faster and allows the user with an all-ROM memory to still have nesting.

Signetics makes use of its own version of the "program status word" (PSW) that IBM has developed for large computers like the 360. The designers have put the assortment of control and feedback bits, that are usually scattered about the architecture, into one "PSW" register. They can thus be moved about "in toto" into the arithmetic or data registers (by their own instructions) where they can be modified or stored away. Fourteen active bits in the PSW allow the programmer to quickly set up the operating mode of the PIP for executing various types of routines, and, if he chooses, to store away applicable PSW's at the beginning of routines.

A list of the 14 bits that Signetics packs into the 2-byte long PSW will indicate the "power" of this architectural twist: three bits for pointer to the return-address stack; two bits for value in the ALU after an arithmetic operation; one bit for

one bit for changing the carry to a borrow for subtraction; one bit for overflow indication; one bit to inhibit interrupt; one bit for sense from outside world; one bit for interdigit carry (for use in BCD operations); two bits to control the compare modes; and a final bit to select which side of the on-chip register bank is being addressed. The PSW feature plus the eight modes of off-chip addressing (about all possible modes in use today) ought to make the PIP worth careful study. These features should allow some users to economize on external ROM and RAM.

TELEDYNE SYSTEMS, Northridge, California

Combing LSI technology with a proprietary microelectronic packaging technique, Teledyne Systems is able to place a complete general-purpose computer in a single 2" x 2" x 0.2" plug-in module. Known as the TDY-52, the series consists of two different microcomputer modules and several RAM, ROM or RAM/ROM units. The TDY-52A is a single component/package microcomputer consisting of a CPU with 8 registers, a 4K x 8-bit microinstruction ROM control memory, a 4K x 8-bit application program RAM, a 2K bit scratchpad RAM, input mux, output buffer registers, priority interrupts, and an oscillator. The TDY-52B, another single-component microcomputer, comes with a 16-bit CPU and registers, priority interrupt, memory and I/O address register, clock generator, timing and control. Memory modules include the TDY-522A, holding 512 x 16 words of RAM and 4096 x 16 words of

ROM; the TDY-522B, an 8K x 16 ROM; the TDY-522C, with either 4K x 4, 2K x 8 or 1K x 16 of RAM; the TDY-522D, a CMOS RAM with 1K x 4 or 512 x 8 capacity. Other special ROM, RAM or ROM/RAM module configurations are also available on special order.

TOSHIBA, Tokyo, Japan

Twelve-bit microprocessor nears minicomputer's performance level. Microprogrammed central processing unit on 12-bits in parallel, respond to eight levels of interrupt, and use an asynchronous bus for both internal and external communications fabricated in the form of an MOS large-scale integrated circuit. One of its unusual features is its 12-bit word length, whereas words in other common microprocessors are limited to 4 or 8 bits. Furthermore, the TLCS-12 is organized around a common asynchronous bus, through which the functional units on the chip communicate with each other and also with external memory, input/output registers, and other system elements (Refer to Figure 11.)

Other significant features include a microprogram in a read-only memory within the microprocessor chip itself, an internal clock generator, and bit-handling instructions capable of modification for indexing and indirect addressing, an automatic start capability, and eight general registers.

The TLCS-12 can not only handle interrupts, but after an interrupt has been processed, the microprocessor can restore to a general register the previous program-status word from temporary storage in the main memory to resume the interrupted program.

Although this concept was first used in large computers about 10 years ago, this is the first time it has been used in a microprocessor.

The 12-bit bidirectional bus contained in the microprocessor itself is also the backbone of the system built around the microprocessor. Data and addresses are both transferred along this bus, but not at the same time. The microprocessor, all memory chips, and input/output registers are connected to the common bus and communicate with one another along it asynchronously, so that devices of any speed can be used.

Central processor has ROM control - The microprocessor itself is a fully parallel 12-bit processor on a chip. It contains a 12-bit parallel arithmetic and logic unit with fast-carry logic and five working registers, a 4,000-bit microprogram in a read-only memory, eight 12-bit general-purpose registers, a timing generator, and an external bus controller. The functional blocks shown in the block diagram are interconnected via the 12-bit bus, which zigzags up and down slightly to the right of the center of the photograph.

Fast-carry logic divides the bits of a computer word into groups and generates the carry from group to group. In the TLCS-12, the groups contain 1 bit, 3 bits, 4 bits, 3 bits, and 1 bit, respectively, generating a carry substantially more quickly than would a simple bit-to-bit carry, which, however, is used within the groups. The bit-to-bit carry out of any bit

position depends, in part, on the carry into that position; thus, under certain circumstances, a single carry can ripple from the least-significant-bit position along the full length of the word. Enough time must be allowed for an add operation to permit this ripple carry. But with carry look-ahead, the ripple occurs in parallel in separate groups, which speeds up the add operation accordingly.

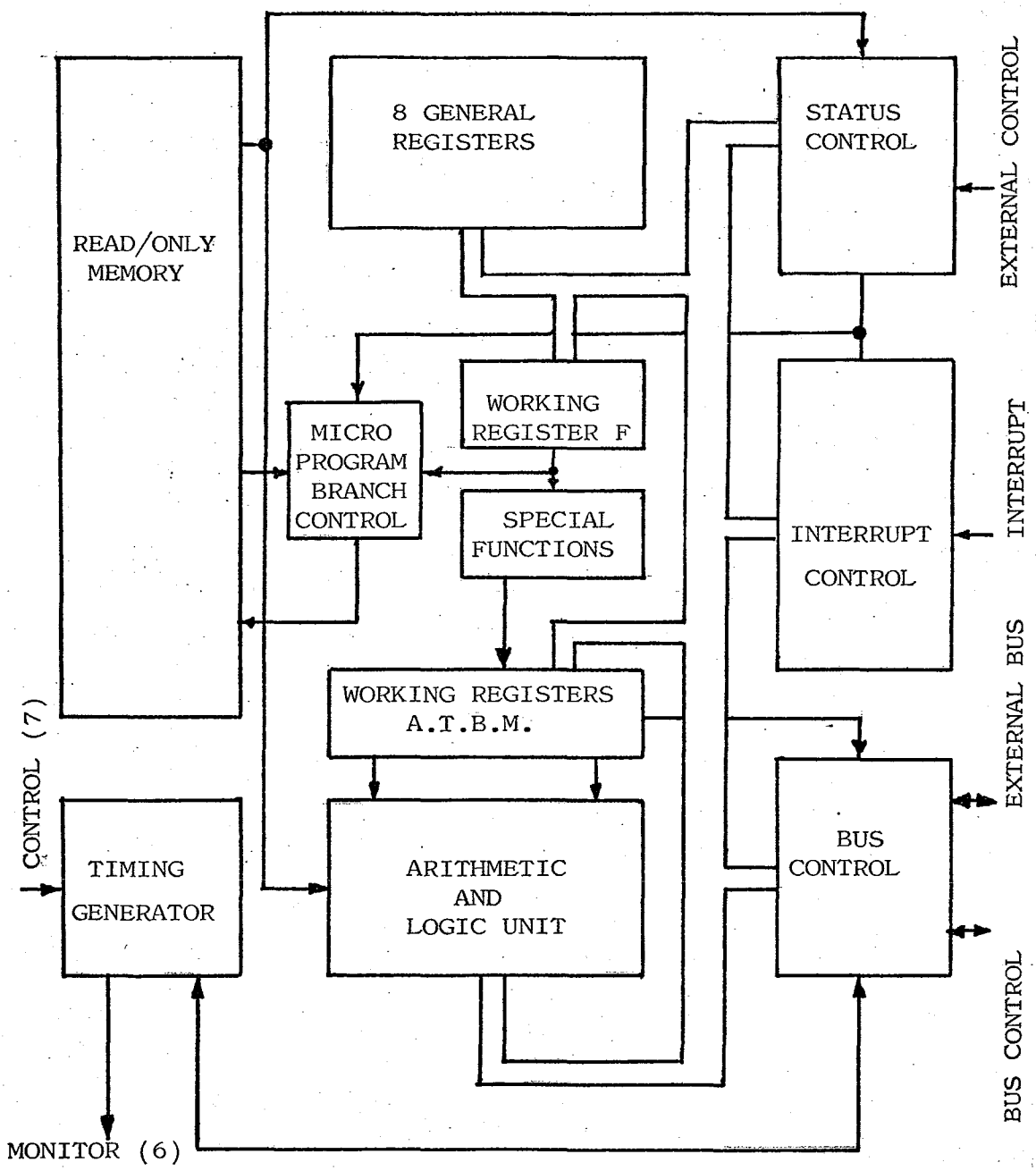


Figure 11. Toshiba TLCS-12

SECTION 4

THE MANUFACTURERS OF MICROCOMPUTERS AND FUTURE SOURCES OF MICROPROCESSORS AND MICROCOMPUTERS

Microprocessors and Microcomputers manufacturers

American Micro Systems, Inc., Santa Clara Calif.

CK114 Serial µcomputer

AMI 7300 8-bit,2chip CPU µcomputer

Applied Computing Technology,

PPS-4MP 4-bit machine

CBC-4 4-bit machine

Computer Automation, Irvine, Calif.

Naked MINI LSI 16-bit cards

Control Logic Inc., Natick, Mass.

L Series 8-bit µcomputer card modules

Digital Equipment Corp., Maynard, Mass.

MPS, PDP-8 8-bit parallel µcomputer

Fairchild Semiconducter, Mt. View, Calif.

PPS-25 7 CPUchips µcomputer has 25 digits max.

(4-bit machine)

FX Systems, Saugerties, N. Y.

MCL--Micrologic controller

General Automation, Anaheim, Calif.

LSI--12/16

General Instruments, Hicksville, N. Y.

CP-1600 16-bit word machine

Intel Corporation, Santa Clara, Calif.

MCS-4

MCS-8

MI^2 Data Systems, Inc., Columbus, Ohio

M^2 8-bit μcomputer

Micro System International, Ottawa, Canada

MP-1 4-bit machine

Monolithic Memories

6701 4-bit bipolar LSI controller

National Semiconducter, Santa Clara, Calif.

IMP-16	16-bit μcomputer
IMP-8	8-bit μcomputer
IMP-4 GPC/P	4-bit slices

Pro-Log Corp. Monterey, Calif.

PLS 400	4-bit μcomputer
PLS 800	8-bit μcomputer

Ratheom/Semiconductor, Mt. View, Calif.

RP16 bipolar 16-bit LSI cards

Future sources of Microprocessors and Microcomputers

The following firms are developing or about to announce their versions of LSI microprocessors.

Electronics Arrays, Mt. View, Calif.

Microsystems International, Palo Alto, Calif.

Monolithic Systems, Englewood, Calif.

Nitron Corporation, Cupertino, Calif.

Western Digital, Newport Beach, Calif.

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6. "MCS-8 Microcomputer Users' Manual," Rev. 4, November, 1973 Intel Corporation, Santa Clara, California

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9. "Intel Data Catalog," September, 1972, Intel Corporation

10. "Microcomputers - One-day Short Course," The University of Santa Clara, California, November, 1973